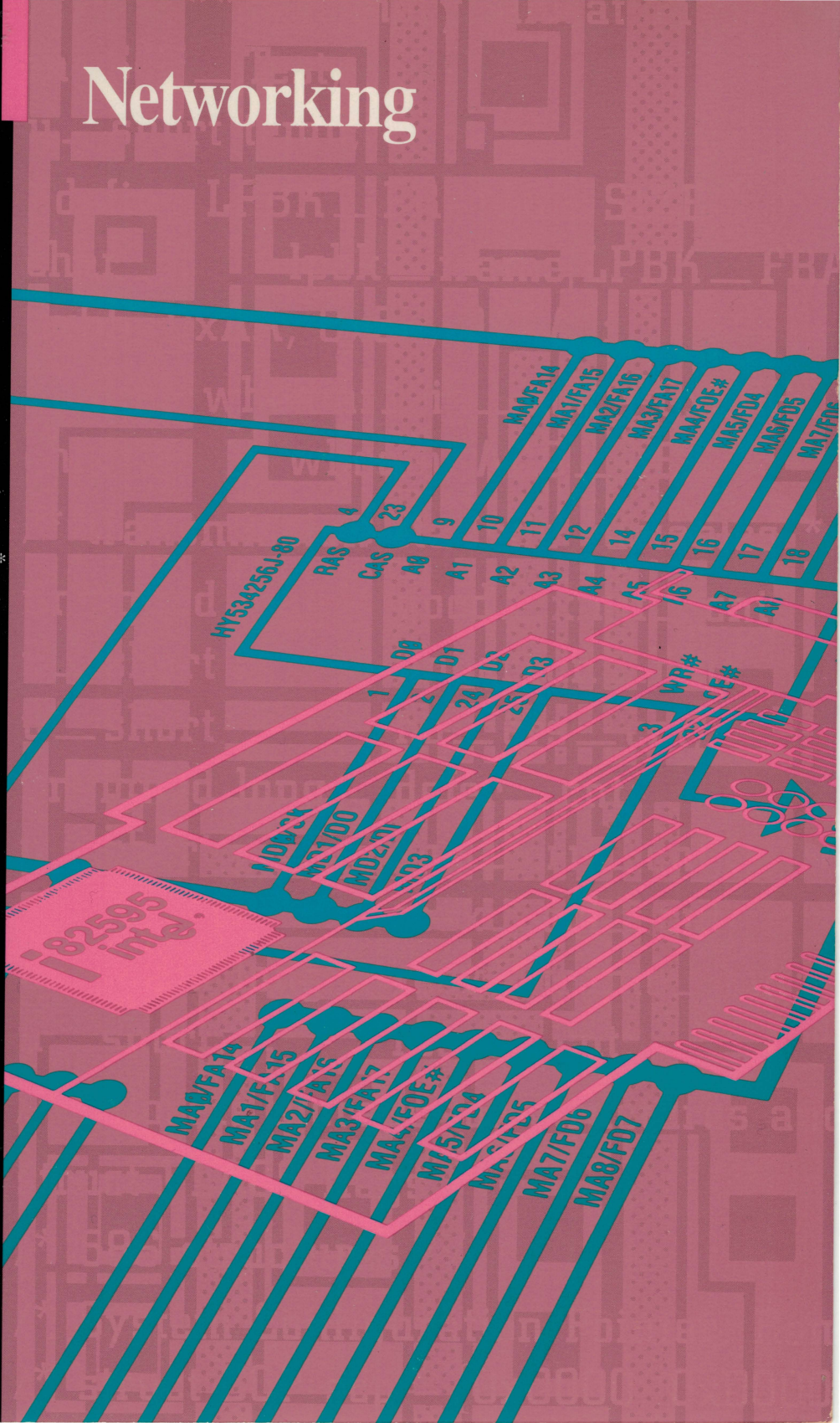
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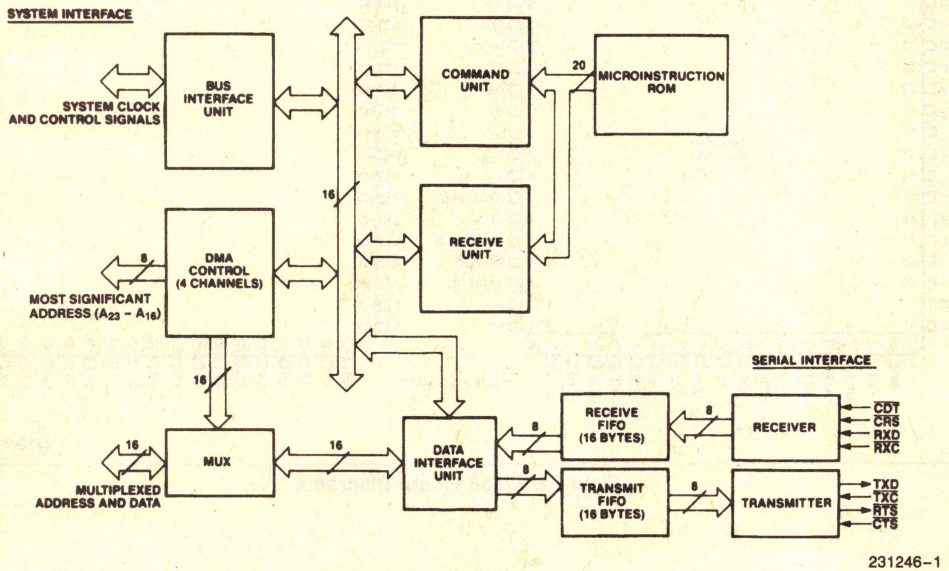
Local Area Network Components

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82586
IEEE 802.3 ETHERNET LAN COPROCESSOR

- **Performs Complete CSMA/CD Medium Access Control Functions Independently of CPU**
  - **— High-Level Command Interface**
- **Supports Established and Emerging LAN Standards**
  - **— IEEE 802.3/Ethernet (10BASE5)**
  - **— IEEE 802.3/Cheapernet (10BASE2)**
  - **— IEEE 802.3/StarLAN (1BASE5)**
  - **— Proposed 10BASE-T**
  - **— Proposed 10BASE-F**
  - **— Proprietary CSMA/CD Networks up to 10 Mb/s**
- **On-Chip Memory Management**
  - **— Automatic Buffer Chaining**
  - **— Buffer Reclaim After Receipt of Bad Frames**
  - **— Save Bad Frames, Optionally**
- **Interfaces to 8-Bit and 16-Bit Microprocessors**
- **48-Pin DIP and 68-Pin PLCC**
  (see "Intel Packaging" Document, Order Number: 231369)
- **Supports Minimum Component Systems**
  - **— Shared Bus Configuration**
  - **— Interface to 80186 and 80188 Microprocessors Without Glue**
- **Supports High-Performance Systems**
  - **— Bus Master, with On-Chip DMA**
  - **— 5-MB/s Bus Bandwidth**
  - **— Compatible with Dual-Port Memory**
  - **— Back-to-Back Frame Reception at 10 Mb/s**
- **Network Management**
  - **— CRC Error Tally**
  - **— Alignment Error Tally**
  - **— Location of Cable Faults**
- **Self-Test Diagnostics**
  - **— Internal Loopback**
  - **— External Loopback**
  - **— Internal Register Dump**
  - **— Backoff Timer Check**

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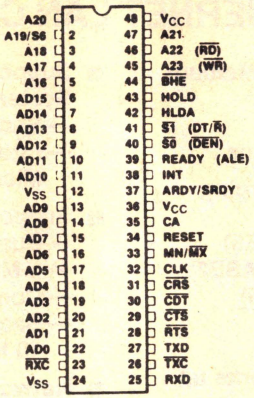


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Figure 1. 82586 Functional Block Diagram

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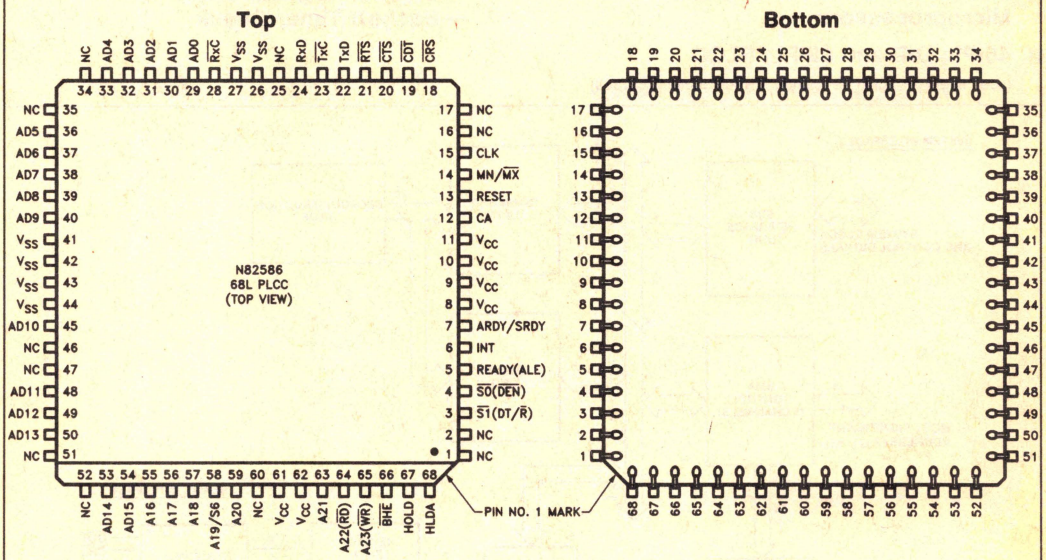
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231246-2

NOTE:
The symbols in parentheses correspond to minimum mode.

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Figure 2. 82586 Pinout Diagrams

The 82586 is an intelligent, high-performance Local Area Network coprocessor, implementing the CSMA/CD access method (Carrier Sense Multiple Access with Collision Detection). It performs all time-critical functions independently of the host processor, which maximizes performance and network efficiency.

The 82586 performs the full set of IEEE 802.3 CSMA/CD Medium Access Control and channel interface functions including: framing, preamble generation and stripping, source address generation, destination address checking, CRC generation and checking, short frame detection. Any data rate up to 10 Mb/s can be used.

The 82586 features a powerful host system interface. It automatically manages memory structures with command chaining and bidirectional data chaining. An on-chip DMA controller manages four channels transparently to the user. Buffers containing errored or collided frames can be automatically recovered. The 82586 can be configured for 8-bit or 16-bit data path, with maximum burst transfer rate of 2 or 4 MB/s respectively. Memory address space is 16 megabytes maximum.

The 82586 provides two independent 16-byte FIFOs, one for receiving and one for transmitting. The threshold for block transfer to/from memory is programmable, enabling the user to optimize bus overhead for a given worst case bus latency.

The 82586 provides a rich set of diagnostic and network management functions including: internal and external loopbacks, exception condition tallies, channel activity indicators, optional capture of all frames regardless of destination address, optional capture of errored or collided frames, and time domain reflectometry for locating faults in the cable.

The 82586 can be used in either baseband or broadband networks. It can be configured for maximum network efficiency (minimum contention overhead) for any length network operating at any data rate up to 10 Mb/s. The controller supports address field lengths of 1, 2, 3, 4, 5, or 6 bytes. It can be configured for either the IEEE 802.3/Ethernet or HDLC method of frame delineation. Both 16-bit and 32-bit CRCs are supported.

The 82586 is fabricated in Intel's reliable HMOS II 5-V technology and is available in a 48-pin DIP or 68-pin PLCC package.

Table 1. 82586 Pin Description

Symbol	48 Pin DIP Pin No.	68 Pin PLCC Pin No.	Type Level	Name and Function
V_{CC}, V_{CC}	48, 36	8, 9, 10, 11, 61, 62		System Power: +5V Power Supply.
V_{SS}, V_{SS}	12, 24	26, 27, 41, 42, 43, 44		System Ground.
RESET	34	13	I TTL	RESET is an active HIGH internally synchronized signal, causing the 82586 to terminate present activity immediately. The signal must be HIGH for at least four clock cycles. The 82586 will execute RESET within ten system clock cycles starting from RESET HIGH. When RESET returns LOW, the 82586 waits for the first CA to begin the initialization sequence.
TxD	27	22	0 TTL	Transmitted Serial Data output signal. This signal is HIGH when not transmitting.
$\overline{TxC}$	26	23	I *	Transmit Data Clock. This signal provides timing information to the internal serial logic, depending upon the mode of data transfer. For NRZ mode of operation, data is transferred to the TxD pin on the HIGH to LOW clock transition.
RxD	25	24	I TTL	Received Data Input Signal.
$\overline{RxC}$	23	28	I *	Received Data Clock. This signal provides timing information to the internal shifting logic depending upon the mode of data transfer. For NRZ data, the state of the RxD pin is sampled on the HIGH to LOW clock transition.

*See D.C. Characteristics.

Table 1. 82586 Pin Description (Continued)

Symbol	48 Pin DIP Pin No.	68 Pin PLCC Pin No.	Type Level	Name and Function
$\overline{RTS}$	28	21	O TTL	Request To Send signal. When LOW, notifies an external interface that the 82586 has data to transmit. It is forced HIGH after a Reset and while the Transmit Serial Unit is not sending data.
$\overline{CTS}$	29	20	I TTL	Active LOW Clear To Send input enables the 82586 transmitter to actually send data. It is normally used as an interface handshake to $\overline{RTS}$. This signal going inactive stops transmission. It is internally synchronized. If $\overline{CTS}$ goes inactive, meeting the setup time to $\overline{TxC}$ negative edge, transmission is stopped and $\overline{RTS}$ goes inactive within, at most, two TxC cycles.
$\overline{CRS}$	31	18	I TTL	Active LOW Carrier Sense input used to notify the 82586 that there is traffic on the serial link. It is used only if the 82586 is configured for external Carrier Sense. When so configured, external circuitry is required for detecting serial link traffic. It is internally synchronized. To be accepted, the signal must stay active for at least two serial clock cycles.
$\overline{CDT}$	30	19	I TTL	Active LOW Collision Detect input is used to notify the 82586 that a collision has occurred. It is used only if the 82586 is configured for external Collision Detect. External circuitry is required for detecting the collision. It is internally synchronized. To be accepted, the signal must stay active for at least two serial clock cycles. During transmission, the 82586 is able to recognize a collision one bit time after preamble transmission has begun.
INT	38	6	O TTL	Active HIGH Interrupt request signal.
CLK	32	15	I MOS	The system clock input from the 80186 or another symmetrical clock generator.
MN/$\overline{MX}$	33	14	I TTL	When HIGH, MN/$\overline{MX}$ selects $\overline{RD}$, $\overline{WR}$, ALE $\overline{DEN}$, DT/$\overline{R}$ (Minimum Mode). When LOW, MN/$\overline{MX}$ selects A22, A23, READY, $\overline{S0}$, $\overline{S1}$ (Maximum Mode). Note: This pin should be static during 82586 operation.
AD0–AD15	6–11, 13–22	29–33, 36–40, 45, 48, 49, 50, 53, 54	I/O TTL	These lines form the time multiplexed memory address (t1) and data (t2, t3, tW, t4) bus. When operating with an 8-bit bus, the high byte will output the address only during T1. AD0–AD15 are floated after a RESET or when the bus is not acquired.
A16–A18 A20–A23	1, 3–5 45–47	55–57, 59, 63–65	O TTL	These lines constitute 7 out of 8 most significant address bits for memory operation. They switch during t1 and stay valid during the entire memory cycle. The lines are floated after RESET or when the bus is not acquired. Address lines A22 and A23 are not available for use in minimum mode.
A19/S6	2	58	O TTL	During t1 it forms line 19 of the memory address. During t2 through t4 it is used as a status indicating that this is a Master peripheral cycle, and is HIGH. Its timing is identical to that of AD0–AD15 during write operation.

Table 1. 82586 Pin Description (Continued)

Symbol	48 Pin DIP Pin No.	68 Pin PLCC Pin No.	Type Level	Name and Function
HOLD	43	67	O TTL	HOLD is an active HIGH signal used by the 82586 to request local bus mastership at the end of the current CPU bus transfer cycle, or at the end of the current DMA burst transfer cycle. In normal operation, HOLD goes inactive before HLDA. The 82586 can be forced off the bus by HLDA going inactive. In this case, HOLD goes inactive within four clock cycles in word mode and eight clock cycles in byte mode.
HLDA	42	68	I TTL	HLDA is an active HIGH Hold Acknowledge signal indicating that the CPU has received the HOLD request and that bus control has been relinquished to the 82586. It is internally synchronized. After HOLD is detected as LOW, the processor drives HLDA LOW. Note, CONNECTING V_{CC} TO HLDA IS NOT ALLOWED because it will cause a deadlock. Users wanting to give permanent bus access to the 82586 should connect HLDA with HOLD.
CA	35	12	I TTL	The CA pin is a Channel Attention input used by the CPU to initiate the 82586 execution of memory resident Command Blocks. The CA signal is synchronized internally. The signal must be HIGH for at least one system clock period. It is latched internally on HIGH to LOW edge and then detected by the 82586.
$\overline{BHE}$	44	66	O TTL	The Bus High Enable signal ($\overline{BHE}$) is used to enable data onto the most significant half of the data bus. Its timing is identical to that of A16–A23. With a 16-bit bus it is LOW and with an 8-bit bus it is HIGH. Note: after RESET, the 82586 is configured to 8-bit bus.
READY	39	5	I TTL	This active HIGH signal is the acknowledgement from the addressed memory that the transfer cycle can be completed. While LOW, it causes wait states to be inserted. This signal must be externally synchronized with the system clock. The Ready signal internal to the 82586 is a logical OR between READY and SRDY/ARDY.
ARDY/SRDY	37	7	I TTL	This active HIGH signal performs the same function as READY. If it is programmed at configure time to SRDY, it is identical to READY. If it is programmed to ARDY, the positive edge of the Ready signal is internally synchronized. Note, the negative edge must still meet setup and hold time specifications, when in ARDY mode. The ARDY signal must be active for at least one system clock HIGH period for proper strobing. The Ready signal internal to the 82586 is a logical OR between READY (in Maximum Mode only) and SRDY/ARDY. Note that following RESET, this pin assumes ARDY mode.

Table 1. 82586 Pin Description (Continued)

Symbol	48 Pin DIP Pin No.	68 Pin PLCC Pin No.	Type Level	Name and Function
$\overline{S0}$, $\overline{S1}$	40,41	4, 3	0 TTL	Maximum mode only. These status pins define the type of DMA transfer during the current memory cycle. They are encoded as follows: $\overline{S1}$ $\overline{S0}$ 0 0 Not Used 0 1 Read Memory 1 0 Write Memory 1 1 Passive Status is active from the middle of t4 to the end of t2. They return to the passive state during t3 or during tW when READY or ARDY is HIGH. These signals can be used by the 8288 Bus Controller to generate all memory control and timing signals.* Any change from the passive state, signals the 8288 to start the next t1 to t4 bus cycle. These pins are pulled HIGH and floated after a system RESET and when the bus is not acquired.
$\overline{RD}$	46	64	0 TTL	Used in minimum mode only. The read strobe indicates that the 82586 is performing a memory read cycle. $\overline{RD}$ is active LOW during t2, t3 and tW of any read cycle. This signal is pulled HIGH and floated after a RESET and when the bus is not acquired.
$\overline{WR}$	45	65	0 TTL	Used in minimum mode only. The write strobe indicates that the 82586 is performing a write memory cycle. $\overline{WR}$ is active LOW during t2, t3 and tW of any write cycle. It is pulled HIGH and floats after RESET and when the bus is not acquired.
ALE	39	5	0 TTL	Used in minimum mode only. Address Latch Enable is provided by the 82586 to latch the address into the 8282/8283 address latch. It is a HIGH pulse, during t1 ('clock low') of any bus cycle. Note that ALE is never floated.
$\overline{DEN}$	40	4	0 TTL	Used in minimum mode only. Data ENable is provided as output enable for the 8286/8287 transceivers in a stand-alone (no 8288) system. $\overline{DEN}$ is active LOW during each memory access. For a read cycle, it is active from the middle of t2 until the beginning of t4. For a write cycle, it is active from the beginning of t2 until the middle of t4. It is pulled HIGH and floats after a system RESET or when the bus is not acquired.
DT/$\overline{R}$	41	3	0 TTL	Used in minimum mode only. DT/$\overline{R}$ is used in non-8288 systems using an 8286/8287 data bus transceiver. It controls the direction of data flow through the Transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$. It becomes valid in the t4 preceding a bus cycle and remains valid until the final t4 of the cycle. This signal is pulled HIGH and floated after a RESET or when the bus is not acquired.

NOTE:
*8288 does not support 10 MHz operation.

82586/HOST CPU INTERACTION

Communication between the 82586 and the host is carried out via shared memory. The 82586's on-chip DMA capability allows autonomous transfer of data blocks (buffers, frames) and relieves the CPU of byte transfer overhead. The 82586 is optimized to interface the iAPX 186, but due to the small number of hardware signals between the 82586 and the CPU, the 82586 can operate easily with other processors. The 82586/host interaction is explained separately in terms of the logical interface and the hardware bus interface.

The 82586 consists of two independent units: Command Unit (CU) and Receive Unit (RU). The CU executes commands from shared memory. The RU handles all activities related to frame reception. The CU and RU enable the 82586 to engage in the two types of activities simultaneously: the CU may be fetching and executing commands out of memory, and the RU may be storing received frames in memory. CPU intervention is only required after the CU executes a sequence of commands or the RU stores a sequence of frames.

The only hardware signals that connect the CPU and the 82586 are INTERRUPT and CHANNEL ATTENTION (see Figure 3). Interrupt is used by the 82586 to draw the CPU's attention to a change in the contents of the SCB. Channel Attention is used by the CPU to draw the 82586's attention.

82586 SYSTEM MEMORY STRUCTURE

The Shared Memory structure consists of four parts: Initialization Root, System Control Block (SCB), Command List, and Receive Frame Area (RFA) (see Figure 4).

The Initialization Root is at a predetermined location in the memory space, (0FFFFF6H), known to both the host CPU and the 82586. The root is accessed at initialization and points to the System Control Block.

The System Control Block (SCB) functions as a bidirectional mail drop between the host CPU, CU and RU. It is the central element through which the CPU and the 82586 exchange control and status information. The SCB consists of two parts, the first of which entails instructions from the CPU to the 82586. These include: control of the CU and RU (START, ABORT, SUSPEND, RESUME), a pointer to the list of commands for the CU, a pointer to the receive frame area, and a set of Interrupt acknowledge bits. The second entails status information keyed by the 82586 to the CPU, including: state of the CU and RU (e.g. IDLE, ACTIVE READY, SUSPENDED, NO RECEIVE RESOURCES), interrupts bits (command completed, frame received, CU not ready, RU not ready), and statistics (see Figure 4).

The Command List serves as a program for the CU. Individual commands are placed in memory units called a Command Block, or CB. CB's contain command specific parameters and command specific statuses. Specifically, these high level commands are called Action Commands (e.g. Transmit, Configure).

A specific command, Transmit, causes transmission of a frame by the 82586. The Transmit command block includes Destination Address, Length Field, and a pointer to a list of linked buffers that holds the frame to be constructed from several buffers scattered in memory. The Command Unit performs with-

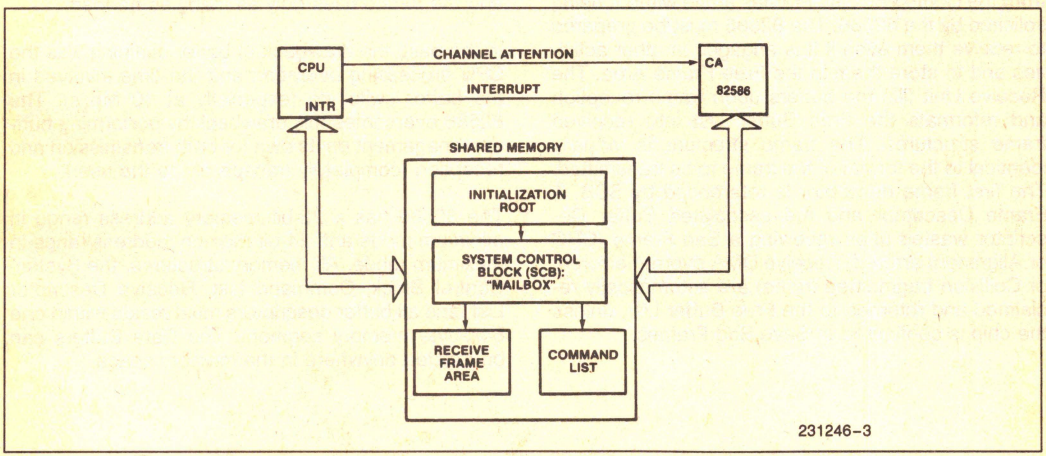


Figure 3. 82586/Host CPU Interaction

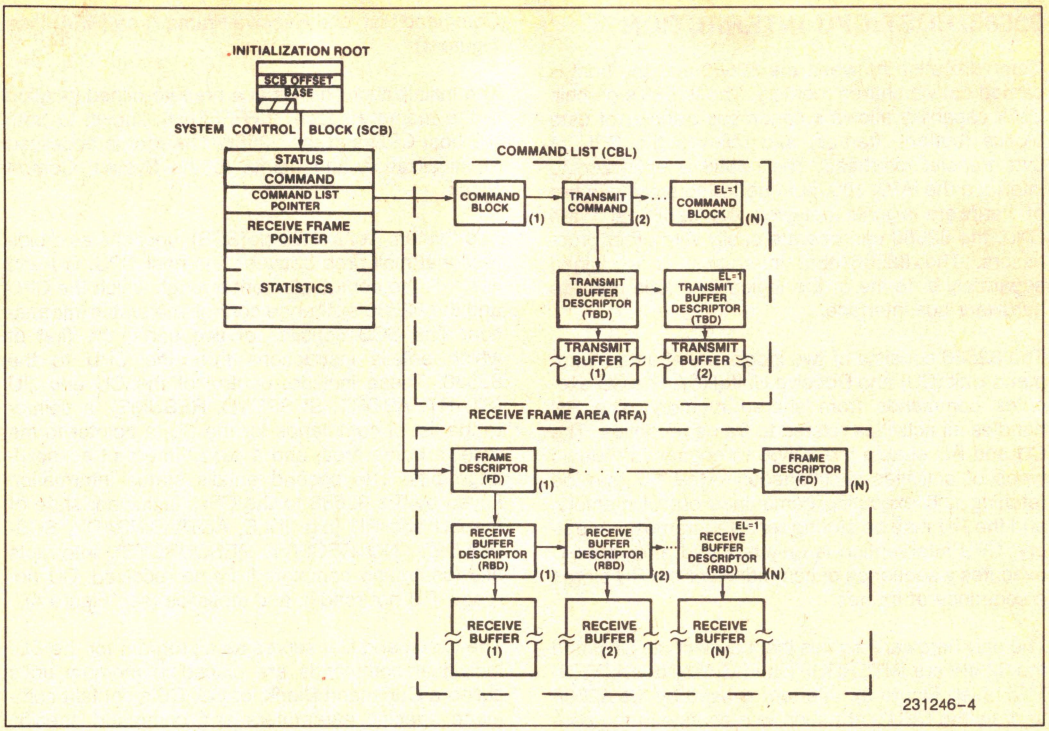


Figure 4. 82586 Shared Memory Structure

out the CPU intervention, the DMA of each buffer and the prefetching of references to new buffers in parallel. The CPU is notified only after successful transmission or retransmission.

The Receive Frame Area is a list of Free Frame Descriptors (Descriptors not yet used) and a list of buffers prepared by the user. It is conceptually distinct from the Command List. Frames arrive without being solicited by the 82586. The 82586 must be prepared to receive them even if it is engaged in other activities and to store them in the Free Frame Area. The Receive Unit fills the buffers upon frame reception and reformats the Free Buffer List into received frame structures. The frame structure is virtually identical to the format of the frame to be transmitted. The first frame descriptor is referenced by SCB. A Frame Descriptor and the associated Buffer Descriptor wasted upon receiving a Bad Frame (CRC or Alignment errored, Receive DMA overrun errored, or Collision fragmented frame) are automatically reclaimed and returned to the Free Buffer List, unless the chip is configured to Save Bad Frames.

Receive buffer chaining (i.e. storing incoming frames in a linked list of buffers) improves memory utilization significantly. Without buffer chaining, the user must allocate consecutive blocks of the maximum frame size (1518 bytes in Ethernet) for each frame. Taking into account that a typical frame size may be about 100 bytes, this practice is very inefficient. With buffer chaining, the user can allocate small buffers and the 82586 uses only as many as needed.

In the past, the drawback of buffer chaining was the CPU processing overhead and the time involved in the buffer switching (especially at 10 Mb/s). The 82586 overcomes this drawback by performing buffer management on its own for both transmission and reception (completely transparent to the user).

The 82586 has a 22-bit memory address range in minimum mode and 24-bit memory address range in maximum mode. All memory structures, the System Control Block, Command List, Receive Descriptor List, and all buffer descriptors must reside within one 64K-byte memory segment. The Data Buffers can be located anywhere in the memory space.

TRANSMITTING FRAMES

The 82586 executes high level action commands from the Command List in external memory. Action commands are fetched and executed in parallel with the host CPU's operation, thereby significantly improving system performance. The general action commands format is shown in Figure 5.

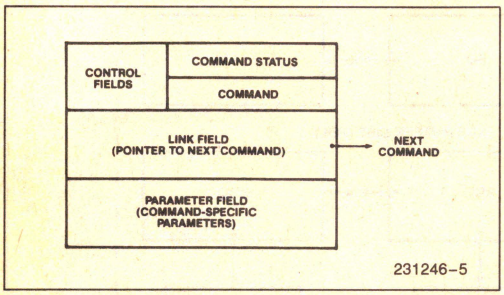


Figure 5. Action Command Format

Message transmission is accomplished by using the Transmit command. A single Transmit command contains, as part of the command-specific parameters, the destination address and length field for the transmitted frame along with a pointer to a buffer area in memory containing the data portion of the frame. (See Figure 15.) The data field is contained in a memory data structure consisting of a Buffer Descriptor (BD) and Data Buffer (or a linked list of buffer descriptors and buffers) as shown in Figure 6. The BD contains a Link Field which points to the next BD on the list and a 24-bit address pointing to the Data Buffer itself. The length of the Data Buffer is specified by the Actual Count field of the BD.

Using the BD's and Data Buffers, multiple Data Buffers can be 'chained' together. Thus, a frame with a long Data Field can be transmitted using multiple (shorter) Data buffers chained together. This chaining technique allows the system designer to develop efficient buffer management policies.

The 82586 automatically generates the preamble (alternating 1's and 0's) and start frame delimiter, fetches the destination address and length field from the Transmit command, inserts its unique address as the source address, fetches the data field from

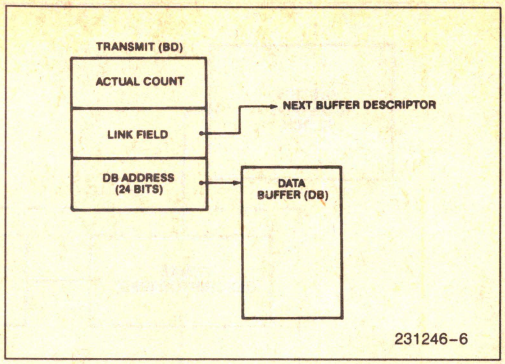


Figure 6. Data Buffer Descriptor and Data Buffer Structure

buffers pointed to by the Transmit command, and computes and appends the CRC at the end of the frame. See Figure 7.

The 82586 can be configured to generate either the Ethernet or HDLC start and end frame delimiters. In the Ethernet mode, the start frame delimiter is 10101011 and the end frame delimiter indicated by the lack of a signal after transmitting the last bit of the frame check sequence field. When in the HDLC mode, the 82586 will generate the 01111110 'flag' for the start and end frame delimiters and perform the standard 'bit stuffing/stripping'. In addition, the 82586 will optionally pad frames that are shorter than the specified minimum frame length by appending the appropriate number of flags to the end of the frame.

In the event of a collision (or collisions), the 82586 manages the entire jam, random wait and retry process, reinitializing DMA pointers without CPU intervention. Multiple frames can be sent by linking the appropriate number of Transmit commands together. This is particularly useful when transmitting a message that is larger than the maximum frame size (1518 bytes for Ethernet).

RECEIVING FRAMES

In order to minimize CPU overhead, the 82586 is designed to receive frames without CPU supervision. The host CPU first sets aside an adequate

PREAMBLE	START FRAME DELIMITER	DEST ADDR	SOURCE ADDR	LENGTH FIELD	DATA FIELD	FRAME CHECK SEQUENCE	END FRAME DELIMITER

Figure 7. Frame Format

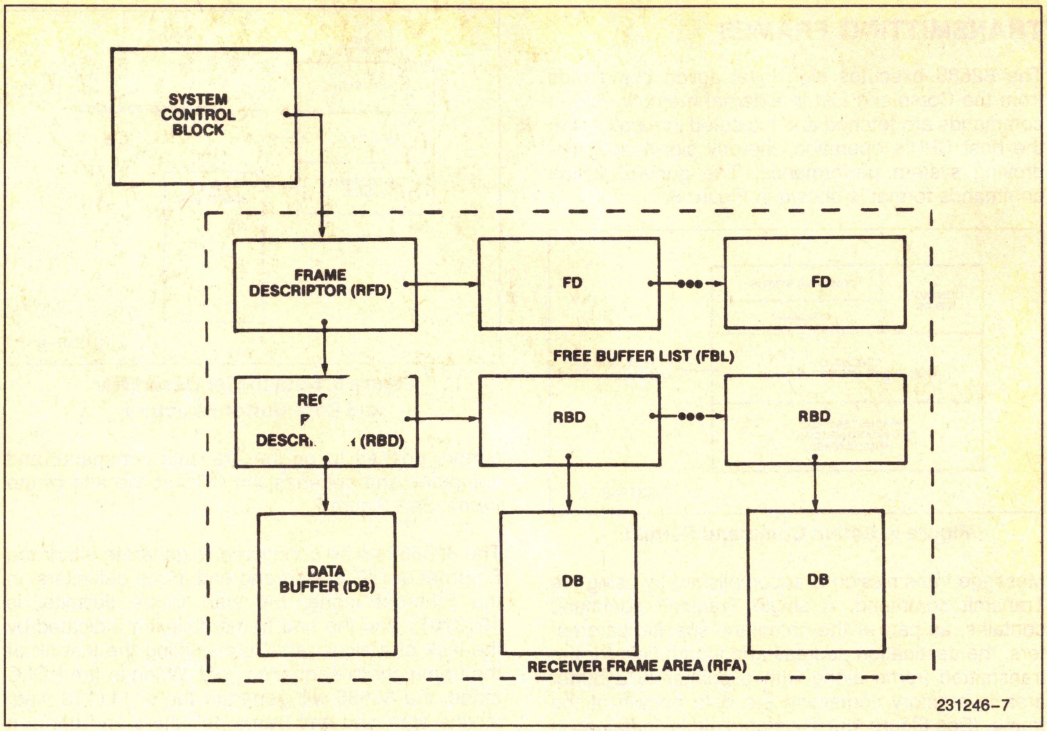


Figure 8. Receive Frame Area Diagram

amount of receive buffer space and then enables the 82586's Receive Unit. Once enabled, the RU 'watches' for any of its frames which it automatically stores in the Receive Frame Area (RFA). The RFA consists of a Receive Descriptor List (RDL) and a list of free buffers called the Free Buffer List (FBL) as shown in Figure 8. The individual Receive Frame Descriptors that make up the RDL are used by the 82586 to store the destination and source address, length field and status of each frame that is received. (Figure 9.)

The 82586, once enabled, checks each passing frame for an address match. The 82586 will recognize its own unique address, one or more multicast addresses or the broadcast address. If a match occurs, it stores the destination and source address and length field in the next available RFD. It then begins filling the next free Data Buffer on the FBL (which is pointed to by the current RFD) with the data portion of the incoming frame. As one DB is filled, the 82586 automatically fetches the next DB on the FBL until the entire frame is received. This buffer chaining technique is particularly memory efficient because it allows the system designer to set aside buffers that fit a frame size that may be much shorter than the maximum allowable frame.

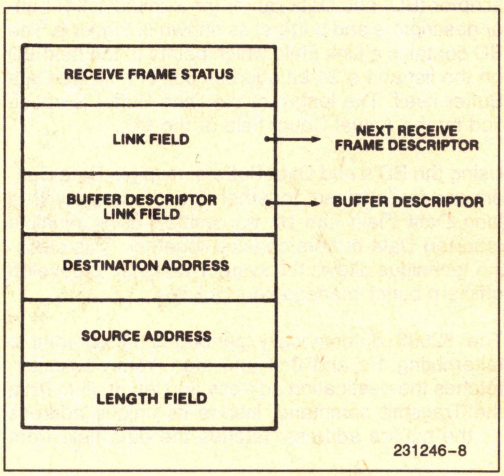


Figure 9. Receive Frame Descriptor

Once the entire frame is received without error, the 82586 performs the following housekeeping tasks:

- Updates the Actual Count field of the last Buffer Descriptor used to hold the frame just received with the number of bytes stored in its associated Data Buffer.

- Fetches the address of the next free Receive Frame Descriptor.
- Writes the address of the next free Buffer Descriptor into the next free Receive Frame Descriptor.
- Posts a 'Frame Received' interrupt status bit in the SCB.
- Interrupts the CPU.

In the event of a frame error, such as a CRC error, the 82586 automatically reinitializes its DMA pointers and reclaims any data buffers containing the bad frame. As long as Receive Frame Descriptors and data buffers are available, the 82586 will continue to receive frames without further CPU help.

82586 NETWORK MANAGEMENT AND DIAGNOSTIC FUNCTIONS

The behavior of data communication networks is typically very complex due to their distributed and asynchronous nature. It is particularly difficult to pinpoint a failure when it occurs. The 82586 was designed in anticipation of these problems and includes a set of features for improving reliability and testability.

The 82586 reports on the following events after each frame transmitted:

- Transmission successful.
- Transmission unsuccessful; lost Carrier Sense.
- Transmission unsuccessful; lost Clear-to-Send.
- Transmission unsuccessful; DMA underrun because the system bus did not keep up with the transmission.
- Transmission unsuccessful; number of collisions exceeded the maximum allowed.

The 82586 checks each incoming frame and reports on the following errors, (if configured to 'Save Bad Frame'):

- CRC error: incorrect CRC in a well aligned frame.
- Alignment error: incorrect CRC in a misaligned frame.
- Frame too short: the frame is shorter than the configured value for minimum frame length.
- Overrun: the frame was not completely placed in memory because the system bus did not keep up with incoming data.
- Out of buffers: no memory resources to store the frame, so part of the frame was discarded.

NETWORK PLANNING AND MAINTENANCE

To perform proper planning, operation, and maintenance of a communication network, the network management entity must accumulate information on network behavior. The 82586 provides a rich set of network-wide diagnostics that can serve as the basis for a network management entity.

Network Activity information is provided in the status of each frame transmitted. The activity indicators are:

- Number of collisions: number of collisions the 82586 experienced in attempting to transmit this frame.
- Deferred transmission: indicates if the 82586 had to defer to traffic on the link during the first transmission attempt.

Statistics registers are updated after each received frame that passes the address filtering, and is longer than the Minimum Frame Length configuration parameter.

- CRC errors: number of frames that experienced a CRC error and were properly aligned.
- Alignment errors: number of frames that experienced a CRC error and were misaligned.
- No-resources: number of correct frames lost due to lack of memory resources.
- Overrun errors: number of frame sequences lost due to DMA overrun.

The 82586 can be configured to Promiscuous Mode. In this mode it captures all frames transmitted on the Network without checking the Destination Address. This is useful in implementing a monitoring station to capture all frames for analysis.

The 82586 is capable of determining if there is a short or open circuit anywhere in the Network using the built in Time Domain Reflectometer (TDR) mechanism.

STATION DIAGNOSTICS

The chip can be configured to External Loopback. The transmitter to receiver interconnection can be placed anywhere between the 82586 and the link to locate faults, for example: the 82586 output pins, the Serial Interface Unit, the Transceiver cable, or in the Transceiver.

The 82586 has a mechanism recognizing the transceiver 'heart beat' signal for verifying the correct operation of the Transceiver's collision detection circuitry.

82586 SELF TESTING

The 82586 can be configured to Internal Loopback. It disconnects itself from the Serial Interface Unit, and any frame transmitted is received immediately. The 82586 connects the Transmit Data to the Receive Data signal and the Transmit Clock to the Receive Clock.

The Dump Command causes the chip to write over 100 bytes of its internal registers to memory.

The Diagnose command checks the exponential Backoff random number generator internal to the 82586.

CONTROLLING THE 82586

The CPU controls operation of the 82586's Command Unit (CU) and Receive Unit (RU) of the 82586 via the System Control Block.

THE COMMAND UNIT (CU)

The Command Unit is the logical unit that executes Action Commands from a list of commands very similar to a CPU program. A Command Block (CB) is associated with each Action Command.

The CU can be modeled as a logical machine that takes, at any given time, one of the following states:

- IDLE—CU is not executing a command and is not associated with a CB on the list. This is the initial state.
- SUSPENDED—CU is not executing a command but (different from IDLE) is associated with a CB on the list.
- ACTIVE—CU is currently executing an Action Command, and points to its CB.

The CPU may affect the CU operation in two ways: issuing a CU control Command or setting bits in the COMMAND word of the Action Command.

THE RECEIVE UNIT (RU)

The Receive Unit is the logical unit that receives frames and stores them in memory.

The RU is modeled as a logical machine that takes, at any given time, one of the following states:

- IDLE—RU has no memory resources and is discarding incoming frames. This is the initial RU state.
- NO-RESOURCES—RU has no memory resources and is discarding incoming frames. This state differs from the IDLE state in that RU accumulates statistics on the number of frames it had to discard.
- SUSPENDED—RU has free memory resources to store incoming frames but discard them anyway.

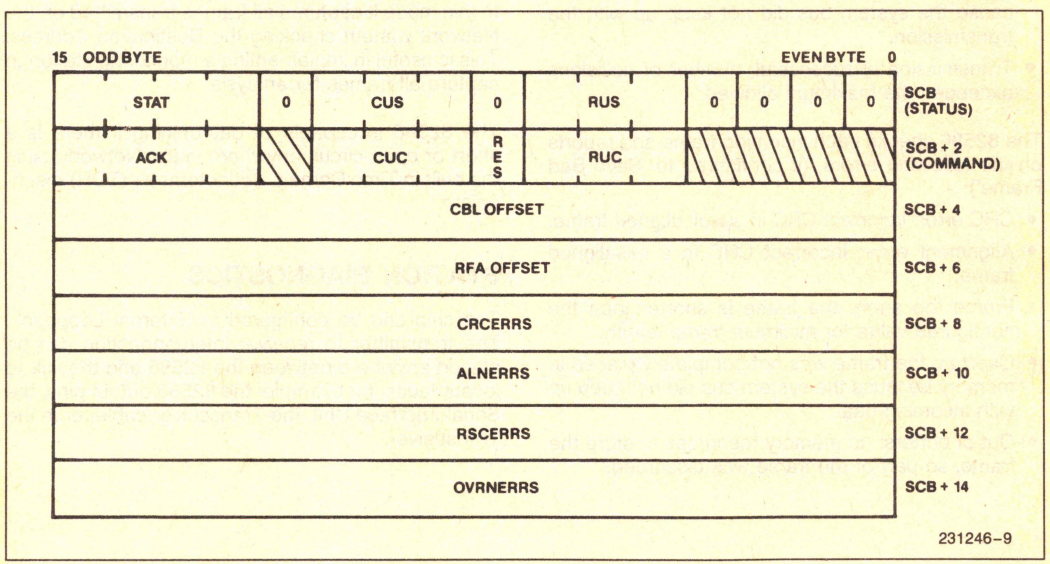


Figure 10. System Control Block (SCB) Format

- READY—RU has free memory resources and stores incoming frames.

The CPU may affect RU operation in three ways: issuing an RU Control Command, setting bits in Frame Descriptor, FD, COMMAND word of the frame currently being received, or setting EL bit of Buffer Descriptor, BD, of the buffer currently being filled.

SYSTEM CONTROL BLOCK (SCB)

The System Control Block is the communication mail-box between the 82586 and the host CPU. The SCB format is shown in Figure 10.

The host CPU issues Control Commands to the 82586 via the SCB. These commands may appear at any time during routine operation, as determined by the host CPU. After the required Control Command is setup, the CPU sends a CA signal to the 82586.

SCB is also used by the 82586 to return status information to the host CPU. After inserting the required status bits into SCB, the 82586 issues an Interrupt to the CPU.

The format is as follows:

STATUS word: Indicates the status of the 82586. This word is modified only by the 82586. Defined bits are:

CX	(Bit 15)	• A command in the CBL having its 'I' (interrupt) bit set has been executed.
FR	(Bit 14)	• A frame has been received.
CNR	(Bit 13)	• The Command Unit left the Active state.
RNR	(Bit 12)	• The Receive Unit left the Ready state.
CUS	(Bits 8–10)	• (3 bits) this field contains the status of the Command Unit. Valid values are: 0 — Idle 1 — Suspended 2 — Active 3–7 — Not Used
RUS	(Bits 4—6)	• (3 bits) this field contains the status of the Receive Unit. Valid values are: 0 — Idle 1 — Suspended 2 — No Resources 3 — Not Used 4 — Ready 5–7 — Not Used

COMMAND word: Specifies the action to be performed as a result of the CA. This word is set by the CPU and cleared by the 82586. Defined bits are:

ACK-CX	(Bit 15)	• Acknowledges the command executed event.
ACK-FR	(Bit 14)	• Acknowledges the frame received event.
ACK-CNA	(Bit 13)	• Acknowledes that the Command Unit became not ready.
ACK-RNR	(Bit 12)	• Acknowledges that the Receive Unit became not ready.
CUC	(Bits 8–10)	• (3 bits) this field contains the command to the Command Unit.
	0	• NOP (doesn't affect current state of the unit).
	1	• Start execution of the first command on the CBL. If a command is in execution, then complete it before starting the new CBL. The beginning of the CBL is in CBL OFFSET.
	2	• Resume the operation of the command unit by executing the next command. This operation assumes that the command unit has been previously suspended.
	3	• Suspend execution of commands on CBL after current command is complete.
	4	• Abort execution of commands immediately.
	5–7	• Reserved, illegal for use.
RUC	(Bits 4–6)	• (3 bits) This field contains the command to the receive unit. Valid values are:
	0	• NCP (does not alter current state of unit).
	1	• Start reception of frames. If a frame is being received, then complete reception before starting. The beginning of the RFA is contained in the RFA OFFSET.
	2	• Resume frame receiving (only when in suspended state.)
	3	• Suspend frame receiving. If a frame is being received, then complete its reception before suspending.
	4	• Abort receiver operation immediately.
	5–7	• Reserved, illegal for use.
RESET	(Bit 7)	• Reset chip (logically the same as hardware RESET).

CBL-OFFSET:

Gives the 16-bit offset address of the first command (Action Command) in the command list to be executed following CU-START. Thus, the 82586 reads this word only if the CUC field contained a CU-START Control Command.

RFA-OFFSET:

Points to the first Receive Frame Descriptor in the Receive Frame Area.

CRCERRS:

CRC Errors - contains the number of properly aligned frames received with a CRC error.

ALNERRS:

Alignment Errors - contains the number of misaligned frames received with a CRC error.

RSCERRS:

Resource Errors - records the number of correct incoming frames discarded due to lack of memory resources (buffer space or received frame descriptors).

OVRNERRS:

Overrun Errors - counts the number of received frame sequences lost because the memory bus was not available in time to transfer them.

ACTION COMMANDS

The 82586 executes a 'program' that is made up of action commands in the Command List. As shown in Figure 5, each command contains the command field, status and control fields, link to the next action command in the CL, and any command-specific parameters. This command format is called the Command Block.

The 82586 has a repertoire of 8 commands:

NOP
Setup Individual Address
Configure
Setup Multicast Address
Transmit
TDR
Diagnose
Dump

NOP

This command results in no action by the 82586, except as performed in normal command processing. It is present to aid in Command List manipulation.

NOP command includes the following fields:

STATUS word (written by 82586):

C	(Bit 15)	• Command Completed
B	(Bit 14)	• Busy Executing Command
OK	(Bit 13)	• Error Free Completion

COMMAND word:

EL	(Bit 15)	• End of Command List
S	(Bit 14)	• Suspend After Completion
I	(Bit 13)	• Interrupt After Completion
CMD	(Bits 0–2)	• NOP = 0

LINK OFFSET: Address of next Command Block

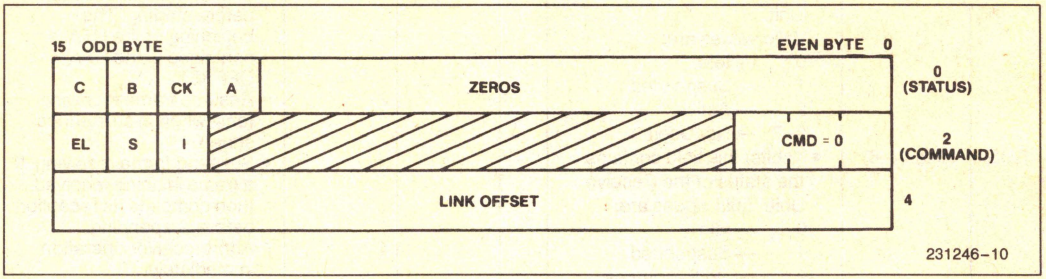


Figure 11. The NOP Command Block

IA-SETUP

This command loads the 82586 with the Individual Address. This address is used by the 82586 for recognition of Destination Address during reception and insertion of Source Address during transmission.

The IA-SETUP command includes the following fields:

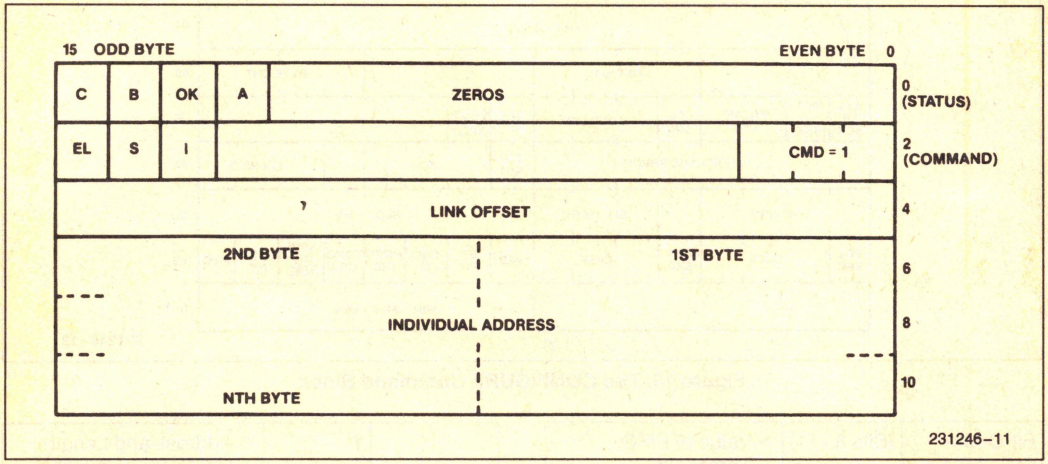


Figure 12. The IA-SETUP Command Block

STATUS word (written by 82586).

C	(Bit 15)	• Command Completed
B	(Bit 14)	• Busy Executing Command
OK	(Bit 13)	• Error Free Completion
A	(Bit 12)	• Command Aborted

COMMAND word:

EL	(Bit 15)	• End of Command List
S	(Bit 14)	• Suspend After Completion
I	(Bit 13)	• Interrupt After Completion
CMD	(Bits 0–2)	• IA-SETUP = 1

LINK OFFSET: Address of next Command Block

INDIVIDUAL ADDRESS: Individual Address parameter

The least significant bit of the Individual Address parameter must be zero for IEEE 802.3/Ethernet. However, no enforcement of 0 is provided by the 82586. Thus, an Individual Address with least significant bit 1, is possible.

CONFIGURE

The CONFIGURE command is used to update the 82586 operating parameters.

The CONFIGURE command includes the following fields:

STATUS word (written by 82586):

C	(Bit 15)	• Command Completed
B	(Bit 14)	• Busy Executing Command
OK	(Bit 13)	• Error Free Completion
A	(Bit 12)	• Command Aborted

COMMAND word:

EL	(Bit 15)	• End of Command List
S	(Bit 14)	• Suspend After Completion
I	(Bit 13)	• Interrupt After Completion
CMD	(Bits 0–2)	• Configure = 2

LINK OFFSET: Address of next Command Block

Byte 6–7:

BYTE CNT	(Bits 0–3)	• Byte Count, Number of bytes including this one, holding the parameters to be configured. A number smaller than 4 is interpreted as 4. A number greater than 12 is interpreted as 12.

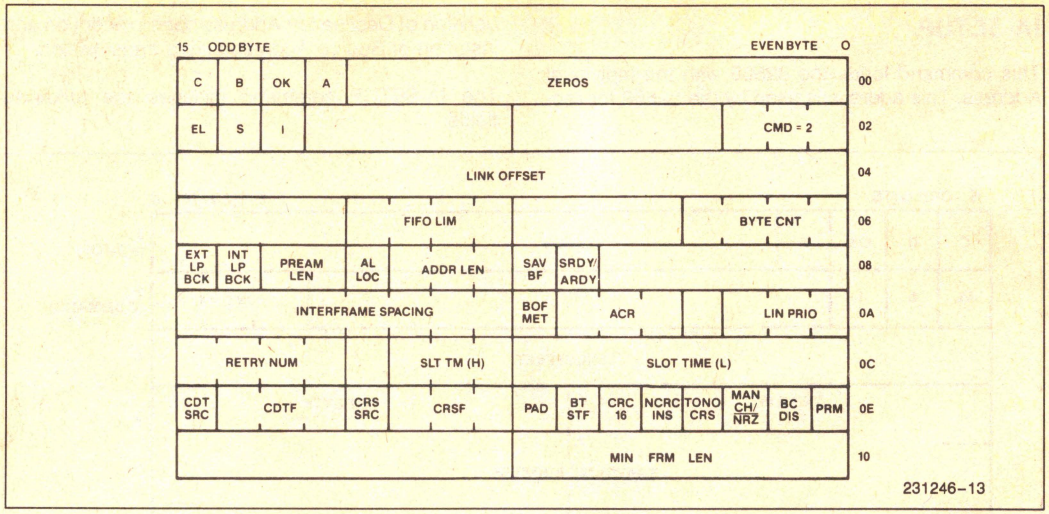


Figure 13. The CONFIGURE Command Block

FIFO-LIM	(Bits 8–11)	• Value of FIFO Threshold.

Byte 8–9:

SRDY/ARDY	(Bit 6)	
	0	• SRDY/ARDY pin operates as ARDY (internal synchronization).
	1	• SRDY/ARDY pin operates as SRDY (external synchronization).
SAV-BF	(Bit 7)	
	0	• Received bad frames are not saved in memory.
	1	• Received bad frames are saved in memory.
ADD-LEN	(Bits 8–10)	• Number of address byes. NOTE: 7 is interpreted as 0.
AL-LOC	(Bit 11)	
	0	• Address and Length Fields separated from data and associated with Transmit Command Block or Receive Frame Descriptor. For transmitted Frame, Source Address is inserted by the 82586.
	1	• Address and Length Fields are part of the Transmit/Receive data buffers, including Source Address (which is not inserted by the 82586).
PREAM-LEN	(Bits 12–13)	• Preamble Length including Beginning of Frame indicator: 00 - 2 bytes 01 - 4 bytes 10 - 8 bytes 11 - 16 bytes
INT-LPBCK	(Bit 14)	• Internal Loopback
EXT-LPBCK	(Bit 15)	• External Loopback. NOTE: Bits 14 and 15 configured to 1, cause Internal Loopback.

Byte 10–11:

LIN-PRIO	(Bits 0–2)	• Linear Priority
ACR	(Bits 4–6)	• Accelerated Contention Resolution (Exponential Priority)
BOF-MET	(Bit 7)	• Exponential Backoff Method 0 - IEEE 802.3/Ethernet 1 - Alternate Method

INTER FRAME SPACING	(Bits 8–15)	• Number indicating the Interframe Spacing in TxC period units.

Byte 12–13:

SLOT-TIME (L)	(Bits 0–7)	• Slot Time Number, Low Byte
SLT-TM (H)	(Bits 8–10)	• Slot Time Number, High Bits
RETRY-NUM	(Bits 12–15)	• Maximum Number of Transmission Retries on Collisions

Byte 14–15:

PRM	(Bit 0)	• Promiscuous Mode
BC-DIS	(Bit 1)	• Broadcast Disable
MANCH/$\overline{NRZ}$	(Bit 2)	• Manchester or NRZ • Encoding/Decoding
	0	• NRZ
	1	• Manchester
TONO-CRS	(Bit 3)	• Transmit on No Carrier Sense
	0	• Cease Transmission if $\overline{CRS}$ Goes Inactive During Frame Transmission
	1	• Continue Transmission Even if no Carrier Sense
NCRC-INS	(Bit 4)	• No CRC Insertion
CRC-16	(Bit 5)	• CRC Type:
	0	• 32 bit Autodin II CRC Polynomial
	1	• 16 bit CCITT CRC Polynomial
BT-STF	(Bit 6)	• Bitstuffing:
	0	• End of Carrier Mode (Ethernet)
	1	• HDLC like Bitstuffing Mode
PAD	(Bit 7)	• Padding
	0	• No Padding
	1	• Perform Padding by Transmitting Flags for Remainder of Slot Time
CRSF	(Bits 8–9)	• Carrier Sense Filter in Bit Times
CRS-SRC	(Bit 11)	• Carrier Sense Source
	0	• External
	1	• Internal
CDTF	(Bits 12–14	• Collision Detect Filter in Bit Times
CDT-SRC	(Bit 15)	• Collision Detect Source
	0	• External
	1	• Internal

Byte 16:

MIN-FRM-	(Bits 0–7)	• Minimum Number of Bytes in a Frame

CONFIGURATION DEFAULTS

The default values of the configuration parameters are compatible with the IEEE 802.3/Ethernet Standards. RESET configures the 82586 according to the defaults shown in Table 2.

Table 2. 82586 Default Values

Preamble Length (Bytes)	=	8
Address Length (Bytes)	=	6
Broadcast Disable	=	0
CRC-16/CRC-32	=	0
No CRC Insertion	=	0
Bitstuffing/EOC	=	0
Padding	=	0
Min-Frame-Length (Bytes)	=	64
Interframe Spacing (Bits)	=	96
Slot Time (Bits)	=	512
Number of Retries	=	15
Linear Priority	=	0
Accelerated Contention Resolution	=	0
Exponential Backoff Method	=	0
Manchester/$\overline{NRZ}$	=	0
Internal CRS	=	0
CRS Filter	=	0
Internal CDT	=	0
CDT Filter	=	0
Transmit On No CRS	=	0
FIFO THRESHOLD	=	8
SRDY/$\overline{ARDY}$	=	0
Save Bad Frame	=	0
Address/Length Location	=	0
INT Loopback	=	0
EXT Loopback	=	0
Promiscuous Mode	=	0

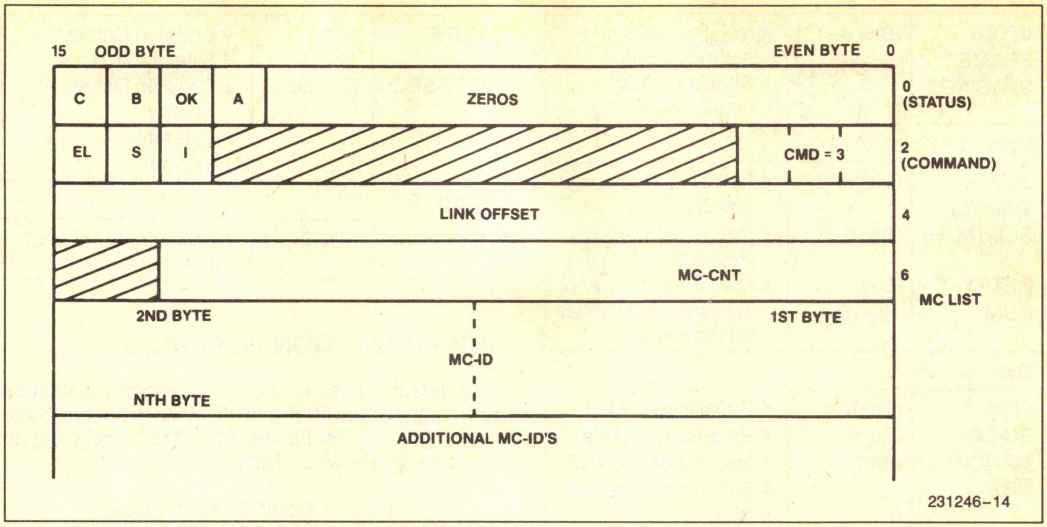


Figure 14. The MC-SETUP Command Block

MC-SETUP

This command sets up the 82586 with a set of Multicast Addresses. Subsequently, incoming frames with Destination Addresses from this set are accepted.

The MC-SETUP command includes the following fields:

STATUS word (written by 82586):

C	(Bit 15)	• Command Completed
B	(Bit 14)	• Busy Executing Command
OK	(Bit 13)	• Error Free Completion
A	(Bit 12)	• Command Aborted

COMMAND word:

EL	(Bit 15)	• End of Command List
S	(Bit 14)	• Suspend After Completion
I	(Bit 13)	• Interrupt After Completion
CMD	(Bits 0–2)	• MC-SETUP = 3

LINK OFFSET: Address of next Command Block

MC-CNT: A 14-bit field indicating the number of bytes in the MC-LIST field. MC-CNT is truncated to the nearest multiple of Address Length (in bytes). Issuing a MC-SETUP command with MC-CNT = 0 disables reception of any incoming frame with a Multicast Address.

MC-LIST: A list of Multicast Addresses to be accepted by the 82586. Note that the most significant byte of an address is followed immediately by the least significant byte of the next address. Note also that the least significant bit of each Multicast Address in the set must be a one.

The Transmit-Byte-Machine maintains a 64-bit HASH table used for checking Multicast Addresses during reception.

An incoming frame is accepted if it has a Destination Address whose least significant bit is a one, and after hashing points to a bit in the HASH table whose value is one. The hash function is selecting bits 2 to 7 of the CRC register. RESET causes the HASH table to become all zeros.

After the Transmit-Byte-Machine reads a MC-SETUP command from TX-FIFO, it clears the HASH table and reads the bytes in groups whose length is determined by the ADDRESS length. Each group is hashed using CRC logic and the bit in the HASH table to which bits 2–7 of the CRC register point is set to one. A group that is not complete has no effect on the HASH table. Transmit-Byte-Machine notifies CU after completion.

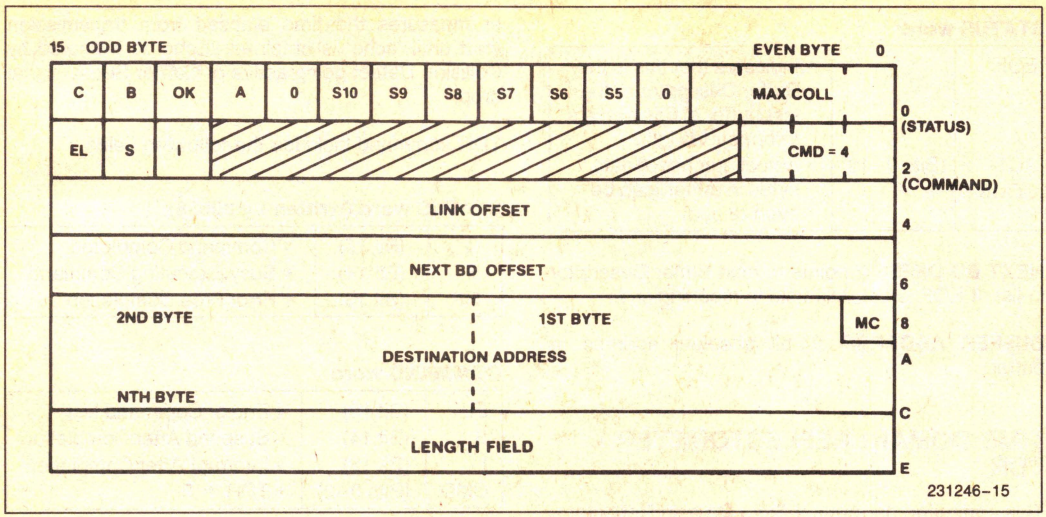


Figure 15. The Transmit Command Block

TRANSMIT

The TRANSMIT command causes transmission (and if necessary retransmission) of a frame.

TRANSMIT CB includes the following fields:

STATUS word (written by 82586):

C	(Bit 15)	• Command Completed
B	(Bit 14)	• Busy Executing Command
OK	(Bit 13)	• Error Free Completion
A	(Bit 12)	• Command Aborted
S10	(Bit 10)	• No Carrier Sense signal during transmission (between beginning of Destination Address and end of Frame Check Sequence).
S9	(Bit 9)	• Transmission unsuccessful (stopped) due to loss of Clear-to-Send signal.
S8	(Bit 8)	• Transmission unsuccessful (stopped) due to DMA underrun, (i.e. data not supplied from the sytem for transmission).
S7	(Bit 7)	• Transmission had to Defer to traffic on the link.
S6	(Bit 6)	• Heart Beat, indicates that during Interframe Spacing period after the previous transmission, a pulse was detected on the Collision Detect pin.
S5	(Bit 5)	• Transmission attempt stopped due to number of collisions exceeding the maximum number of retries.
MAX-COLL	(Bits 3–0)	• Number of Collisions experienced by this frame. S5 = 1 and MAX-COLL = 0 indicates that there were 16 collisions.

COMMAND word:

EL	(Bit 15)	• End of Command List
S	(Bit 14)	• Suspend After Completion
I	(Bit 13)	• Interrupt After Completion
CMD	(Bits 0–2)	• TRANSMIT = 4

LINK OFFSET: Address of next Command Block

TBD OFFSET: Address of list of buffers holding the information field. TBD-OFFSET = 0FFFFH indicates that there is no Information field.

DESTINATION ADDRESS: Destination Address of the frame.

LENGTH FIELD: Length field of the frame.

STATUS word:

EOF		• Indicates that this is the Buffer Descriptor of the last buffer of this frame's Information Field.
ACT-COUNT	(Bits 0–13)	• Actual number of data bytes in buffer (can be even or odd).

NEXT BD OFFSET: points to next Buffer Descriptor in list. If EOF is set, this field is meaningless.

BUFFER ADDRESS: 24-bit absolute address of buffer.

TIME DOMAIN REFLECTOMETER - TDR

This command performs a Time Domain Reflectometer test on the serial link. By performing the command, the user is able to identify shorts or opens and their location. Along with transmission of 'All Ones,' the 82586 triggers an internal timer. The timer measures the time elapsed from transmission start until 'echo' is obtained. 'Echo' is indicated by Collision Detect going active or Carrier Sense signal drop.

TDR command includes the following fields:

STATUS word (written by 82586):

C	(Bit 15)	• Command Completed
B	(Bit 14)	• Busy Executing Command
OK	(Bit 13)	• Error Free Completion

COMMAND word:

EL	(Bit 15)	• End of Command List
S	(Bit 14)	• Suspend After Completion
I	(Bit 13)	• Interrupt After Completion
CMD	(Bits 0–2)	• TDR = 5

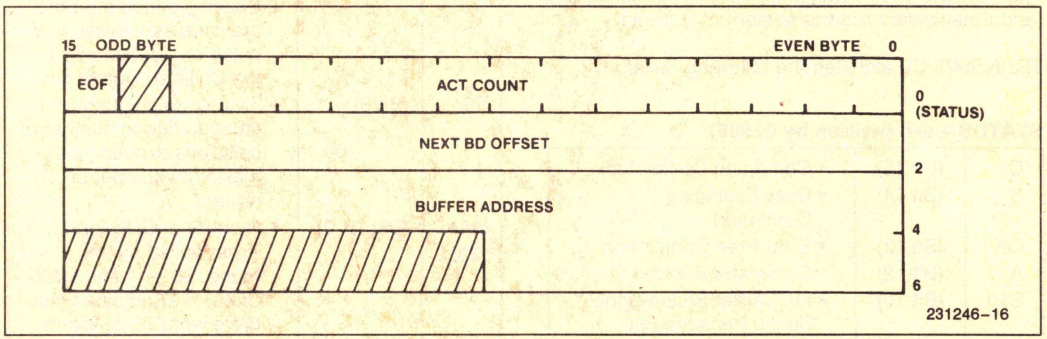


Figure 16. The Transmit Buffer Description

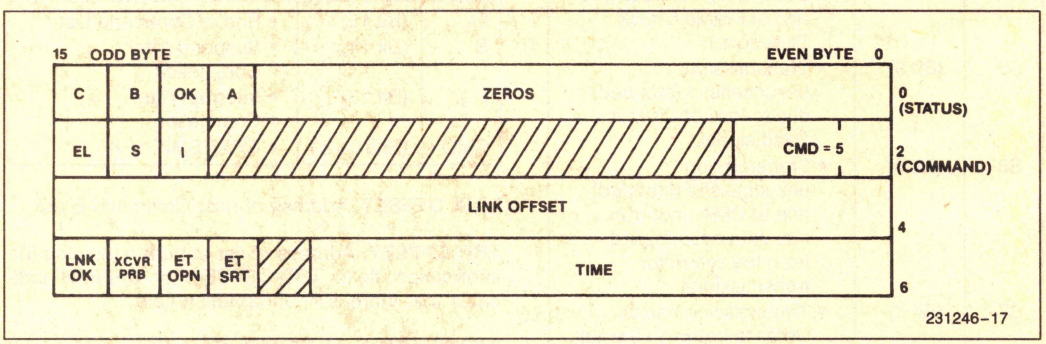


Figure 17. The TDR Command Block

LINK OFFSET: Address of next Command Block

RESULT word:

LNK-OK	(Bit 15)	• No Link Problem Identified
XCVR-PRB	(Bit 14)	• Transceiver Cable Problem identified (valid only in the case of a Transceiver that does not return Carrier Sense during transmission).
ET-OPN	(Bit 13)	• Open on the link identified (valid only in the case of a Transceiver that returns Carrier Sense during transmission).
ET-SRT	(Bit 12)	• Short on the link identified (valid only in the case of a Transceiver that returns Carrier Sense during transmission).
TIME	(Bits 0–10)	• Specifying the distance to a problem on the link (if one exists) in transmit clock cycles.

DUMP

This command causes the contents of over a hundred bytes of internal registers to be placed in memory. It is supplied as a self diagnostic tool, as well as to supply registers of interest to the user.

DUMP command includes the following fields:

STATUS word (written by 82586):

C	(Bit 15)	• Command Completed
B	(Bit 14)	• Busy Executing Command
OK	(Bit 13)	• Error Free Completion

COMMAND word:

EL	(Bit 15)	• End of Command List
S	(Bit 14)	• Suspend After Completion
I	(Bit 13)	• Interrupt After Completion
CMD	(Bits 0–2)	• DUMP = 6

LINK OFFSET: Address of next Command Block

BUFFER OFFSET: This word specifies the offset portion of the memory address which points to the top of the buffer allocated for the dumped registers contents. The length of the buffer is 170 bytes.

DUMP AREA FORMAT

Figure 18 shows the format of the DUMP area. The fields are as follows:

Bytes 00H to 0AH: These bytes correspond to the 82586 CONFIGURE command field.

Bytes 0CH to 11H: The Individual Address Register content. IARO is the Individual Address least significant byte.

Bytes 12H to 13H: Status word of last command block (only bits 0–13).

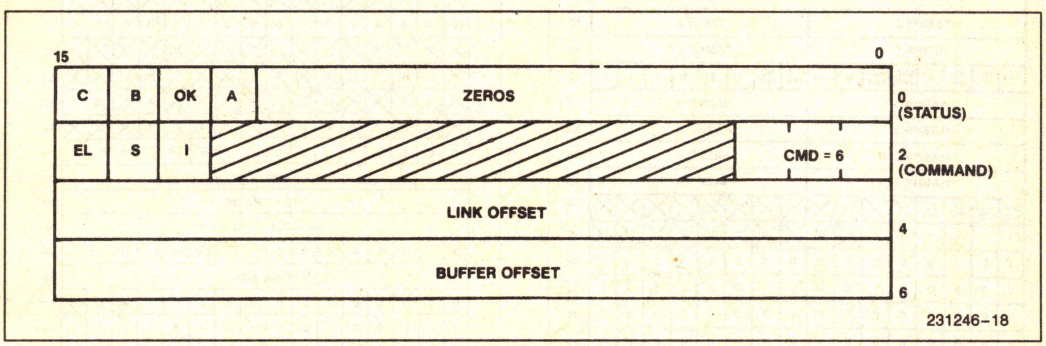


Figure 18. The DUMP Command Block

Bytes 14H to 17H: Content of the Transmit CRC generator. TXCRCRO is the least significant byte. The contents are dependent on the activity before the DUMP command:

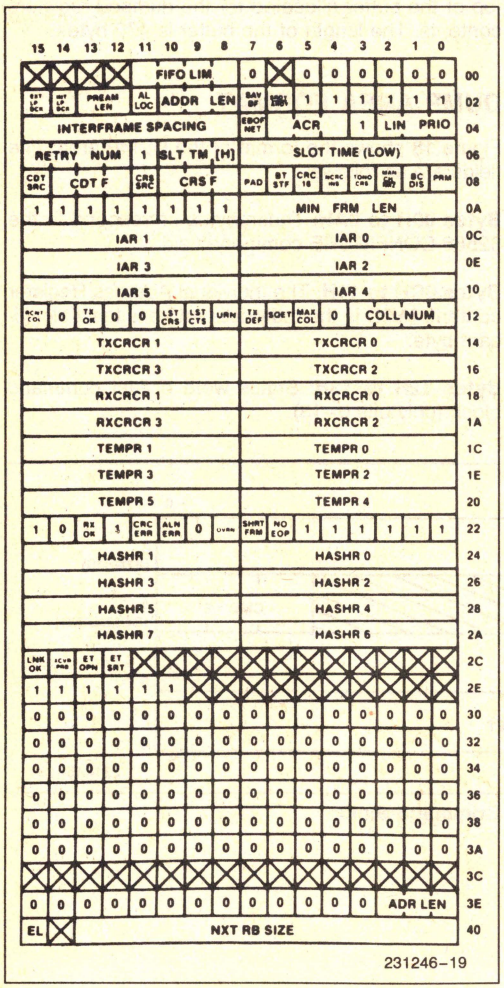
After RESET - 'All Ones.'

After successful transmission - 'All Zeros'.

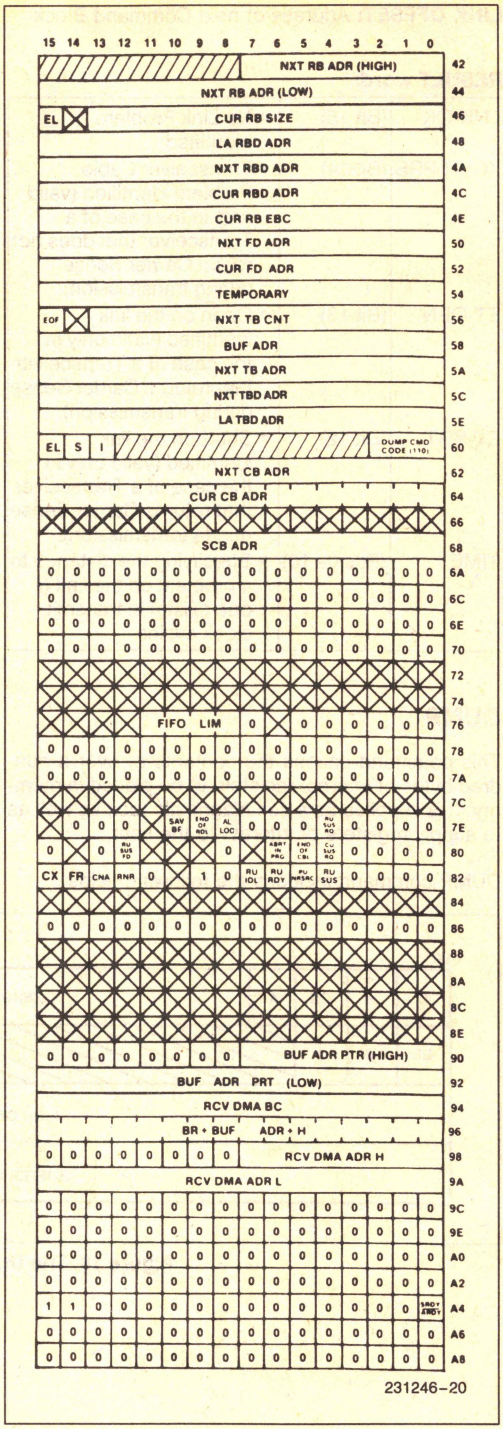
After MC-SETUP command - Generated CRC value of the last MC address, on MC-LIST.

After unsuccessful transmission, depends on where it stopped.

NOTE:
For 16-bit CRC only TXCRCRO and TXCRCR1 are valid.



231246-19



231246-20

Figure 19. The DUMP Area

Bytes 18H to 1BH: Contents of Receive CRC Checker. RXCRCRO is the least significant byte. The contents are dependent on the activity performed before the DUMP command:

After RESET - 'All Ones.'

After good frame reception—

1. For CRC-CCITT - 0ID0FH
2. For CRC-Autodin-II - C704DD7BH

After Bad Frame reception - corresponds to the received information.

After reception attempt, i.e. unsuccessful check for address match, corresponds to the CRC performed on the frame address.

NOTE:
Any frame on the serial link modifies this register contents.

Bytes 1CH to 21H: Temporary Registers.

Bytes 22H to 23H: Receive Status Register. Bits 6, 7, 8, 10, 11 and 13 assume the same meaning as corresponding bits in the Receive Frame Descriptor Status field.

Bytes 24H to 2BH: HASH TABLE.

Bytes 2CH to 2DH: Status bits of the last time TDR command that was performed.

NXT-RB-SIZE: Let N be the last buffer of the last received frame, then NXT-RB-SIZE is the number of bytes of available in the N + 1 buffer. EL - The EL bit of the Receive Buffer Descriptor.

NXT-RB-ADR: Let N be the last Receive Buffer used, then NXT-RB-ADR is the BUFFER-ADDRESS field in the N + 1 Receive-Buffer Descriptor, i.e. the pointer to the N + 1 Receive Buffer.

CUR-RB-SIZE: The number of bytes in the last buffer of the last received frame. EL - The EL bit of the last buffer in the last received frame.

LA-RBD-ADR: Look Ahead Buffer Descriptor, i.e. the pointer to N + 2 Receiver Buffer Descriptor.

NXT-RBD-ADR: Next Receive Buffer Descriptor Address. Similar to LA-RBD-ADR but points to N + 1 Receive Buffer Descriptor.

CUR-RBD-ADR: Current Receive Buffer Descriptor Address. Similar to LA-RBD-ADR, but point to Nth Receive Buffer Descriptor.

CUR-RB-EBC: Current Receive Buffer Empty Byte Count Let N be the currently used Receive Buffer. Then CUR-RB-EBC indicates the Empty part of the buffer, i.e. the ACT-COUNT of buffer N is given by the difference between its SIZE and the CUR-RB-EBC.

NXT-FD-ADR: Next Frame Descriptor Address. Define N as the last Receive Frame Descriptor with bits C = 1 and B = 0, then NXT-FD-ADR is the address of N + 2 Receive Frame Descriptor (with B = C = 0) and is equal to the LINK-ADDRESS field in N + 1 Receive Frame Descriptor.

CUR-FD-ADR: Current Frame Descriptor Address. Similar to next NXT-FD-ADR but refers to N + 1 Receive Frame Descriptor (with B = 1, C = 0).

Bytes 54H to 55H: Temporary register.

NXT-TB-CNT: Next Transmit Buffer Count. Let N be the last transmitted buffer of the TRANSMIT command executed recently, the NXT-TB-CNT is the ACT-COUNT field in the Nth Transmit Buffer Descriptor. EOF - Corresponds to the EOF bit of the Nth Transmit Buffer Descriptor. EOF = 1 indicates that the last buffer accessed by the 82586 during Transmit was the last Transmit Buffer in the data buffer chain associated with the Transmit Command.

BUF-ADR: Buffer Address. The BUF-PTR field in the DUMP-STATUS Command Block.

NXT-TB-AD-L: Next Transmit Buffer Address Low. Let N be the last Transmit Buffer in the transmit buffer chain of the TRANSMIT Command performed recently, then NXT-TB-AD-L are the two least significant bytes of the Nth buffer address.

LA-TB-ADR: Look Ahead Transmit Buffer Descriptor Address. Let N be the last Transmit Buffer in the transmit buffer chain of the TRANSMIT Command performed recently, then LA-TBD-ADR is the NEXT-BD-ADDRESS field of the Nth Buffer Descriptor.

NXT-TBD-ADR: Next Transmit Buffer Descriptor Address. Similar in function to LA-TBD-ADR but related to Transmit Buffer Descriptor N-1. Actually, it is the address of Transmit Buffer Descriptor N.

Bytes 60H, 61H: This is a copy of the 2nd word in the DUMP-STATUS command presently executing.

NXT-CB-ADR: Next Command Block Address. The LINK-ADDRESS field in the DUMP Command Block presently executing. Points to the next command.

CUR-CB-ADR: Current Command Block Address. The address of the DUMP Command Block currently executing.

SCB-ADR: Offset of the System Control Block (SCB).

Bytes 7EH, 7FH:

RU-SUS-RQ (Bit 4) - Receive Unit Suspend Request.

Bytes 80H, 81H:

CU-SUS-RQ (Bit 4) - Command Unit Suspend Request.

END-OF-CBL (Bit 5) - End of Command Block List. If "1" indicates that DUMP-STATUS is the last command in the command chain.

ABRT-IN-PROG (Bit 6) - Command Unit Abort Request.

RU-SUS-FD (Bit 12) - Receive Unit Suspend Frame Descriptor Bit. Assume N is the Receive Frame Descriptor used recently, then RU-SUS-FD is equivalent to the S bit of N + 1 Receive Frame Descriptor.

Bytes 82H, 83H:

RU-SUS (Bit 4) - Receive Unit in SUSPENDED state.

RU-NRSRC (Bit 5) - Receive Unit in NO RESOURCES state.

RU-RDY (Bit 6) - Receive Unit in READY state.

RU-IDL (Bit 7) - Receive Unit in IDLE state.

RNR (Bit 12) - RNR Interrupt in Service bit.

CNA (Bit 13) - CNA Interrupt in Service bit.

FR (Bit 14) - FR Interrupt in Service bit.

CX (Bit 15) - CX Interrupt in Service bit.

Bytes 90H to 93H:

BUF-ADR-PTR - Buffer pointer is the absolute address of the bytes following the DUMP Command block.

Bytes 94H to 95H:

RCV-DMA-BC - Receive DMA Byte Count. This field contains number of bytes to be transferred during the next Receive DMA operation. The value depends on AL-LOCation configuration bit.

1. If AL-LOCation = 0 then RCV-DMA-BC = (2 times ADDR-LEN plus 2) if the next Receive Frame Descriptor has already been fetched.
2. If AL-LOCation = 1 then it contains the size of the next Receive Buffer.

BR+BUF−PTR+96H - Sum of Base Address plus BUF−PTR field and 96H.

RCV-DMA-ADR - Receive DMA absolute Address. This is the next RCV-DMA start address. The value depends on AL-LOCation configuration bit.

1. If AL-LOCation = 0, then RCV-DMA-ADR is the Destination Address field located in the next Receive Frame Descriptor.
2. If AL-LOCation = 1, then RCV-DMA-ADR is the next Receive Data Buffer Address.

The following nomenclature has been used in the DUMP table:

0	• The 82586 writes zero in this location.
1	• The 82586 writes one in this location.
X	• The 82586 writes zero or one in this location.
///	• The 82586 copies this location from the corresponding position in the memory structure.

DIAGNOSE

The DIAGNOSE Command triggers an internal self test procedure of backoff related registers and counters.

The DIAGNOSE command includes the following:

STATUS word (written by 82586):

C	(Bit 15)	• Command Completed
B	(Bit 14)	• Busy Executing Command
OK	(Bit 13)	• Error Free Completion
FAIL	(Bit 11)	• Indicates that the Self Test Procedured Failed

COMMAND word:

EL	(Bit 15)	• End of Command List
S	(Bit 14)	• Suspend After Completion
I	(Bit 13)	• Interrupt After Completion
CMD	(Bits 0–2)	• DIAGNOSE = 7

LINK OFFSET: Address of next Command Block.

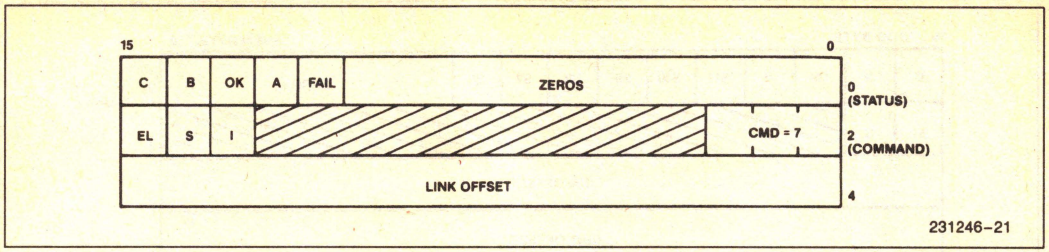


Figure 20. The DIAGNOSE Command Block

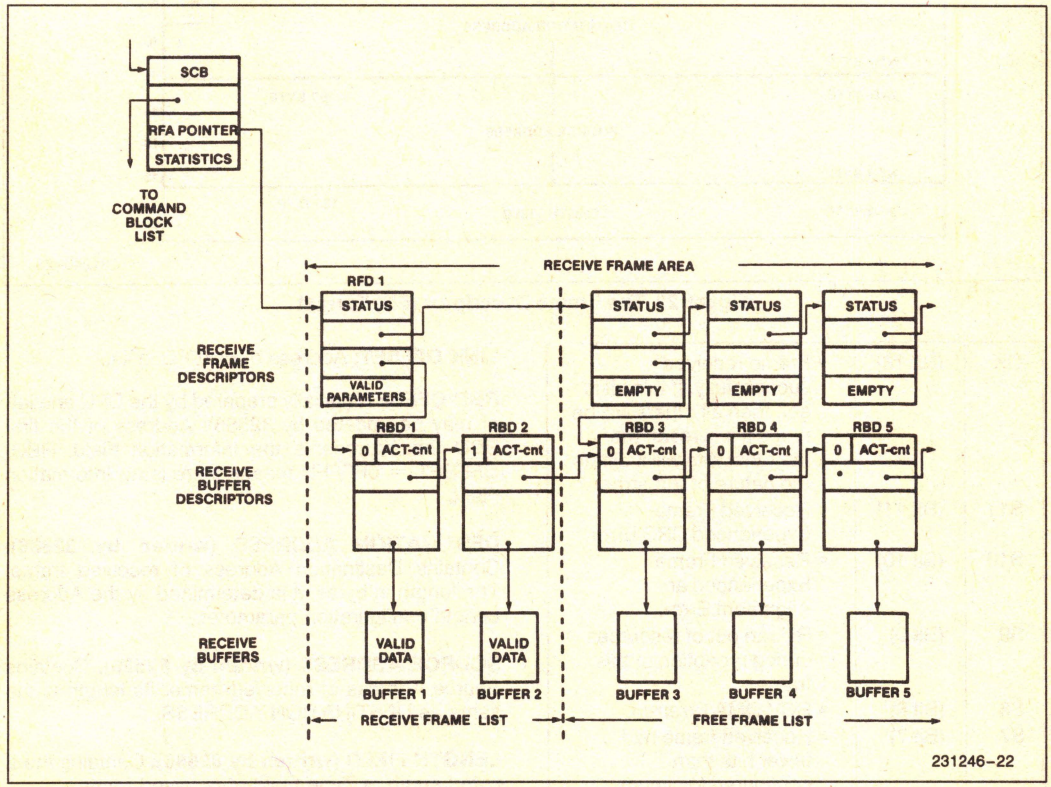


Figure 21. The Receive Frame Area

RECEIVE FRAME AREA (RFA)

The Receive Frame Area, RFA, is prepared by the host CPU, data is placed into the RFA by the 82586 as frames are received. RFA consists of a list of Receive Frame Descriptors (FD), each of which is associated with a frame. RFA-OFFSET field of SCB points to the first FD of the chain; the last FD is identified by the End-of-Listing flag (EL). See Figure 21.

FRAME DESCRIPTOR (FD) FORMAT

The FD includes the following fields:

STATUS word (set by the 82586):

C	(Bit 15)	• Completed Storing Frame.
B	(Bit 14)	• FD was Consumed by RU.

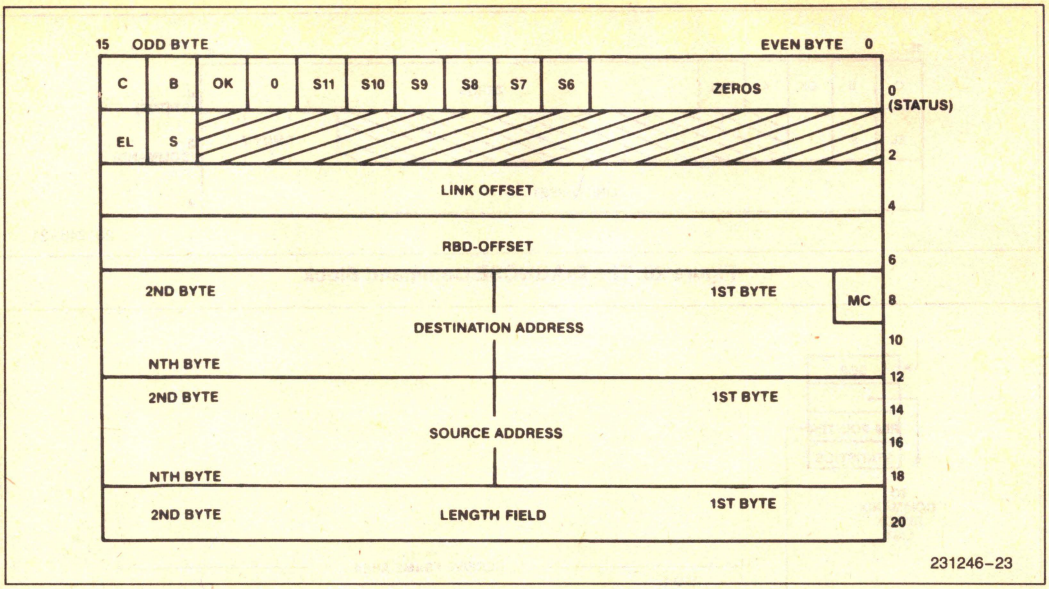


Figure 22. The Frame Descriptor (FD) Format

OK	(Bit 13)	• Frame received successfully. If this bit is set, then all others will be reset; if it is reset, then the other bits will indicate the nature of the error.
S11	(Bit 11)	• Received Frame Experienced CRC Error.
S10	(Bit 10)	• Received Frame Experienced an Alignment Error.
S9	(Bit 9)	• RU ran out of resources during reception of this frame.
S8	(Bit 8)	• RCV-DMA Overrun.
S7	(Bit 7)	• Received frame had fewer bits than configured Minimum Frame Length.
S6	(Bit 6)	• No EOF flag detected (only when configured to Bitstuffing).

COMMAND word:

EL	(Bit 15)	• Last FD in the List.
S	(Bit 14)	• RU should be suspended after receiving this frame.

LINK OFFSET: Address of next FD in list.

RBD-OFFSET: (initially prepared by the CPU and later may be updated by 82586): Address of the first RBD that represents the Information Field. RBD-OFFSET = 0FFFFH means there is no Information Field.

DESTINATION ADDRESS (written by 82586): Contains Destination Address of received frame. The length in bytes, it is determined by the Address Length configuration parameter.

SOURCE ADDRESS (written by 82586): Contains Source Address of received frame. Its length is the same as DESTINATION ADDRESS.

LENGTH FIELD (written by 82586): Contains the 2 byte Length or Type Field of received frame.

RECEIVE BUFFER DESCRIPTOR FORMAT

The Receive Buffer Descriptor (RBD) holds information about a buffer; size and location, and the means for forming a chain of RBDs, (forward pointer and end-of-frame indication).

The Buffer Descriptor contains the following fields.

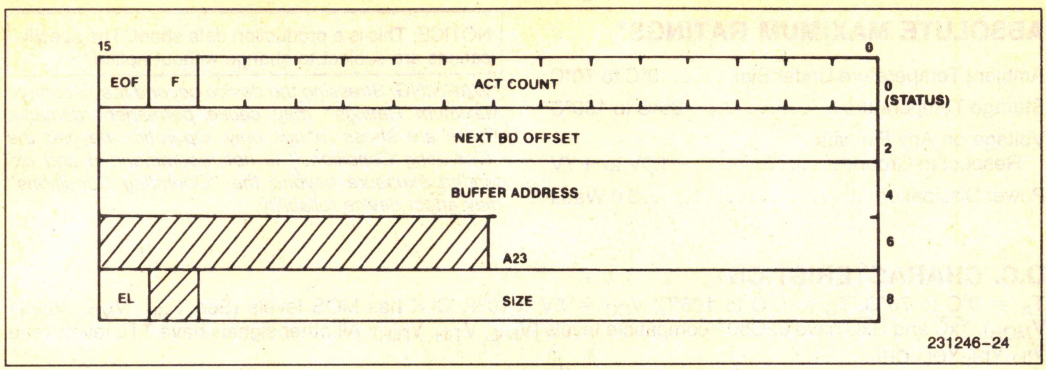


Figure 23. The Receive Buffer Descriptor (RBD) Format

STATUS word (written by the 82586).

EOF	(Bit 15)	• Last buffer in received frame.
F	(Bit 14)	• ACT COUNT field is valid.
ACT COUNT	(Bits 0–13)	• Number of bytes in the buffer that are actually occupied.

NEXT RBD OFFSET: Address of next BD in list of BD's.

BUFFER ADDRESS: 24-bit absolute address of buffer.

EL/SIZE:

EL SIZE	(BIT 15) (Bits 0–13)	• Last BD in list. • Number of bytes the buffer is capable of holding.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature.....−65°C to 150°C
Voltage on Any Pin with Respect to Ground.....−1.0V to +7V
Power Dissipation.....3.0 Watts

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, T_C = 0°C to 105°C, V_{CC} = 5V ±10%, CLK has MOS levels (See V_{MIL}, V_{MIH}, V_{MOL}, V_{MOH}). $\overline{TxC}$ and $\overline{RxC}$ have 82C501 compatible levels (V_{MIL}, V_{TIH}, V_{RIH}). All other signals have TTL levels (see V_{IL}, V_{IH}, V_{OL}, $_{OH}$).

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (TTL)	−0.5	+0.8	V	
V_{IH}	Input High Voltage (TTL)	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (TTL)		0.45	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage (TTL)	2.4		V	I_{OH} − 400 μA
V_{MIL}	Input Low Voltage (MOS)	−0.5	0.6	V	
V_{MIH}	Input High Voltage (MOS)	3.9	V_{CC} + 0.5	V	
V_{TIH}	Input High Voltage ($\overline{TxC}$)	3.3	V_{CC} + 0.5	V	
V_{RIH}	Input High Voltage ($\overline{RxC}$)	3.0	V_{CC} + 0.5	V	
V_{MOL}	Output Low Voltage (MOS)		0.45	V	I_{OL} 2.5 mA
V_{MOH}	Output High Voltage (MOS)	V_{CC} − 0.5		V	I_{OH} − 400 μA
I_{LI}	Input Leakage Current		±10	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45 \le V_{OUT} \le V_{CC}$
C_{IN}	Capacitance of Input Buffer		10	pF	FC = 1 MHz
C_{OUT}	Capacitance of Output Buffer		20	pF	FC = 1 MHz
I_{CC}	Power Supply Current		550 450	mA	T_A = 0°C T_A = 70°C

SYSTEM INTERFACE A.C. TIMING CHARACTERISTICS

T_A = 0°C to 70°C, T_C = 0°C to 105°C, V_{CC} = 5V ±10%. Figures 24 and 25 define how the measurements should be done.

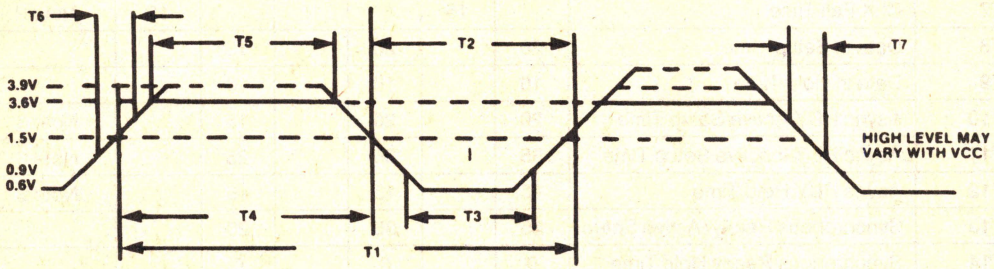
INPUT AND OUTPUT WAVEFORMS FOR A.C. TESTS



231246-25

AC Testing Inputs are Driven at 2.4V for a Logic 1 and 0.45 for a Logic 0. Timing measurements are made at 1.5V for both a Logic 1 and 0

Figure 24. TTL Input/Output Voltage Levels for Timing Measurements



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MOS I/O measurements are taken at 0.1 and 0.9 of the voltage swing

Figure 25. System Clock CMOS Input Voltage Levels for Timing Measurements

INPUT TIMING REQUIREMENTS*

Symbol	Parameter	82586-6 (6 MHz)		82586 (8 MHz)		82586-10 (10 MHz)		Comments
		Min	Max	Min	Max	Min	Max	
T1	CLK Cycle Period	166	2000	125	2000	100	200	
T2	CLK Low Time at 1.5V	73	1000	55	1000	44	1000	
T3	CLK Low Time at 0.9V			42.5	1000	42.5	1000	
T4	CLK High Time at 1.5V	73		55		44		
T5	CLK High Time at 3.6V			42.5		42.5		
T6	CLK Rise Time		15		15		12	Note 1
T7	CLK Fall Time		15		15		12	Note 2
T8	Data in Setup Time	20		20		15		
T9	Data in Hold Time	10		10		10		
T10	Async RDY Active Setup Time	20		20		15		Note 3
T11	Async RDY Inactive Setup Time	35		35		25		Note 3
T12	Async RDY Hold Time	15		15		15		Note 3
T13	Synchronous Ready/Active Setup	35		35		20		
T14	Synchronous Ready Hold Time	0		0		0		
T15	HLDA Setup Time	20		20		20		Note 3
T16	HLDA Hold Time	10		10		5		Note 3
T17	Reset Setup Time	20		20		20		Note 3
T18	Reset Hold Time	10		10		10		Note 3
T19	CA Pulse Width	1 T1		1 T1		1 T1		
T20	CA Setup Time	20		20		20		Note 3
T21	CA Hold Time	10		10		10		Note 3

OUTPUT TIMINGS**

Symbol	Parameter	Min	Max	Min	Max	Min	Max	Comments
T22	DT/R Valid Delay	0	60	0	60	0	44	
T23	$\overline{WR}$, $\overline{DEN}$ Active Delay	0	70	0	70	0	56	
T24	$\overline{WR}$, $\overline{DEN}$ Inactive Delay	10	65	10	65	10	45	
T25	Int. Active Delay	0	85	0	85	0	70	Note 4
T26	Int. Inactive Delay	0	85	0	85	0	70	Note 4
T27	Hold Active Delay	0	85	0	85	0	70	Note 4
T28	Hold Inactive Delay	0	85	0	85	0	70	Note 4
T29	Address Valid Delay	0	55	0	55	0	50	
T30	Address Float Delay	0	50	0	50	12	50	
T31	Data Valid Delay	0	55	0	55	0	50	Note 7
T32	Data Hold Time	0		0		0		
T33	Status Active Delay	10	60	10	60	10	45	

OUTPUT TIMINGS** (Continued)

Symbol	Parameter	82582-6 (6 MHz)		82586 (8 MHz)		82586-10 (10 MHz)		Comments
		Min	Max	Min	Max	Min	Max	
T34	Status Inactive Delay	10	70	10	70	10	50	Note 8
T35	ALE Active Delay	0	45	0	45	0	35	Note 5
T36	ALE Inactive Delay	0	45	0	45	0	37	Note 5
T37	ALE Width	T2–10		T2–10		T2–10		Note 5
T38	Address Valid to ALE Low	T2–40		T2–30		T2–25		
T39	Address Hold to ALE Inactive	T4–10		T4–10		T4–10		
T40	$\overline{RD}$ Active Delay	10	95	10	95	10	95	
T41	$\overline{RD}$ Inactive Delay	10	70	10	70	10	70	
T42	$\overline{RD}$ Width	2T1–50		2T1–50		2T1–46		
T43	Address Float to $\overline{RD}$ Active	10		10		0		
T44	$\overline{RD}$ Inactive to Address Active	T1–40		T1–40		T1–34		
T45	$\overline{WR}$ Width	2T1–40		2T1–40		2T1–34		
T46	Data Hold After $\overline{WR}$	T2–25		T2–25		T2–25		
T47	Control Inactive After Reset	0	60	0	60	0	60	Note 6

*All units are in ns.
**CL on all outputs is 20–200 pF unless otherwise specified.

NOTES:
1. 1.0V to 3.5V
2. 3.5V to 1.0V
3. To guarantee recognition at next clock
4. CL = 50 pF
5. CL = 100 pF
6. Affects:
   MIN MODE: $\overline{RD}$, $\overline{WR}$, DT/$\overline{R}$, $\overline{DEN}$
   MAX MODE: $\overline{S0}$, $\overline{S1}$
7. High address lines (A16–A24, BHE) become valid one clock before T1 only on first memory cycle after the 82586 acquired the bus.
8. $\overline{S1}$, S0 go inactive just prior to T4.

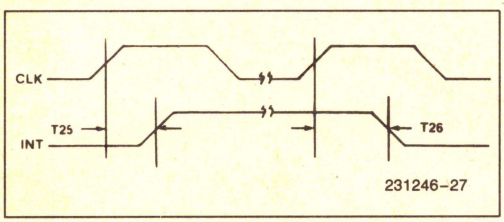


Figure 26. INT Output Timing

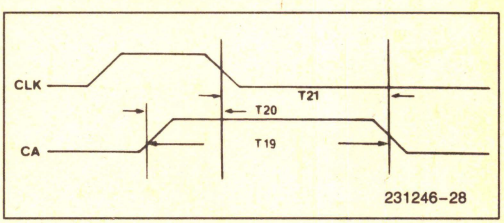


Figure 27. CA Input Timing

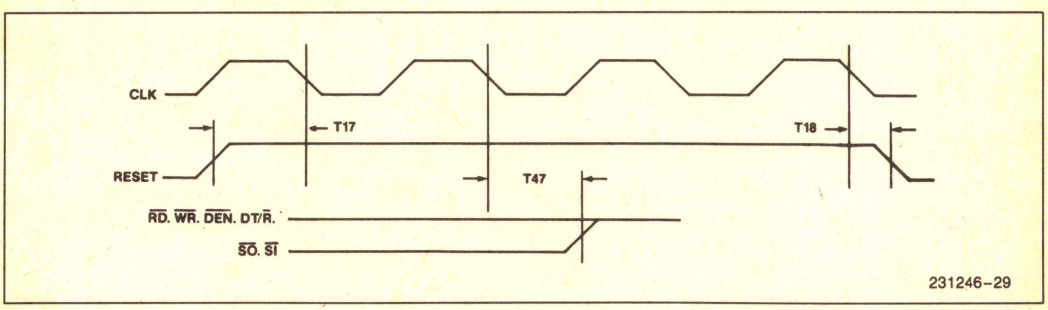


Figure 28. RESET Timing

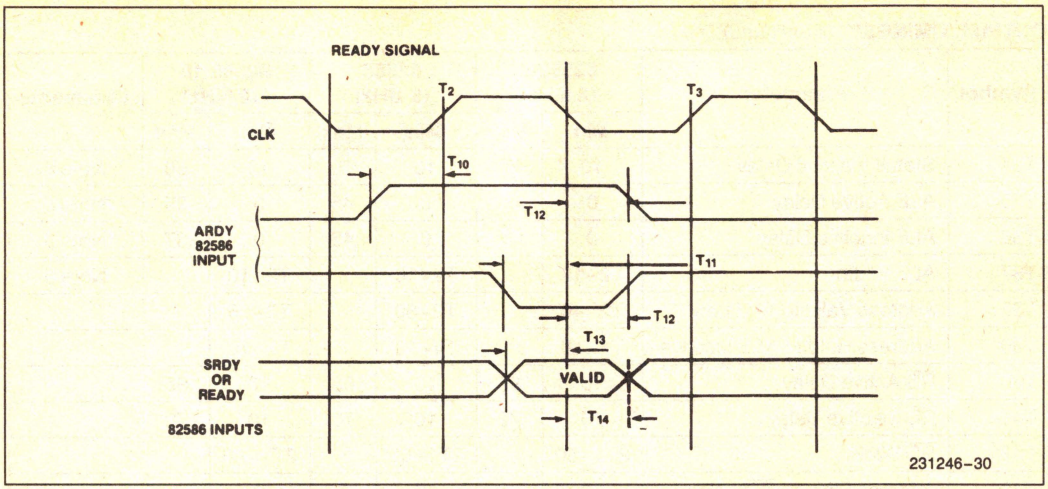


Figure 29. ARDY and SRDY Timings Relative to CLK

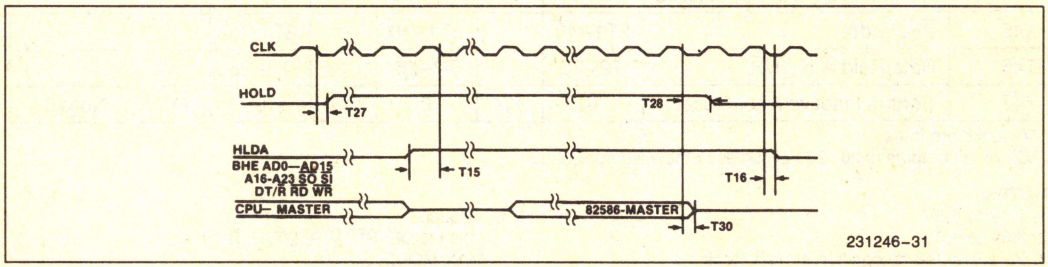


Figure 30. HOLD/HLDA Timing Relative to CLK

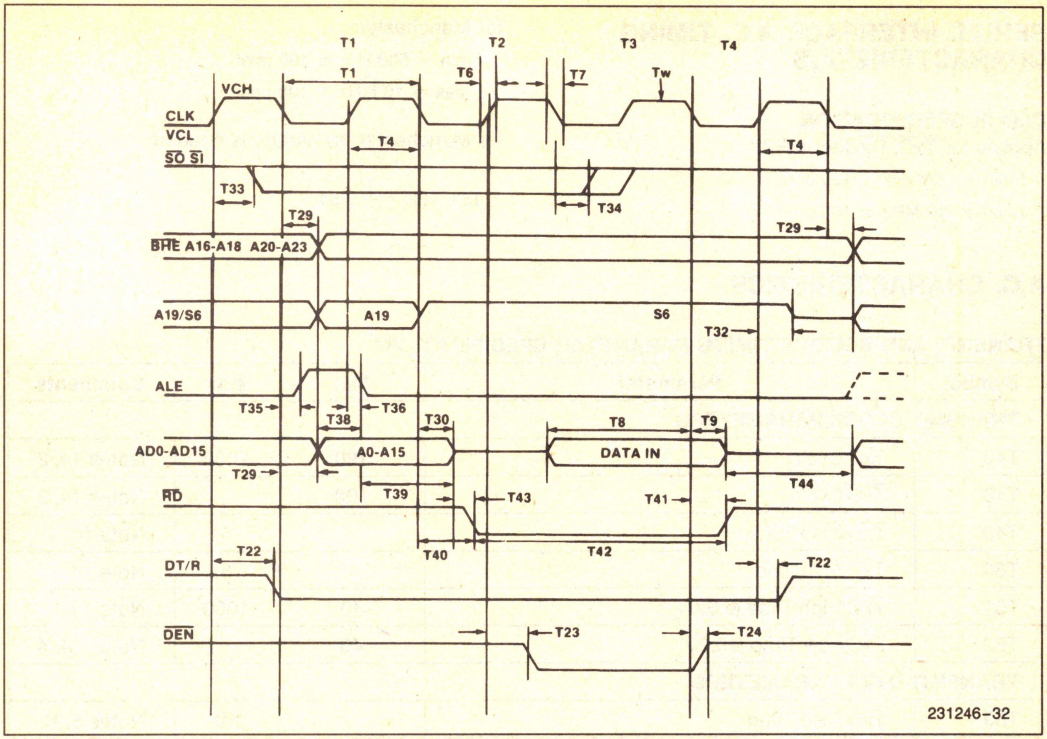


Figure 31. Read Cycle Timing

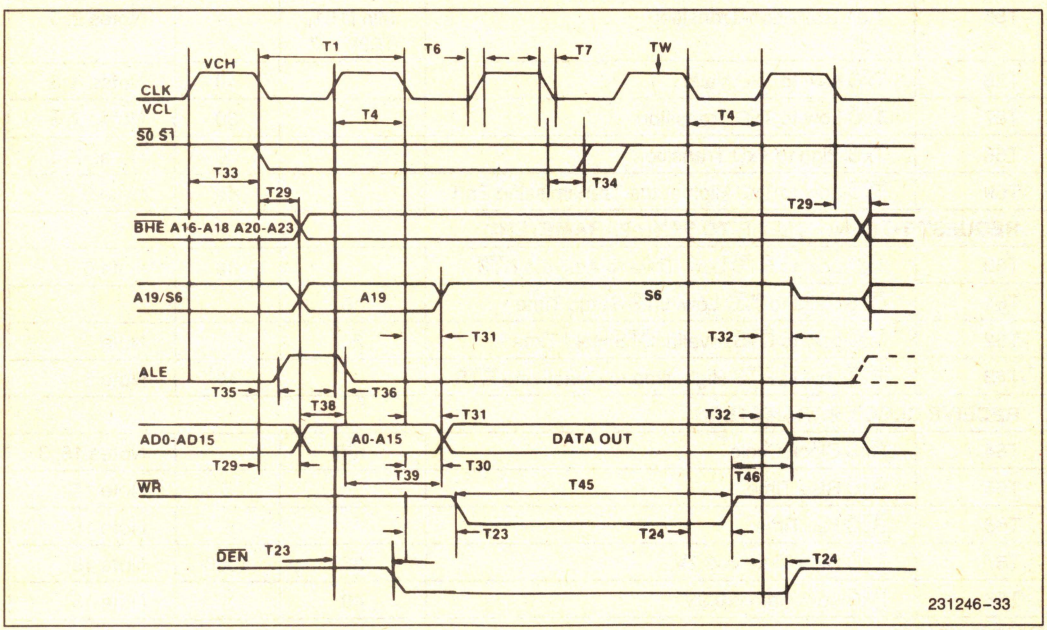


Figure 32. Write Cycle Timing

SERIAL INTERFACE A.C. TIMING CHARACTERISTICS

CLOCK SPECIFICATION

Applies for $\overline{TxC}$, $\overline{RxC}$ for NRZ:

f min = 100 kHz ± 100 ppm

f max = 10 MHz ± 100 ppm

for Manchester:

f min = 500 kHz ± 100 ppm

f max = 10 MHz ± 100 ppm

for Manchester, symmetry is needed:

$$T51, T52 = \frac{1}{2f} \pm 5\%$$

A.C. CHARACTERISTICS

TRANSMIT AND RECEIVE TIMING PARAMETER SPECIFICATION*

Symbol	Parameter	Min	Max	Comments
TRANSMIT CLOCK PARAMETERS				
T48	$\overline{TxC}$ Cycle	100	1000	Notes 14, 2
T48	$\overline{TxC}$ Cycle	100		Notes 14, 3
T49	$\overline{TxC}$ Rise Time		5	Note 14
T50	$\overline{TxC}$ Fall Time		5	Note 14
T51	$\overline{TxC}$ High Time @ 3.0V	40	1000	Note 14
T52	$\overline{TxC}$ Low Time @0.9V	40		Notes 14, 4
TRANSMIT DATA PARAMETERS				
T53	TxD Rise Time		10	Notes 5, 13
T54	TxD Fall Time		10	Notes 5, 13
T55	TxD Transition-Transition	Min (T51, T52) − 7		Notes 2, 5
T56	$\overline{TxC}$ Low to TxD Valid		40	Notes 3, 5
T57	$\overline{TxC}$ Low to TxD Transition		30	Notes 2, 5
T58	$\overline{TxC}$ High to TxD Transition		30	Notes 2, 5
T59	$\overline{TxC}$ Low to TxD High at the Transmission End		40	Note 5
REQUEST TO SEND/CLEAR TO SEND PARAMETERS				
T60	$\overline{TxC}$ Low to $\overline{RTS}$ Low. Time to Activate $\overline{RTS}$		40	Note 6
T61	$\overline{CTS}$ Valid to $\overline{TxC}$ Low. $\overline{CTS}$ Setup Time	45		
T62	$\overline{TxC}$ Low to $\overline{CTS}$ Invalid. $\overline{CTS}$ Hold Time	20		Note 7
T63	$\overline{TxC}$ Low to $\overline{RTS}$ High, time to Deactivate $\overline{RTS}$		40	Note 6
RECEIVE CLOCK PARAMETERS				
T64	$\overline{RxC}$ Clock Cycle	100		Notes 15, 3
T65	$\overline{RxC}$ Rise Time		5	Note 15
T66	$\overline{RxC}$ Fall Time		5	Note 15
T67	$\overline{RxC}$ High Time @ 2.7V	36	1000	Note 15
T68	$\overline{RxC}$ Low Time @0.9V	40		Note 15

*All units are in ns.

A.C. CHARACTERISTICS (Continued)

TRANSMIT AND RECEIVE TIMING PARAMETER SPECIFICATION* (Continued)

Symbol	Parameter	Min	Max	Comments
RECEIVE DATA PARAMETERS				
T69	RxD Setup Time	30		Note 1
T70	RxD Hold Time	30		Note 1
T71	RxD Rise Time		10	Note 1
T72	RxD Fall Time		10	Note 1
CARRIER SENSE/COLLISION DETECT PARAMETERS				
T73	$\overline{CDT}$ Valid to $\overline{TxC}$ High Ext. Collision Detect Setup Time	30		Note 12
T74	$\overline{TxC}$ High to $\overline{CDT}$ Inactive. $\overline{CDT}$ Hold Time	20		Note 12
T75	$\overline{CDT}$ Low to Jamming Start			Note 8
T76	$\overline{CRS}$ Valid to $\overline{TxC}$ High Ext. Carrier Sense Setup Time	30		Note 12
T77	$\overline{TxC}$ High to $\overline{CRS}$ Inactive. $\overline{CRS}$ Hold Time	20		Note 12
T78	$\overline{CRS}$ Low to Jamming Start			Note 9
T79	Jamming Period			Note 10
T80	$\overline{CRS}$ Inactive Setup Time to $\overline{RxC}$ High End of Receive Frame	60		
T81	$\overline{CRS}$ Active Hold Time from $\overline{RxC}$ High	3		
INTERFRAME SPACING PARAMETER				
T82	Inter Frame Delay			Note 11

*All units are in ns.

NOTES:
1. TTL levels
2. Manchester only
3. NRZ only
4. Manchester requires 50% duty cycle
5. 1 TTL load + 50 pF
6. 1 TTL load + 100 pF
7. Abnormal end of transmission. $\overline{CTS}$ expires before $\overline{RTS}$
8. Programmable value:
   T75 = NCDF × T48 + (12.5 to 23.5) × T48 if collision occurs after preamble
   NCDF—The collision detection filter configuration value
9. Programmable value:
   T78 = NCSF × T48 + (12.5 to 23.5) × T48
   NCSF—The carrier sense filter configuration value
   TBD is a function of internal/external carrier sense bit
10. T79 = 32 × T48
11. Programmable value:
    T82 = NIFS × T48
    NIFS—the IFS configuration value
*12. To guarantee recognition on the next clock
13. Applies to TTL levels
14. 82C501 compatible levels, see Figure 34
15. 82C501 compatible levels, see Figure 35

A.C. TIMING CHARACTERISTICS

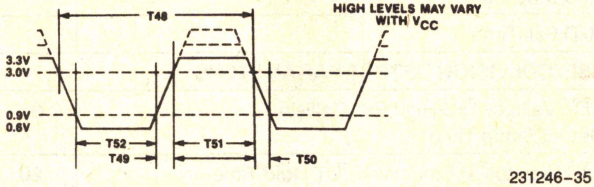
Input and Output Waveforms for AC Tests



231246-34

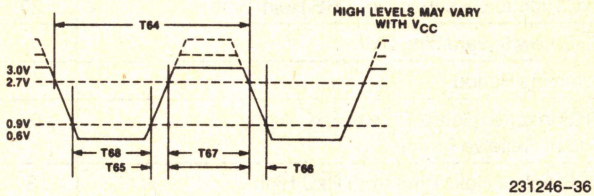
AC testing inputs are driven at 2.4V for a Logic 1 and 0.45 for a Logic 0. Timing measurements are made at 1.5V for both a Logic 1 and 0.

Figure 33. TTL Input/Output Voltage Levels for Timing Measurements



231246-35

Figure 34. $\overline{TxC}$ Input Voltage Levels for Timing Measurements



231246-36

Figure 35. $\overline{RxC}$ Input Voltage Levels for Timing Measurements

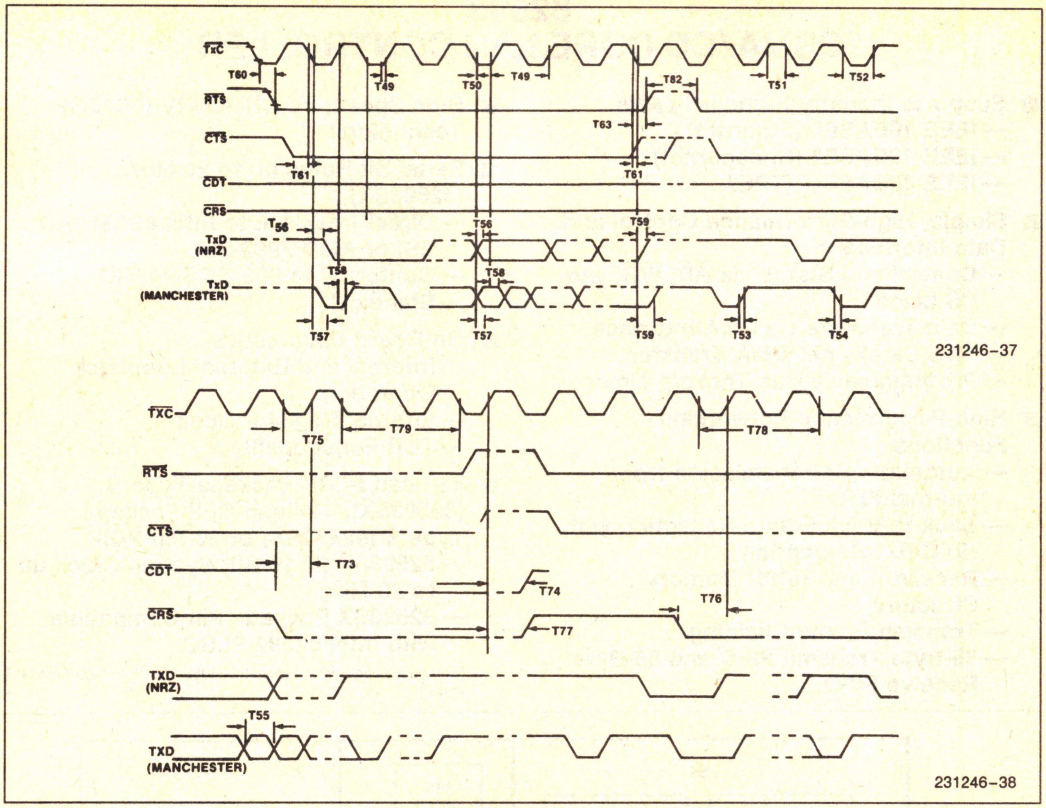


Figure 36. Transmit and Control and Data Timing

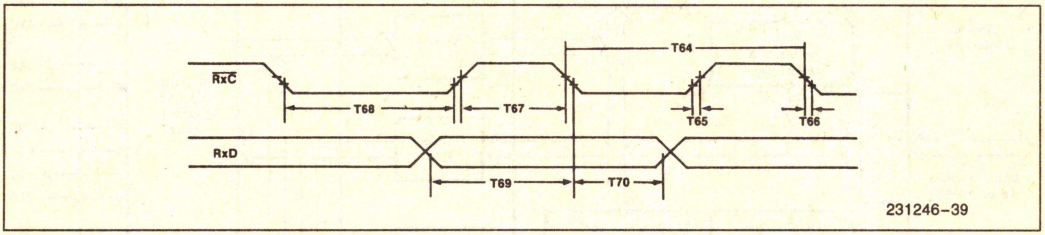


Figure 37. RxD Timing Relative to $\overline{\text{RxC}}$

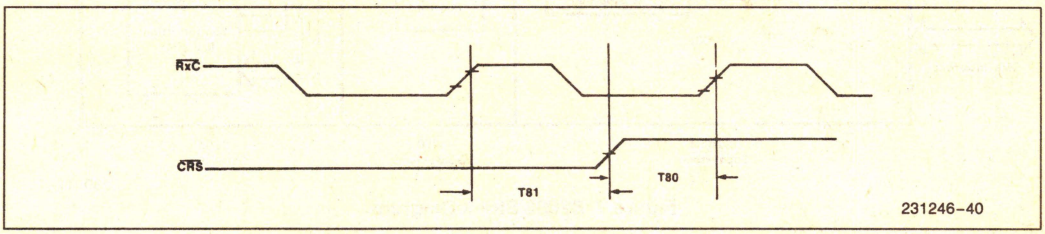


Figure 38. $\overline{\text{CRS}}$ Timing Relative to $\overline{\text{RxC}}$

82593
CSMA/CD CORE LAN CONTROLLER

- **Supports Industry Standard LANs**
  - **— IEEE 10BASE5 (Ethernet*)**
  - **— IEEE 10BASE2 (Cheapernet)**
  - **— IEEE 10BASE-T (TPE)**
- **Simple, High-Performance Control and Data Interface**
  - **— Control and Status via $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ Lines**
  - **— Data Transfers via DMA Interface**
  - **— Two Clocks per DMA Transfer**
  - **— Programmable Bus Throttle Timer**
- **High-Performance Networking Functions**
  - **— Automatic Retransmission from Internal FIFO**
  - **— Back-to-Back Frame Reception with No CPU Intervention**
  - **— Receive Ring Buffer Memory Structure**
  - **— Transmit Frame Chaining**
  - **— 96-Byte Transmit FIFO and 96-Byte Receive FIFO**
- **High Speed, 5V CHMOS IV (P648.8) Technology**
- **Serial Bit Rates up to 20 Mb/s (82593SX)**
  - **— Direct Interface to Intel 82C501AD ESI or AMD 7992 SIA**
  - **— Conforms to 802.3 CSMA/CD Standard**
- **On-Board Diagnostics**
  - **— Internal and External Loopback Operation**
  - **— Internal Register Dump**
  - **— TDR Functionality**
- **44-Lead PLCC Package Type N (82593SX), 44-Lead QFP Package Type S (82593SX) or 28-Pin PDIP**
  - **— 82593SX (8/16-Bit) System Clock up to 20 MHz**
  - **— 82593SX Package Pin Compatible with Intel 82592 PLCC**

(See Packaging Spec., Order No. 240800-001 Package Type N, S and P)

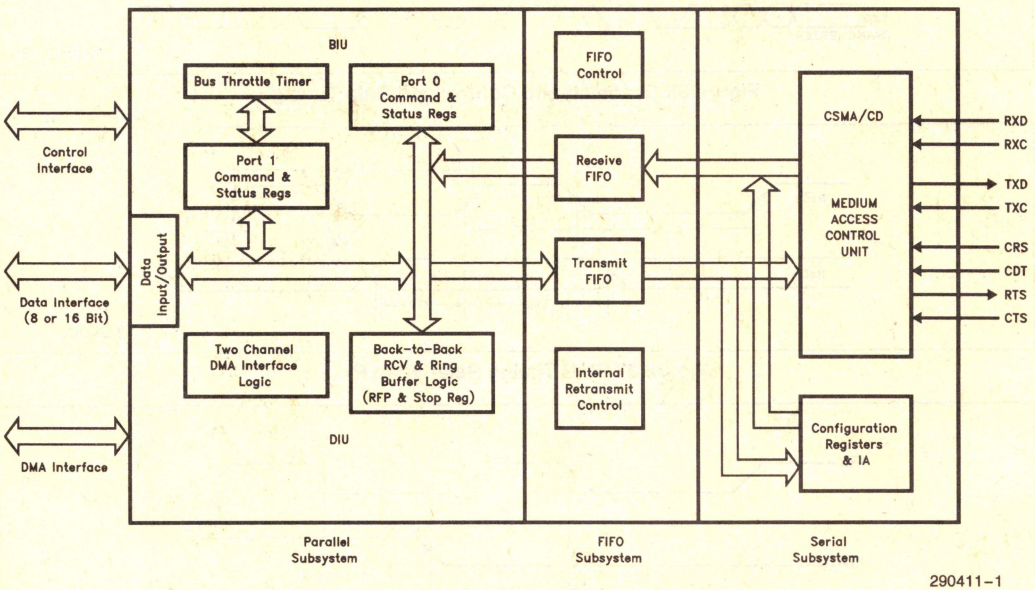


Figure 1. 82593 Block Diagram

*Ethernet is a registered trademark of Xerox Corporation.

October 1992
Order Number: 290411-004

82593
CSMA/CD Core LAN Controller

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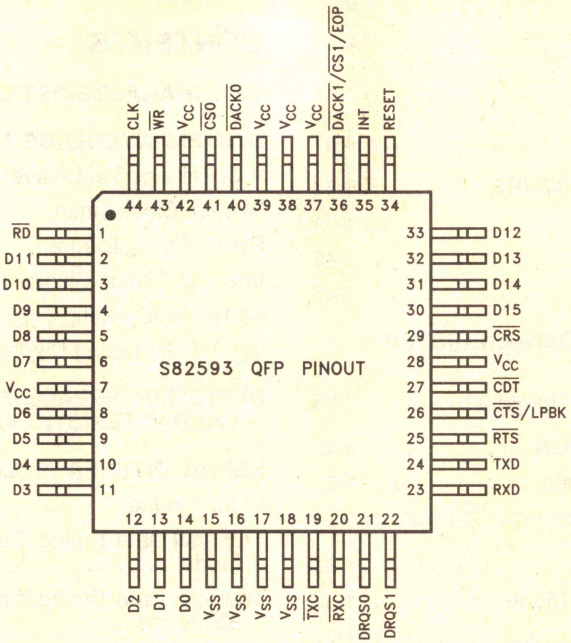
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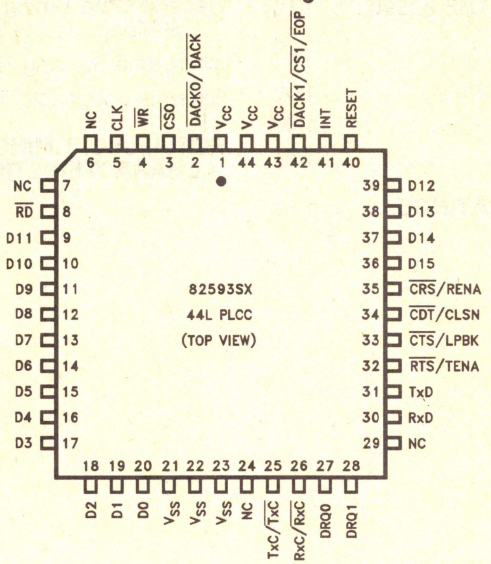
82593 PIN CONFIGURATION

S82593 Pin Configuration



290411-36

N82593SX Pin Configuration



290411-2

INTRODUCTION

The 82593 is a new generation CMOS Local Area Network controller designed for cost sensitive applications. It allows for maximum flexibility in designing and creating differentiated solutions. The 82593 features a simple, high-performance system interface which allows it to function as a CSMA/CD core for custom LAN designs. Designers can determine the performance and complexity of their solution based on the design of the logic interfaced to the 82593. This allows OEMs to develop proprietary LAN solutions that protect both their hardware and software investment into their solution. The 82593 is optimized to support IEEE 802.3 protocols such as Ethernet*, Cheapernet, and Twisted Pair Ethernet.

The 82593 contains a number of high-performance networking features that offload time-critical tasks from the CPU. The 82593 performs automatic retransmission upon collision by accessing the data for retransmission from within its 96-byte-deep transmit FIFO. This requires no intervention by the CPU as well as no need to reset the transmit DMA channel. For frame reception, the 82593, along with industry standard DMA controllers (e.g., 8237, 82380/370, etc.) or buses (ISA, EISA, etc.), implements a recyclable ring buffer structure. This structure allows reception of back-to-back receive frames without the need for CPU processing of each frame. These features also allow the 82593 to operate in embedded control applications when interfaced to embedded processors such as the Intel 80C186 and 80C188.

The 82593 is fully compatible with the IEEE 802.3 standard. When used with the Intel 82C501AD ESI it provides a complete CMOS Ethernet solution. When used with the Intel 82C501AD and 82506TB, or 82503 it provides a complete CMOS Twisted Pair Ethernet (TPE) solution.

The 82593 is compatible with the 82590 and 82592 LAN Controllers (*) operating in High Speed mode (Mode 1). The 82593SX is packaged in a 28-pin PDIP package, and is the 8-bit version of this device. The 82593SX comes in a 44-lead PLCC package, and in a 44-lead QFP package, both can be configured to have an 8- or 16-bit data bus. The 82593SX is pin compatible with the 82590. It runs at speeds up to 16 MHz for both the parallel and serial subsystems. The 82593SX in PLCC package is pin compatible with the 82592 PLCC package, with both the parallel and serial interface running at speeds up to 20 MHz. The 82593 is fabricated with Intel's reliable CHMOS IV technology.

*In this document, the 82590 and 82592 are generically referred to as the 82590 unless otherwise specified.

PIN DESCRIPTIONS

Table 1. Pin Description

Symbol	Pin No. 82593SX PLCC	Pin No. 82593SX QFP	Type	Name and Function
D15	36	30	I/O	**DATA BUS:** The Data Bus lines are bidirectional, three-state lines connected to the CPU's Data Bus for transfers of data, commands, status, and parameters. The 82593SX has an 8- or 16-bit data bus.
D14	37	31		
D13	38	32		
D12	39	33		
D11	9	2		
D10	10	3		
D9	11	4		
D8	12	5		
D7	13	6		
D6	14	8		
D5	15	9		
D4	16	10		
D3	17	11		
D2	18	12		
D1	19	13		
D0	20	14		

Table 1. Pin Description (Continued)

Symbol	Pin No. 82593SX PLCC	Pin No. 82593SX QFP	Type	Name and Function
$\overline{RD}$	8	1	I	**READ:** Together with $\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$, or $\overline{DACK1}$, Read controls data or status transfers out of the 82593.
$\overline{WR}$	4	43	I	**WRITE:** Together with $\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$, or $\overline{DACK1}$, Write controls data or command transfers into the 82593.
$\overline{CS0}$	3	41	I	**CHIP SELECT (PORT 0):** When LOW, the 82593 is selected by the CPU for command or status transfer through PORT 0.
RESET	40	34	I	**RESET:** A HIGH signal on this pin causes the 82593 to terminate current activity. This signal is internally synchronized and must be held HIGH for at least four Clock (CLK) cycles. The system should allow a minimum of 50 μs after the delta between V_{CC} and V_{SS} has reached at least 2.4V and CLK has reached minimum V_{IL}/V_{IH} levels.
INT	41	35	O	**INTERRUPT:** A HIGH signal on this pin notifies the CPU that the 82593 is requesting an interrupt.
DRQ0	27	21	O	**DMA REQUEST (CHANNEL 0):** This pin is used by the 82593 to request DMA transfers. DRQ0 remains HIGH as long as the 82593 requires DMA transfers. Burst transfers are thus possible. When the 82593 is programmed for Continuous Mode with TCI signaling the 82593 notifies the DMA controller of the status of transmission or reception, using this pin together with $\overline{EOP}$.
DRQ1	28	22	O	**DMA REQUEST (CHANNEL 1):** This pin is used by the 82593 to request DMA transfer. DRQ1 remains HIGH as long as the 82593 requires DMA transfers. Burst transfers are thus possible. When the 82593 is programmed for Continuous Mode with TCI signaling the 82593 notifies the DMA controller of the status of transmission or reception, using this pin together with $\overline{EOP}$.
$\overline{DACK0}$/ $\overline{DACK}$	2	40	I	**DMA ACKNOWLEDGE (CHANNEL 0):** When LOW, this input signal from the DMA controller notifies the 82593 that the requested DMA cycle is in progress. This signal acts similarly to Chip Select for data and parameter transfers, using DMA channel 0. **DMA ACKNOWLEDGE (CHANNELS 0 AND 1):** When the $\overline{DACK1}/\overline{CS1}/\overline{EOP}$ pin is programmed to $\overline{CS1}/\overline{EOP}$, this pin provides a DMA acknowledge for both channels 0 and 1. Two DMA acknowledge signals from the DMA controller, $\overline{DACK0}$ and $\overline{DACK1}$, must be externally ANDed in this mode of operation.

Table 1. Pin Description (Continued)

Symbol	Pin No. 82593SX PLCC	Pin No. 82593SX QFP	Type	Name and Function
$\overline{\text{DACK1}}$ $\overline{\text{CS1}}/\overline{\text{EOP}}$	42	36	I	This is a multifunction, bidirectional pin which can be programmed to $\overline{\text{DACK1}}$ or $\overline{\text{CS1}}/\overline{\text{EOP}}$ during configuration. When it is configured for $\overline{\text{EOP}}$, it provides an open-drain output. **DMA ACKNOWLEDGE (CHANNEL 1):** When LOW, this input signal from the DMA controller notifies the 82593 that the requested DMA cycle is in progress. This signal acts similarly to Chip Select for data and parameter transfers, using DMA channel 1.
			I/O	**CHIP SELECT (PORT 1):** When LOW, the 82593 is selected by the CPU for command or status transfer through PORT 1. **END OF PROCESS:** A LOW output signal requests the DMA controller to terminate the active DMA service.
CLK	5	44	I	**CLOCK:** A TTL-compatible clock input to this pin provides the timing for the 82593 parallel subsystem.
$\overline{\text{TXC}}$/ TXC	25	19	I	**TRANSMIT CLOCK:** This input provides the fundamental timing for the serial subsystem. This clock is also used to transmit data synchronously on the TXD pin. The polarity of this pin is programmable. Data is transferred to the TXD pin on the High to Low transition of the Transmit Clock.
$\overline{\text{RXC}}$/ RXC	26	20	I	**RECEIVE CLOCK:** This input used to synchronously sample data on the RXD pin. The polarity of this pin is programmable. The state of the RXD pin is sampled on the High to Low transition of the Receive Clock.
$\overline{\text{CRS}}$/ RENA	35	29	I	**CARRIER SENSE/RECEIVE ENABLE:** This pin is used to notify the 82593 that the serial link is active. The polarity and timings of this input are programmable.
$\overline{\text{CDT}}$/ CLSN	34	27	I	**COLLISION DETECT:** This input notifies the 82593 that a collision has occurred. The polarity and timings of this input are programmable.
RxD	30	23	I	**RECEIVE DATA:** This pin receives serial data. It must be HIGH when not receiving.
TxD	31	24	O	**TRANSMIT DATA:** This pin transmits data to the serial link. It is HIGH when not transmitting.
$\overline{\text{RTS}}$/ TENA	32	25	O	**REQUEST TO SEND/TRANSMIT ENABLE:** When this signal is active, the 82593 notifies the serial interface device that it has data to transmit. The polarity of this pin is programmable. It is tri-state on power-up until the first configuration is performed. A pull-up or pull-down resistor should be connected to this pin to guarantee it is at an inactive level prior to the initial configuration.

Table 1. Pin Description (Continued)

Symbol	Pin No. 82593SX PLCC	Pin No. 82593SX QFP	Type	Name and Function
$\overline{CTS}$/ LPBK	33	26	I/O	This pin's polarity is programmable. When CTS is active high, $\overline{LPBK}$ is active low. Conversely, when $\overline{CTS}$ is active low, LPBK is active high.
CTS/ $\overline{LPBK}$				**CLEAR TO SEND:** This signal enables the 82593 transmitter. Deasserting this signal stops the transmission.
				LOOPBACK: This pin, in conjunction with a pull-down or pull-up resistor, can be programmed to provide a loopback signal to the serial interface device.
V_{CC}	1 43 44	7, 28, 37, 38, 39, 42		**POWER:** +5V ±10%.
V_{SS}	21 22 23	15, 16, 17, 18		**GROUND:** 0V.

INTERNAL ARCHITECTURE

The 82593 consists of a parallel subsystem, a serial subsystem, and a FIFO subsystem (see Figure 1).

PARALLEL SUBSYSTEM

The parallel subsystem consists of a bus interface unit (BIU), through which commands can be written and status registers can be read by the CPU, a DMA interface unit (DIU) through which configuration parameters and data can be written and read from memory and a 10-bit bus throttle timer.

The BIU is composed of two I/O ports, Port 0 through which time-critical tasks and configurations are executed and Port 1, which is used for auxiliary commands. The 8-bit Port 0 command and status registers are interfaced to the CPU via the data lines D0–D7. Operation and initialization commands such as TRANSMIT, RCV-ENABLE, and CONFIGURE are issued to the 82593 via the Port 0 Command Register. The resultant status of these commands, as well as the states (Idle, Active, Ready, etc.) of the 82593's RCV and EXEC units are contained in the Port 0 Status Registers.

Port 1 command and status registers are also 8 bits wide. The Port 1 Command Register is used for additional commands such as POWER-DOWN and STOP-REG-UPDATE. The Port 1 status registers, Status Bank 1, contain the values of the Bus Throttle Timer, the RCV Stop Register and the Power Down and Hi-Impedance status.

The DIU is composed of two separate DMA channels, Channel 0 and Channel 1. The DMA channels are 8 bits wide for the 82593SX, and 8 or 16 bits wide for the 82593SX depending on its configuration. When the 82593SX is reset, the DMA channels are initialized for an 8-bit data path. The CPU can then configure the 82593SX for a 16-bit data path if desired. Once the 82593SX is configured for a 16-bit data path, all subsequent DMA transfers are performed on the data lines D0–D15. The two DMA channels are independent of each other. Both channels can request DMA service simultaneously for operations such as transmission and reception.

Dedicated logic in the DIU enables back-to-back transmission and reception when configured to Continuous Mode. This means that continuous transmissions and receptions can be handled by the 82593 without real time intervention of the CPU. In this mode, the DRQ and $\overline{EOP}$ pins can be used to discriminate between successful and unsuccessful operations.

The Bus Throttle Timer controls the maximum amount of time the 82593 can actively hold the bus (via the DMA controller) during a DMA cycle. This feature is programmable during configuration. The timer is started at the beginning of the first DMA cycle in a DMA burst ($\overline{DACK}$ and $\overline{RD}$ or $\overline{WR}$ active). It stops and is reset upon the $\overline{DACK}$ signal going inactive (the end of the DMA burst). If the timer expires, and the 82593 is still requesting DMA service, the 82593 will deassert its DMA request (DRQ0 or DRQ1) on the next DMA cycle, ending the DMA burst and releasing the bus. The 82593 will then reassert its DMA request after a minimum of two 82593 CLK period to complete the necessary DMA transfers.

SERIAL SUBSYSTEM

The 82593's Serial Subsystem is highly flexible in implementing the CSMA/CD protocol. It can operate in a variety of IEEE 802.3 and other CSMA/CD LAN environments, including 10BASE5 (Ethernet), 10BASE2 (Cheapernet), 10BASE-T (Twisted Pair Ethernet), 10BASE-F (Fiber Optic Ethernet), and 1BASE5 (StarLAN). The 82593 can be configured to interface directly with the Intel 82C501AD Ethernet Serial Interface device or to the AMD SIA device. Unlike the 82590, the 82593 does not provide encoding/decoding mechanisms for Manchester and NRZI (82590 High Integration Mode).

The programmable parameters include:

- Address Field Length
- Station Priority (Linear and Exponential Priority)
- Interframe Spacing
- Slot Time
- CRC-32 or CRC-16
- Preamble Length

The CSMA/CD unit is capable of running at speeds from dc to 20 Mb/s for the 82593SX, and dc to 16 Mb/s for the 82593SX.

The 82593 detects a collision when an active signal is driven on its $\overline{CDT}$/CLSN input. This signal is usually driven from the serial interface device (for example the Intel 82C501AD). It detects a carrier on the link when an active signal is driven on its $\overline{CRS}$/RENA input. The 82593 can be configured to filter the collision or carrier sense signal so that it must be active for at least 1 to 7 TXC periods before it is recognized.

FIFO SUBSYSTEM

The FIFO subsystem is located between the parallel subsystem and the serial subsystem. It consists of a 96-byte XMT FIFO, a 96-byte RCV FIFO, and FIFO control logic. The XMT and RCV FIFOs are independent, and individually provide an interface between the parallel and serial subsystems which may be running from different clock sources.

When configured to its 82590 compatible mode, the 82593 FIFO length defaults to 32 bytes for both the RCV and XMT FIFO, and the FIFO threshold (the level where a DMA request is asserted or deasserted) is fixed at 16 bytes. In all other configurations, the FIFO length is 96 bytes, with the FIFO threshold programmable through configuration. The 82593 can also be configured to delay the start of transmission until the programmed XMT FIFO threshold has been reached.

Expansion of the XMT FIFO to 96 bytes allows the 82593 to perform automatic transmission from within the XMT FIFO when a collision occurs during transmission.

PROGRAMMING MODEL—REGISTER OVERVIEW

Port 0

Figure 2 shows the 82593 Port 0 Command Register. Figure 3 shows the Port 0 commands. Port 0 is accessed when $\overline{CS0}$ is asserted, along with the assertion of the $\overline{RD}$ or $\overline{WR}$ signal. However, if the SWIT-TO-PORT-1 command is issued to the 82593, Port 1 will become the active port, even though $\overline{CS0}$ is asserted. To return to Port 0, the SWIT-TO-PORT-0 command is executed. Port switching should be used when the hardware does not support the second chip select line, $\overline{CS1}$. Port switching is disabled when hardware accesses to Port 1 via $\overline{CS1}$ are enabled.

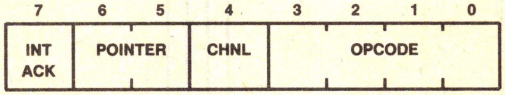


Figure 2. Port 0 Command Register

The 82593 can be configured to have 4 or 6 bytes of status registers in Port 0 (see Figures 5, 6, and 7). For the 4-byte status configuration, the first three registers (STATUS 0 through 2) contain the information about the last command executed, or the last frame received. The last status register, STATUS 3, contains the state of the 82593 Execution and Receive units. When the 82593 is configured to 6 bytes of status registers, the two additional bytes of status are used to report a more complete status of the most recently received frame, and also transmit chaining status (Continuous mode only).

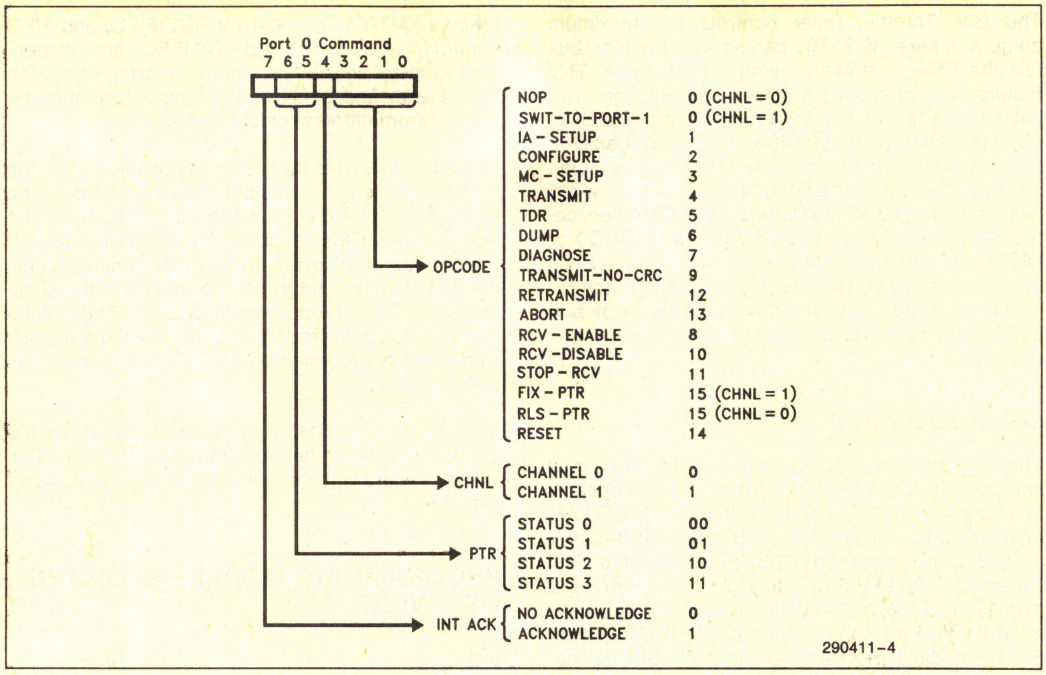


Figure 3. Port 0 Channels

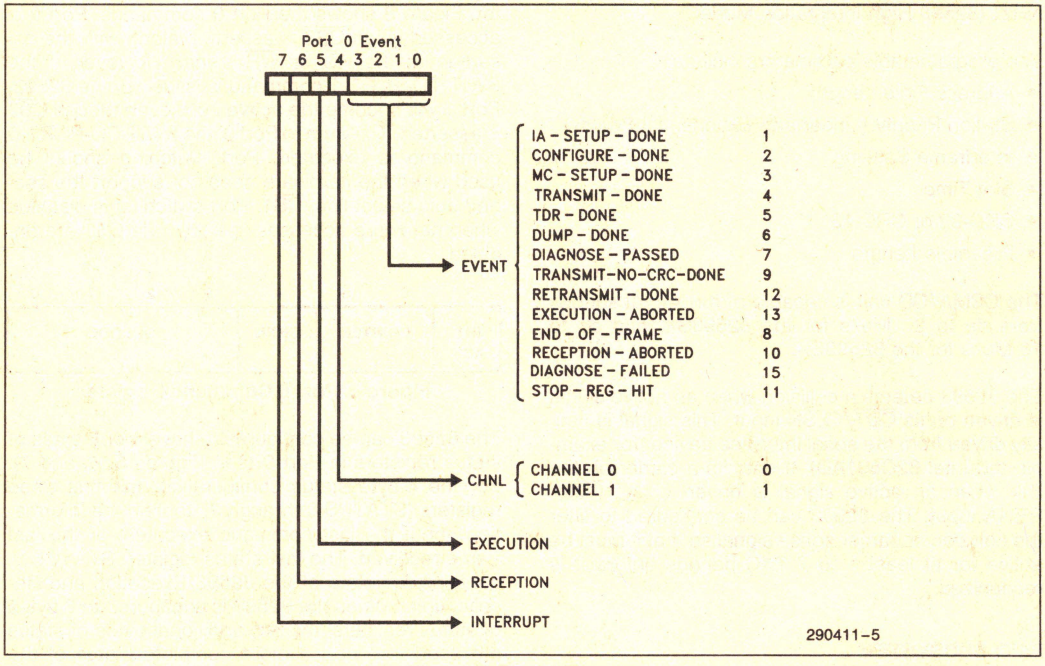


Figure 4. Port 0 Events

7	6	5	4	3	2	1	0	
INT	RCV	EXEC	CHNL	EVENT				STATUS 0
RESULT 1								STATUS 1
RESULT 2								STATUS 2
RCV CHNL	RCV STATE		RCVING NO RSC	0	EXEC CHNL	EXEC STATE		STATUS 3

Figure 5. Port 0 Status Registers—4 Bytes

7	6	5	4	3	2	1	0	
INT	RCV	EXEC	CHNL	EVENT				STATUS 0
RESULT 1								STATUS 1–0
RESULT 2								STATUS 1–1
RCV BYTE COUNT (LOW)/FFh								STATUS 2–0
RCV BYTE COUNT (HIGH)/FFh								STATUS 2–1
RCV CHNL	RCV STATE		RCVING NO RSC	0	EXEC CHNL	EXEC STATE		STATUS 3

Figure 6. Port 0 Status Registers—6 Bytes, Noncontinuous Mode

7	6	5	4	3	2	1	0	
INT	RCV	EXEC	CHNL	EVENT				STATUS 0
LAST XMT RESULT 1								STATUS 1–0
LAST XMT RESULT 2								STATUS 1–1
RCV FRAME POINTER (LOW)								STATUS 2–0
RCV FRAME POINTER (HIGH)								STATUS 2–1
RCV CHNL	RCV STATE		RCVING NO RSC	STP ON NO RSC	EXEC CHNL	EXEC STATE		STATUS 3

Figure 7. Port 0 Status Registers—6 Bytes, Continuous Mode

Port 1

Figures 8 and 9 show the 82593 Port 1 command register. The command register has two formats, a format for issuing the STOP-REGISTER-UPDATE command, and a format for all other commands issued to Port 1. Figure 10 shows the Port 1 commands. Port 1 is accessed when $\overline{CS1}$ is asserted, along with the assertion of the $\overline{RD}$ or $\overline{WR}$ signal. If the hardware configuration does not support $\overline{CS1}$, the SWIT-TO-PORT-1 command will switch the active port from Port 0 to Port 1. To return to Port 0, the SWIT-TO-PORT-0 command is executed.

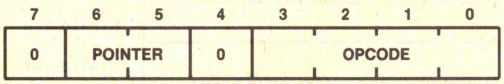


Figure 8. Port 1 Command Register, General Purpose Commands

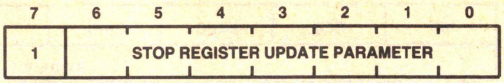


Figure 9. Port 1 Command Register, Stop Register Update Command

The Port 1 status registers are called Status Bank 1. The three registers contained in Status Bank 1 are shown in Figure 11. Status Bank 1 holds the value of the Stop Register, the Bus Throttle Timer, and the power down and high impedance states.

7	6	5	4	3	2	1	0	
0	0	PWRDN	0	0	0	0	HI-Z	STATUS 4
0	STOP REGISTER VALUE							STATUS 5
TC	BUS THROTTLE TIMER VALUE							STATUS 6

Figure 11. Port 1 Status Registers (Status Bank 1)

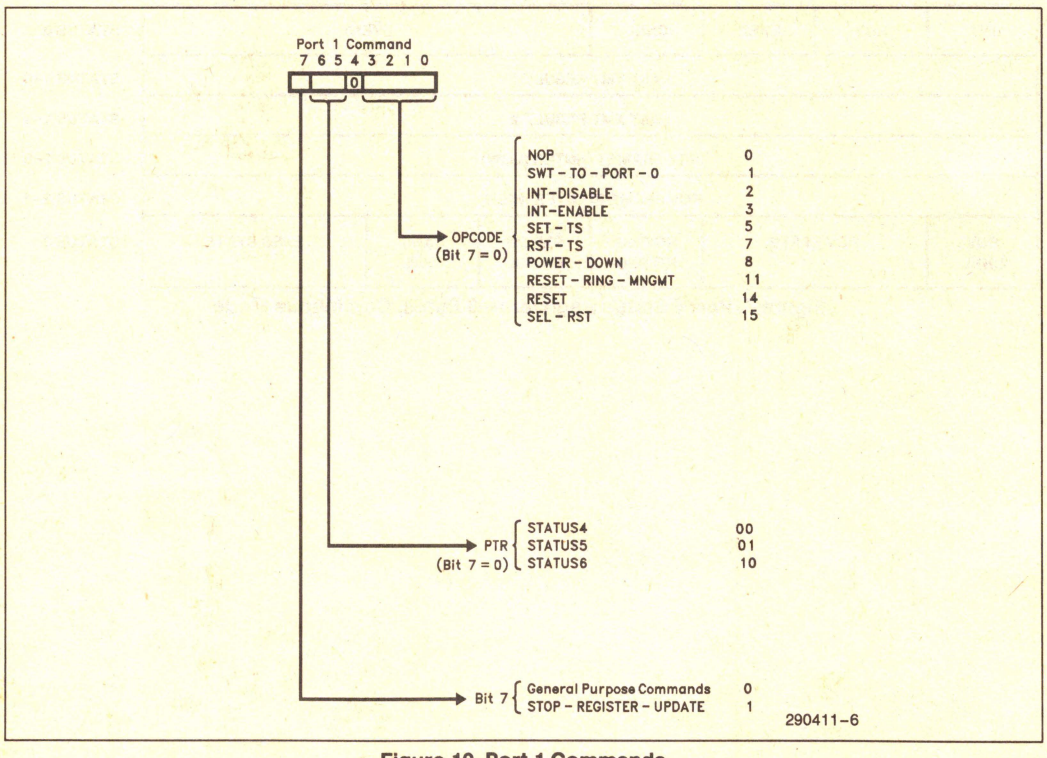


Figure 10. Port 1 Commands

82593 AND HOST CPU INTERACTION

The CPU interacts with the 82593 through the system's memory and the 82593's on-chip registers (see Figure 12). The CPU writes commands to the 82593 using the $\overline{CS0}$ (or $\overline{CS1}$) and $\overline{WR}$ signals, and reads status using $\overline{CS0}$ (or $\overline{CS1}$) and $\overline{RD}$. Parametric commands such as TRANSMIT, CONFIGURE, etc., require the transfer of data parameters from memory to the 82593. These data transfers are requested by the 82593 via its DRQ0 or DRQ1 lines, and are usually performed by an external DMA controller. When these data (or DMA) transfers are performed, $\overline{DACK0}$ or $\overline{DACK1}$ is asserted to the 82593 along with assertion of the $\overline{RD}$ or $\overline{WR}$ lines. Table 2 summarizes this operation.

Prior to issuing a parametric command to the 82593, the CPU creates a data structure in memory, and programs the external DMA controller with the start address and byte count of the memory block. For commands which require no transfer of parameters to the 82593, i.e.; TDR, DIAGNOSE, etc. the CPU issues the command to the device, without creating a data structure in memory. The 82593 performs the command with no further involvement from the CPU. Any parameters or data associated with the command are transferred between the memory and the 82593 by the DMA controller. Upon completion of the operation, the 82593 updates the appropriate status registers and asserts its INT line to the CPU.

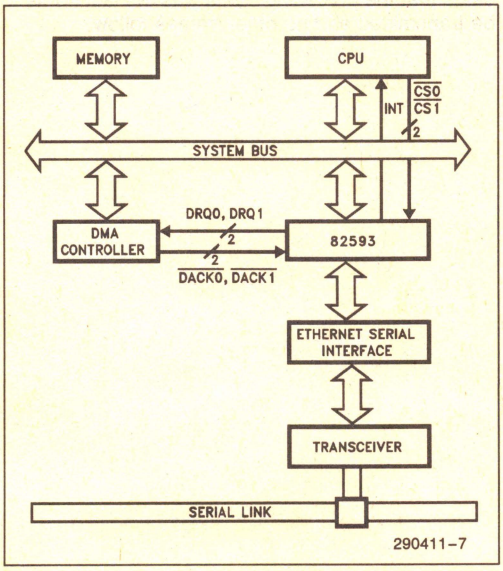


Figure 12. 82593 Host CPU Interaction

Table 2. Data Bus Control Signals and Functions

Pin Name			Function
$\overline{CS0}$ $\overline{CS1}$*	$\overline{RD}$	$\overline{WR}$	
1	X	X	No Transfer to/from
0	1	1	Command/Status
0	0	0	Illegal
0	0	1	Read from Status Register
0	1	0	Write to Command Register
$\overline{DACK0}$ $\overline{DACK1}$*	$\overline{RD}$	$\overline{WR}$	
1	X	X	No DMA Transfer
0	1	1	
0	0	0	Illegal
0	0	1	Data Read from DMA Channel 0 (or 1)
0	1	0	Data Write to DMA Channel 0 (or 1)

*Only one of $\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$, or $\overline{DACK1}$ may be active at any time.

FRAME TRANSMISSION

To transmit a frame, the CPU prepares a Transmit Data Block in memory as shown in Figure 13. Its first two bytes specify the length of the rest of the block. The next few bytes (up to six) contain the destination address of the station the frame is being sent to. The rest of the block is the data field. The CPU programs the DMA controller with the start address of the block, length of the block, and other control information and then issues a TRANSMIT command to the 82593. Upon receiving this command, the 82593 fetches the first two bytes of the block to determine its length. If the link is free and at least one data byte is loaded into the 82593's XMT FIFO, the 82593 begins transmitting the preamble and concurrently requests more bytes from the transmit buffer which are loaded into the XMT FIFO to keep them ready for transmission. The 82593 can also be configured to start transmission only after the initial 64 bytes of the transmit frame are written into its XMT FIFO. The 82593 independently resolves access and possible contention on the link (collisions). When the transmission is completed, the 82593 updates its status registers and raises its INT signal to inform the CPU of the completed transmission.

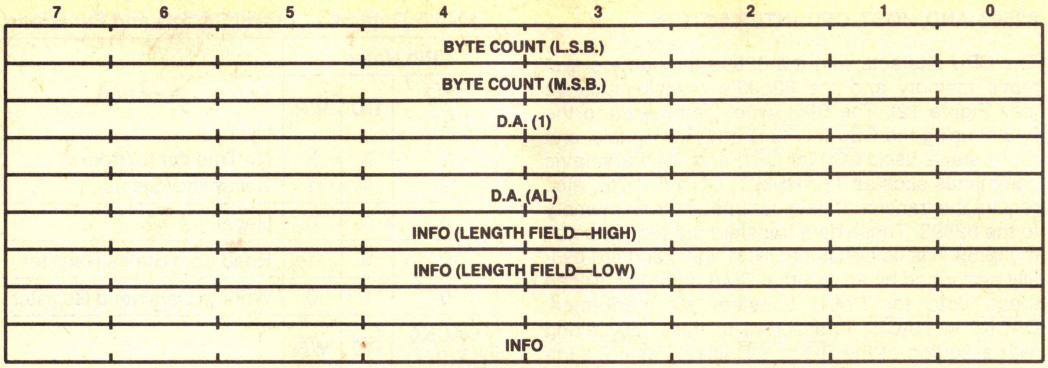


Figure 13. Transmit Frame Memory Structure

TRANSMIT FRAME CHAINING

When configured to Continuous mode, the 82593 can transmit consecutive frames without having the CPU issue the TRANSMIT command for each frame. This is called transmit frame chaining. Figure 14 shows the memory structure used for transmit chaining with the 82593 in 8-bit configuration. Figure 15 shows the structure for a 16-bit configuration. The CPU can place multiple transmit frames in memory, with each frame separated from the next by a TRANSMIT command byte. The command byte immediately follows the last byte of the transmit frame. It must contain one of three commands: TRANSMIT (04H), TRANSMIT-NO-CRC (09H) or NOP (00H).

Following a successful transmission, the 82593 requests the command byte which follows the last data byte of a frame. $\overline{EOP}$ is asserted during this cycle, indicating a successful transmission. Assertion of $\overline{EOP}$ in this mode can also be disabled.

If the command byte contains the TRANSMIT opcode, the 82593 will behave as if another TRANSMIT command has been issued by the CPU, and will attempt to transmit the new frame as soon as deferring is completed. A NOP in the command byte indicates that the preceding frame was the last frame to be transmitted and no other frames follow.

7 0	
BYTE COUNT (L.S.B.)	← Beg of the 1st Frame
BYTE COUNT (M.S.B.)	
DEST. ADDRESS	
DEST. ADDRESS (A.L.)	
LENGTH FIELD (LOW)	
LENGTH FIELD (HIGH)	
DATA FIELD	
LAST DATA FIELD BYTE	
COMMAND BYTE = 04H (TRANSMIT)	← Com for the 2nd Frame
BYTE COUNT (L.S.B.)	← Beg of the 2nd Frame
BYTE COUNT (M.S.B.)	
DEST. ADDRESS	
DEST. ADDRESS (A.L.)	
LENGTH FIELD (LOW)	
LENGTH FIELD (HIGH)	
DATA FIELD	
LAST DATA FIELD BYTE	
COMMAND BYTE = 09H (TX-NO-CRC)	← Com for the 3rd Frame
BYTE COUNT (L.S.B.)	← Beg of the 3rd Frame
BYTE COUNT (M.S.B.)	
DEST. ADDRESS	
DEST. ADDRESS (A.L.)	
LENGTH FIELD (LOW)	
LENGTH FIELD (HIGH)	
DATA FIELD	
LAST DATA FIELD BYTE	
CRC FIELD (4 BYTES)	
COMMAND BYTE = 00H (NOP)	← End of XMT Chain

Figure 14. Transmit Chaining Data Structure In Byte Mode

15 8	7 0	
BYTE COUNT (M.S.B.)	BYTE COUNT (L.S.B.)	← Beg of 1st Frame
D.A.	D.A.	
D.A. (ADDRESS LENGTH)		
INFO (LENGTH FIELD - HIGH)	INFO (LENGTH FIELD - LOW)	
INFO (LAST DATA BYTE)		
	COMMAND BYTE = 04H (TRANSMIT)	← Com for the 2nd Frame
BYTE COUNT (M.S.B.)	BYTE COUNT (L.S.B.)	← Beg of 2nd Frame
D.A.	D.A.	
D.A. (ADDRESS LENGTH)		
INFO (LENGTH FIELD - HIGH)	INFO (LENGTH FIELD - LOW)	
	INFO (LAST DATA BYTE)	
	COMMAND BYTE = 09 (TX-NO-CRC)	← Com for the 3rd Frame
BYTE COUNT (M.S.B.)	BYTE COUNT (L.S.B.)	← Beg of 3rd Frame
D.A.	D.A.	
D.A. (ADDRESS LENGTH)		
INFO (LENGTH FIELD - HIGH)	INFO (LENGTH FIELD - LOW)	
INFO (LAST DATA BYTE)		
CRC1	CRC0	
CRC3	CRC2	
	COMMAND BYTE = 00H	← End of XMT Chain

NOTE:
The second frame has an odd number of information bytes in this example.

Figure 15. Transmit Chaining Data Structure In Word Mode

AUTOMATIC RETRANSMISSION ON COLLISION

If the 82593 is configured for Internal Retransmission, the FIFO depth can be used to retransmit without the DMA controller involvement when a collision occurs. In an Ethernet network a collision should occur within the first 64 bytes (512 bits) of the transmission (within one slot time). When this configuration is used, the serial parameters should remain configured for Ethernet. A collision that occurs later than this window of 64 bytes will be flagged as a late collision and retransmission will not be attempted. The 82593 automatically prevents overwrite of the first 64 bytes in the FIFO until they have all been read out by the Serial Subsystem. The read counter of the XMT FIFO is reset, and the retransmission attempt is made using the data that is already contained in the FIFO. This process is performed automatically by the 82593. It is not necessary to reset the DMA channel for the retransmission attempt, nor is any CPU intervention required.

FRAME RECEPTION

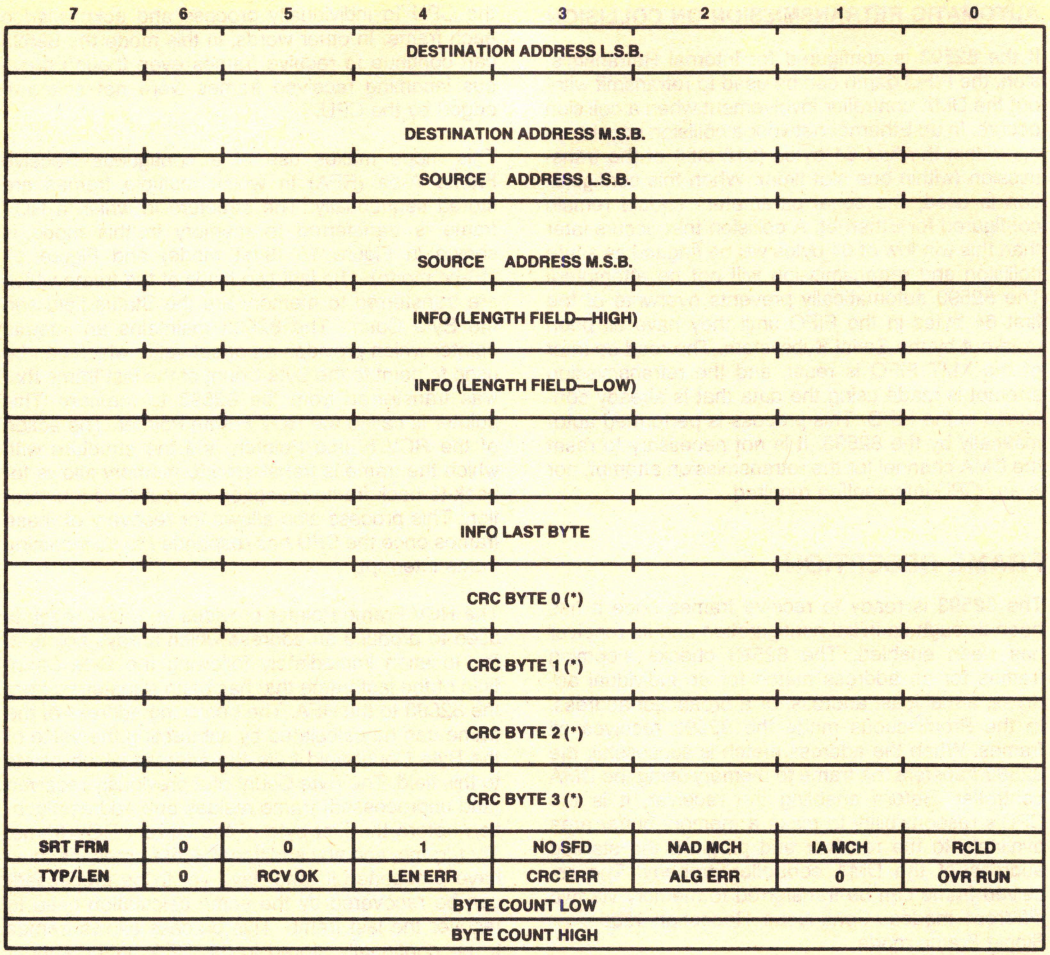
The 82593 is ready to receive frames once it has been through its initial configuration and its receiver has been enabled. The 82593 checks incoming frames for an address match for an individual address, a multicast address, or a broadcast address. In the Promiscuous mode the 82593 receives all frames. When the address match is successful, the 82593 transfers the frame to memory using the DMA controller. Before enabling the receiver, it is the CPU's responsibility to make a memory buffer area available to the receiver and program the starting address of the DMA controller properly. The received frame can be transferred to memory via two different modes, Continuous Reception mode, or Single Frame mode.

CONTINUOUS RECEPTION MODE

In the Continuous Reception mode the 82593 can receive back-to-back frames without the need for the CPU to individually process and acknowledge each frame. In other words, in this mode the 82593 can continue to receive frames even though previous incoming received frames were not acknowledged by the CPU.

This mode makes use of a contiguous Receive Frame Area (RFA) in which multiple frames are stored sequentially. The structure in which a RCV frame is transferred to memory in this mode is shown in Figure 16 (8-bit mode) and Figure 17 (16-bit mode). The last two fields of the frame which are transferred to memory are the Status field and the Byte Count. The 82593 maintains an internal pointer which provides an offset value which can be used to point to the Byte Count of the last frame that was transferred from the 82593 to memory. This pointer is called the RCV Frame Pointer. The action of the RCV Frame Pointer, and the structure with which the frame is transferred to memory allows for back-to-back frame reception without CPU intervention. This process also allows for recovery of these frames once the CPU has responded to an incoming frame interrupt.

The RCV Frame Pointer provides an offset which is used to produce an address which always points to the location immediately following the Byte Count field of the last frame that has been transferred from the 82593 to the RFA. The beginning address of the frame can be calculated by subtracting the value of the Byte Count field from the address which points to this field. The Byte Count of a previously received (and unprocessed) frame resides one address location before the first byte of the current RCV frame. That frame, and any additional RCV frames that may have preceeded it (and have yet to be processed) can be recovered by the same calculation used to recover the last frame. This process allows frames to be continually stored in the RFA buffer without CPU intervention, and to be recovered by the CPU for processing. Figure 18 illustrates the process of back-to-back frame reception.



NOTE:
*The CRC bytes marked with asterisks are transferred to memory only when the device is configured to do so.

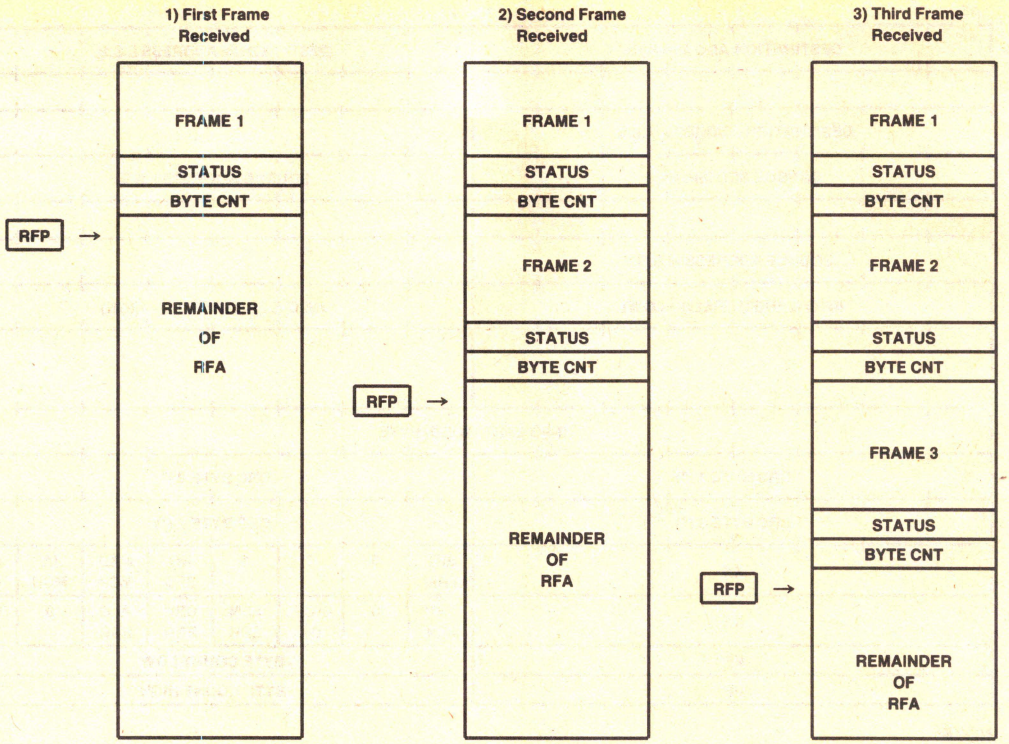
Figure 16. RCV Frame Format in Continuous Reception Mode (8-Bit Configuration)

15 — 8	7 — 0
DESTINATION ADD 2nd Byte	DESTINATION ADDRESS L.S.B.
DESTINATION ADDRESS M.S.B.	
SOURCE ADD 2nd Byte	SOURCE ADDRESS L.S.B.
SOURCE ADDRESS M.S.B.	
INFO (LENGTH FIELD—LOW)	INFO (LENGTH FIELD—HIGH)
INFO LAST WORD/BYTE	
CRC BYTE 1 (*)	CRC BYTE 0 (*)
CRC BYTE 3 (*)	CRC BYTE 2 (*)

XX	SRT FRM	0	0	1	NO SFD	NAD MCH	IA MCH	RCV CLD
XX	TYP /LN	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR ERR
FF	BYTE COUNT LOW							
FF	BYTE COUNT HIGH							

NOTE:
*The CRC bytes marked with asterisks are transferred to memory only when the device is configured to do so. If the total number of data bytes is odd, CRC Byte 3 will be written to both the LSB and MSB of the last CRC word. However, the Byte Count will ignore this duplication of the last byte, counting only four bytes of CRC.

Figure 17. Receive Format In Continuous Reception Mode (16-Bit Configuration)



NOTE:
The RFP always points to the location immediately following the last frame that was transferred to memory. Based on the value of the RFP and the byte count of each frame, the CPU recovers the RCV frames.

Figure 18. Back-to-Back Frame Reception in Continuous Reception Mode

RECEIVE STOP REGISTER (Ring Buffer Implementation)

The 82593 contains a Receive Stop Register. This feature, along with the Receive Frame Pointer, allows for implementation of a recyclable ring buffer when the 82593 is interfaced to a DMA controller (8237A, 82380/370, etc.) or bus (PC AT** compatible, EISA, etc.) which feature an auto-initialize mode. The Stop Register indicates the last location that has been processed in the RFA. This area of the RFA is now available for storage of new incoming frames. This allows the RFA to be continually recycled as it wraps around its ring buffer memory structure.

SINGLE FRAME RECEPTION

In Single Frame mode, the entire RCV frame is contained in one continuous buffer. Upon completion of reception, the status of the frame is appended at the end of the received frame and the total number of bytes transferred to memory is loaded into status registers 1 and 2. An interrupt is then generated to the CPU indicating that a frame has been received.

In this mode, the 82593 can receive one additional frame if an interrupt is pending from a previous reception. In other words, in this mode it can receive two frames without an acknowledge from the CPU. If a third frame arrives before one of the first two frames has been acknowledged, this frame will not be transferred to memory and may eventually overrun internally in the 82593. Figure 19 shows the format with which a received frame is transferred to memory from the 82593 in Single Frame mode in Byte mode. Figure 20 shows frame format in Word mode.

**PC AT is a registered trademark of IBM.

7	6	5	4	3	2	1	0
DESTINATION ADDRESS L.S.B.							
DESTINATION ADDRESS M.S.B.							
SOURCE ADDRESS L.S.B.							
SOURCE ADDRESS M.S.B.							
INFO (LENGTH FIELD - HIGH)							
INFO (LENGTH FIELD - LOW)							
INFO LAST BYTE							
CRC BYTE 0 (*)							
CRC BYTE 1 (*)							
CRC BYTE 2 (*)							
CRC BYTE 3 (*)							
SRT FRM	0	0	1	NO SFD	NAD MCH	IA MCH	RCLD
TYP/LEN	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR RUN

NOTE:
*The CRC bytes marked with asterisks are transferred to memory only when the device is configured to do so.

Figure 19. Receive Format in Byte, Single Buffer Reception Mode

15 — 8	7 — 0
DESTINATION ADD 2nd Byte	DESTINATION ADDRESS L.S.B.
DESTINATION ADDRESS M.S.B.	
SOURCE ADD 2nd Byte	SOURCE ADDRESS L.S.B.
SOURCE ADDRESS M.S.B.	
INFO (LENGTH FIELD—LOW)	INFO (LENGTH FIELD—HIGH)
INFO LAST WORD/BYTE	
CRC BYTE 1 (*)	CRC BYTE 0 (*)
CRC BYTE 3 (*)	CRC BYTE 2 (*)

XX	SRT FRM	0	0	1	NO SFD	NAD MCH	IA MCH	RCV CLD
XX	TYP /LN	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR ERR

NOTE:
*The CRC bytes marked with asterisks are transferred to memory only when the device is configured to do so. If the total number of data bytes is odd, CRC Byte 3 will be written to both the LSB and MSB of the last CRC word. However, the Byte Count will ignore this duplication of the last byte, counting only four bytes of CRC.

Figure 20. Receive Format In Word, Single Buffer Reception Mode

82593 CHANGES FROM THE 82590

The 82593 has a number of functional changes from the 82590. Some changes are functional enhancements from the 82590, while some changes are deletions of currently existing 82590 functionality.

This section is provided for the reader who is currently familiar with the 82590. For more information on the 82590 please consult the Intel LAN Components User's Manual.

Enhancements

Parallel Subsystem Enhancements

- **FIFO Subsection**—The RCV and XMT FIFOs of the 82593 are both expanded to 96 bytes deep, giving a total of 192 bytes of buffering on the device. The 82593 FIFOs can be configured to an 82590 compatible mode of 32 bytes each, and a threshold set at 16.
- **Internal Retransmission From XMT FIFO**—The 82593 can be programmed to hold the first part of a transmit frame internally in its XMT FIFO. In the case of a collision, the data for retransmission is automatically retransmitted from the XMT FIFO.
- **Start of Transmit Threshold**—The 82593 can be configured to delay start of transmission until the XMT FIFO threshold has been reached.
- **Bus Throttle Timer**—The 82593 can be programmed to a maximum time that it can have access to a system bus. When this timer expires, the 82593 will deassert its DMA request releasing the bus.
- **RCV Frame Pointer**—The 82593 contains a counter and a status register which points to the last RCV frame transferred to memory. This enables back-to-back frame reception without CPU intervention or the addition of external glue. The size of the counter is programmable.
- **RCV STOP Register**—The 82593 contains a RCV Stop Register which can be used to implement a recyclable ring buffer in conjunction with the RCV Frame Pointer.
- **Dynamic CRC Enable/Disable on XMT**—The 82593 can dynamically enable or disable insertion of CRC for individual transmit frames.
- **Transmit Frame Chaining Statistics**—The 82593 provides the status of each frame in a chain of transmissions in its status registers until it is replaced by the next frame in the chain. The $\overline{EOP}$ pin signals to the system that a status is available.
- **Synchronous DRQ Deassertion**—The 82593 can be configured to always deassert its transmit DRQ line synchronously to the falling edge of $\overline{WR}$ even when transmission is terminated due to an error condition such as Underrun, Lost CRS or CTS, etc.
- **Port 1 Redefined**—Port 1 functionality has been reduced and modified. Port 1 supports maintenance commands and new commands controlling the RCV Frame Pointer and RCV Stop Register. Port 1 status contents has also been redefined. It now holds the Stop Register and Bus Throttle Timer contents and the Power-Down Status.
- **Big Endian (Byte Swapping) Redefined**—When the Big Endian mode is enabled, the Byte Count field is not swapped. Only the Data field of transmit and receive packets are swapped.

Serial Subsystem Enhancements

- **LPBK/CTS Pin Polarity**—The 82593 LPBK output, and CTS input polarity is selectable by configuration. This allows for a direct interface to the 82C501AD LPBK input.
- **IFS Window Implementation**—The 82593's IFS (Inter Frame Space) counter can be configured to be retriggerable for up to ⅔ of the IFS after frame transmission.
- **Late Collision Detection**—The 82593 interprets a late collision as one which occurs after a slot time has expired from the beginning of the preamble.
- **CRS1 Mode**—The 82583 CRS1 mode provides carrier lost detection for broadband applications.
- **RCV Grace Period**—The 82593 can be configured to delay sampling of receive data for the first 8-bit times of the preamble.
- **Hash Table Decode**—The 82593 can be configured to decode writing into its Hash Table during a MC Setup by two different hashing methods.
- **Length/Type Field Discrimination**—The 82593 can be configured to interpret the Length/Type field as a Type field for values in this field greater than 1500.
- **$\overline{RTS}$ Pin State**—$\overline{RTS}$ is guaranteed to be in the inactive state on power up (regardless of whether TXC or CLK is active), before and during reset assertion. Hardware reset triggers this pin from the high impedance state.
- **OR CDT/CRS**—The 82593 can be configured to logically OR internally the CDT and CRS pins during transmission.
- **Foreign ESI Mode**—The 82593 provides configurability of the serial interface pins polarity and timing in order to be compatible with either the Intel 82C501AD or the AMD SIA serial interface device.

DELETIONS

Serial Subsystem Deletions

- **Deterministic Collision Resolution Mode (DCR)**—DCR is not implemented in the 82593.
- **82590 Mode 0 Functionality**—The Mode 0, or High Integration Mode of the 82590, and its associated functionality, is not included in the 82593.
- **INT CDT/CDBBC**—Internal CDT and the CDBBC mode of collision detect are not included in the 82593.
- **RCV Jabber**—RCV jabber functionality is not included in the 82593. XMT jabber is still included.
- **Serial Parameters Configurability Reduced**—The 82593 supports a reduced set of configurable serial parameters.
- **Manchester Encoding**—The 82590 Mode 1 Manchester Encoding functionality is not included in the 82593.
- **HDLC Framing**—HDLC framing is not supported in the 82593.
- **Preamble until CRS**—This mode is not supported in the 82593.

Parallel Subsystem Deletions

- **General Purpose Timer**—The General Purpose Timer is not included in the 82593.
- **Event Counters**—The three Event Counters are not included in the 82593.
- **Remote Power Down**—The 82593 has only the Local Power Down mode (referred to as Power Down). Remote Power Down mode has been deleted.
- **RCV Buffer Chaining and Frame Switching Modes**—The RCV Buffer Chaining and RCV Frame Switching modes are not implemented in the 82593.
- **Non TCI EOP Modes**—The XMT and RCV EOP modes have been deleted. The 82590 TCI mode remains in the 82593. It is called Continuous mode. The $\overline{EOP}$ and DRQ pins maintain the previous TCI signals handshake. As an option, TCI signalling may be disabled.
- **Port Switching Simplified**—Software switching between ports (Port 0 or 1) is not enabled if hardware access to both ports (both $\overline{CS0}$ and $\overline{CS1}$ are enabled) is implemented. The 82593, however, keeps compatibility with the workaround fix of the "SWIT-TO-PORT-1 erratum" of the 82590.
- **Frame Count In Status**—The 82593 does not record the Frame Count field in its RCV status registers.

APPLICATIONS

PC MOTHERBOARD APPLICATIONS

The 82593 has several unique features that enable implementing a high-performance LAN connection on a PC motherboard with minimal cost and complexity.

Figure 21 shows a 82593 based LAN design on a PC motherboard. It consists of an 82593, a PLD, and two transceivers.

This solution uses the available system resources (DMA and memory) to provide those functions normally added to a LAN solution. Removing DMA and local memory reduces cost and complexity of a LAN solution. Two host DMA channels, one for receive and one for transmit, are used. The DMA interface from the 82593 (through the PLD) is the standard handshake of DMA request and acknowledge. The required memory buffer size depends on the specific applications and the amount of free memory available. The buffer size can be specified by the programmer.

Peripherals on a motherboard must compete for access to the system bus. Because there is no local buffer for intermediate buffering of data, data transfers take place in real time over the system bus to system memory. A very large internal storage area (96-byte receive and transmit FIFOs) enables the 82593 to wait for access to the system bus while serial data is being received or transmitted. The depth of the transmit FIFO allows the 82593 to retransmit the data without DMA involvement, thus reducing the load on the PC bus. The on-chip logic of the 82593 provides a recyclable ring buffer on the PC bus without any external glue.

CUSTOMIZED APPLICATIONS

The 82593 can be interfaced to an ASIC (or Gate Array) device which provides a custom solution for a variety of applications. The 82593 functions as the CSMA/CD core of this type of solution, with the ASIC providing the control and interface functionality usually performed by several ICs. This allows for the implementation of a low component count, cost effective solution for a variety of buses, including buses for which highly integrated, customized silicon is not currently offered. Figure 22 illustrates a 82593SX/ASIC solution.

The ASIC can provide a direct interface to the host system (the host can be either a proprietary or standard bus), performing functions such as address decoding, and control and data interface. The ASIC also directly supports the 82593 and any local mem-

ory required in the solution. The ASIC asserts the $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$ to the 82593 for host accesses to its command or status registers. The ASIC provides the control for host accesses to the local memory, to allow the host to access data for transmission, reception, or initialization. It provides DMA support to the 82593 during operations such as transmission, configuration, and reception. The ASIC also arbitrates simultaneous accesses to the local memory between the host system and the 82593.

EMBEDDED APPLICATIONS

The 82593 can also work in a variety of embedded applications. These applications can include industrial control, interconnect, and print servers among others. These applications can utilize the 82593 interfaced to an ASIC or interfaced to standard components such as the Intel 80C186 embedded processor. The 82593 has a glueless interface to the 80C186 (or 80C188). The 80C186 is a highly integrated embedded processor. It contains a DMA unit, address decoding, a control unit, and an interrupt controller. These functions allow it to directly control the 82593 without the need for external logic. Its two channel DMA unit services the 82593 receive and transmit DMA requests, transferring data between the 82593 and the local memory resources. Its control and address decoding allow direct access to the 82593's command and status registers via the 80C186's Data, $\overline{PCS}$ and $\overline{RD}$ or $\overline{WR}$ lines. The 82593 interrupts the 80C186 through one of the 80C186 INT lines. Figure 23 illustrates the interface between the 80C186 and the 82593.

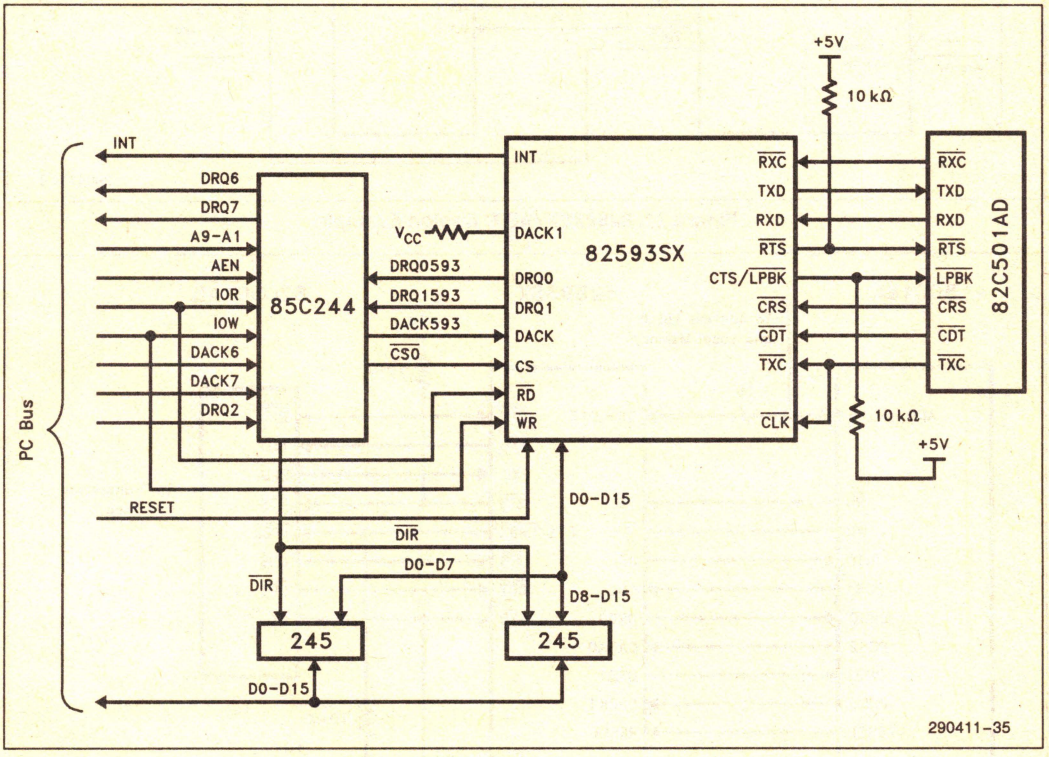


Figure 21. PC Motherboard Solution

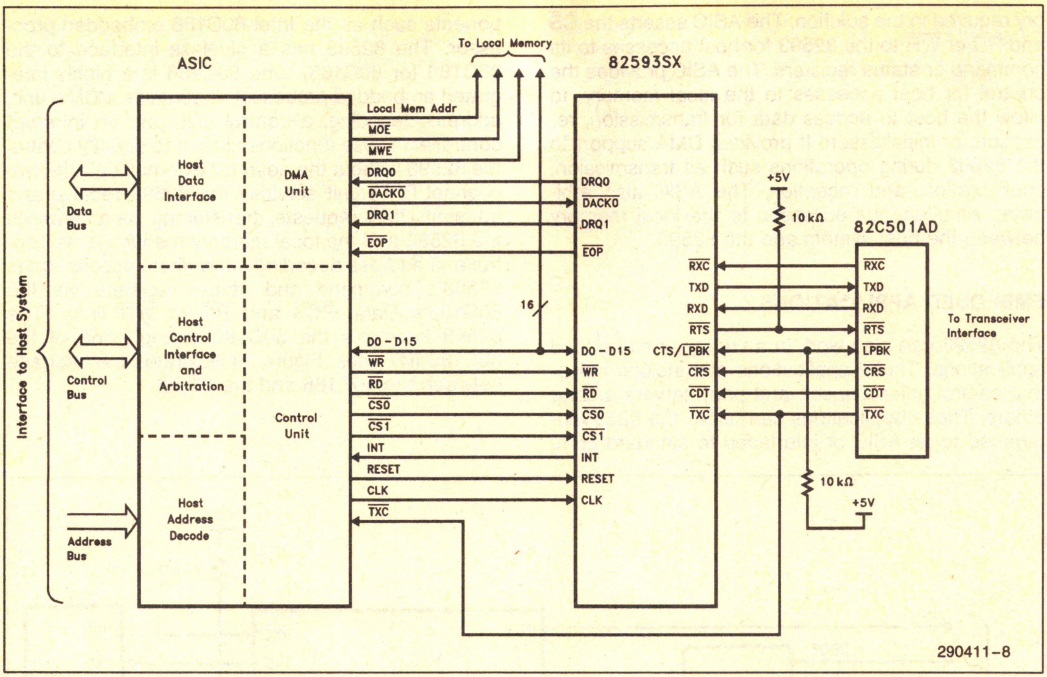


Figure 22. 82593SX/ASIC Design Example

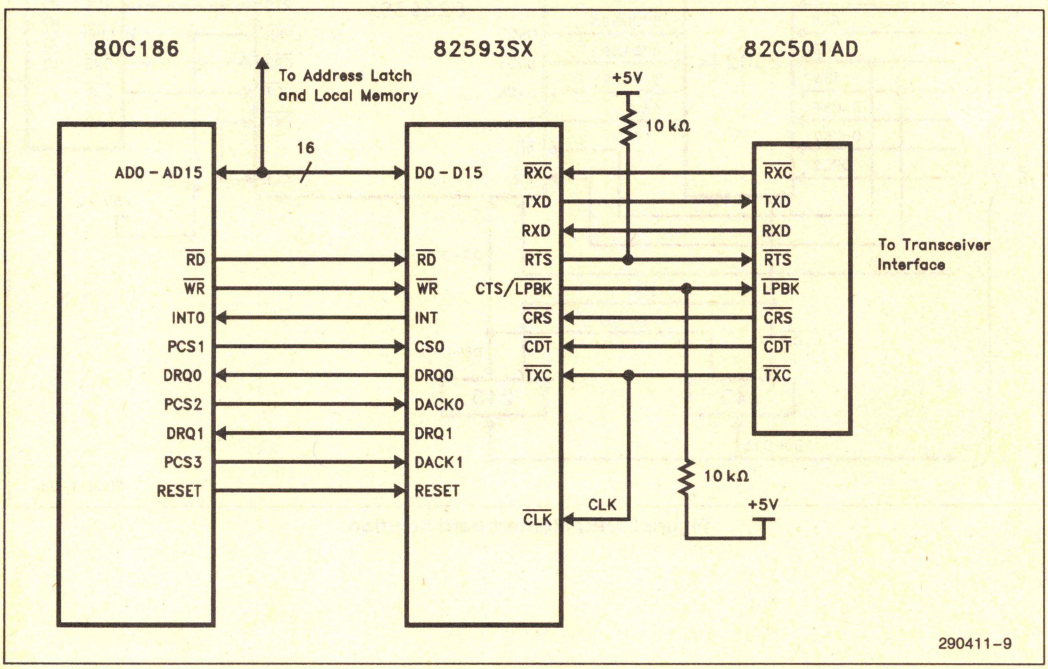


Figure 23. 82593SX/80C186 Interface

ABSOLUTE MAXIMUM RATINGS

Case Temperature (T_C) Under Bias
- Plastic ..... 0°C to +85°C
- PLCC ..... 0°C to +85°C

Storage Temperature ..... −65°C to +140°C

Voltage on any Pin with Respect to Ground ..... −1V to +7V

Power Dissipation ..... 330 mW

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

PACKAGE THERMAL SPECIFICATIONS

Parameter	Thermal Resistance	
	PLCC	PDIP
θJunction-to-Case	16 C°/Watt	36 C°/Watt
θJunction-to-Ambient	36 C°/Watt	96 C°/Watt

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%; I_{CC} = 60 mA

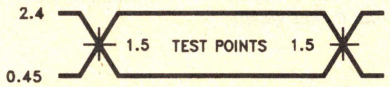
Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (TTL)	−0.5	+0.8	V	
V_{IH}	Input High Voltage (TTL)	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (TTL)		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage (TTL)	2.4		V	I_{OH} = −400 μA
I_{LI}	Input Leakage Current		+10	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45 \le V_{OUT} \le V_{CC}$
C_{IN}	Capacitance of Input Buffer		10	pF	FC = 1 MHz
C_{OUT}	Capacitance of Input/Output Buffer		20	pF	FC = 1 MHz
I_{CC}	Power Supply Current		60 7	mA mA	Active Power Down

NOTES:
1. D0–D15 capacitance is 20 pF–125 pF. All other pins capacitance is 20 pF–50 pF.
2. $\overline{RTS}$/TENA I_{OH} is 2.4 mA in Foreign ESI mode, $\overline{CTS}$/LPBK I_{OH} is 2.4 mA when LPBK is asserted and R_{VSS} = 2.2K.
3. All currents without loading.
4. Power down mode—all inputs at idle level except CLK input.

SYSTEM INTERFACE A.C. TIMINGS

A.C. Timings Test Waveform

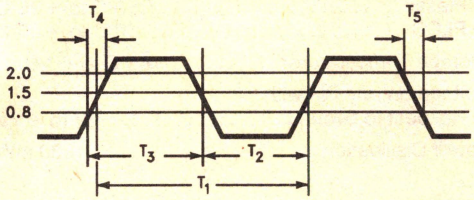
The measurements should be done at:



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A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 1.5V for both a logic "1" and "0".
Rise and fall time of inputs and outputs signals are measured between 0.8V and 2V respectively.

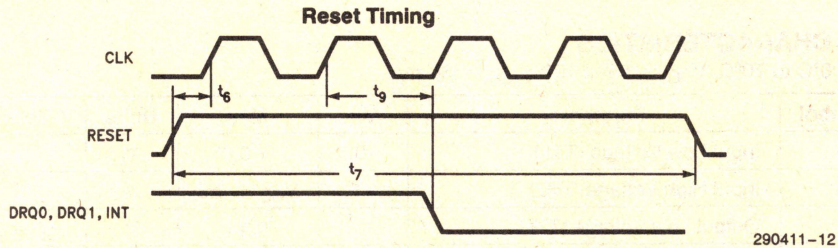
System Clock Timing



290411-11

For CLK: t3 and t2 are 20 ns minimum @ 20 MHz.

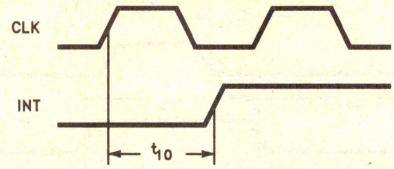
Reset Timing Diagram



290411-12

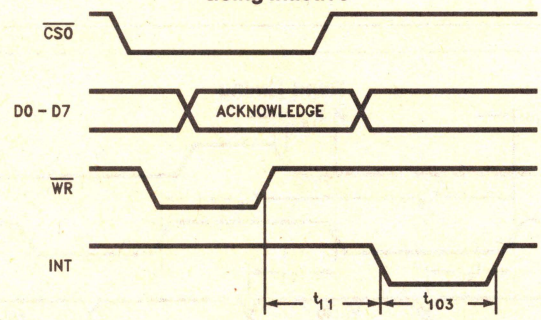
Interrupt Timing Diagrams

Going Active from CLK



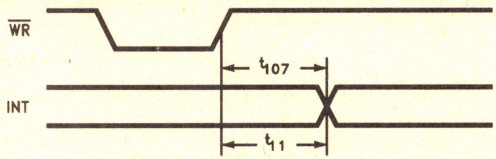
290411-13

Going Inactive



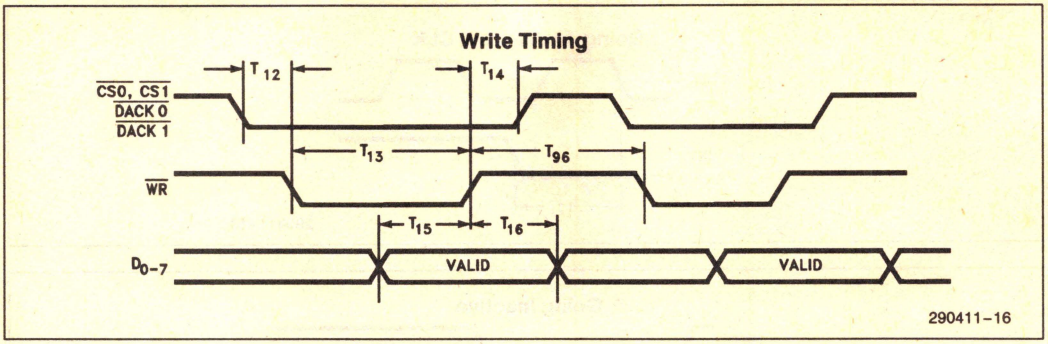
290411-14

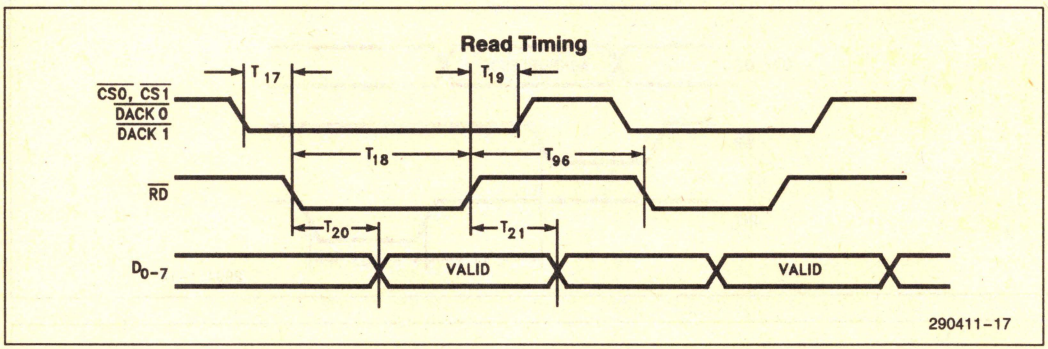
Going Active/Inactive from int-Disable, int-Enable Commands



290411-15

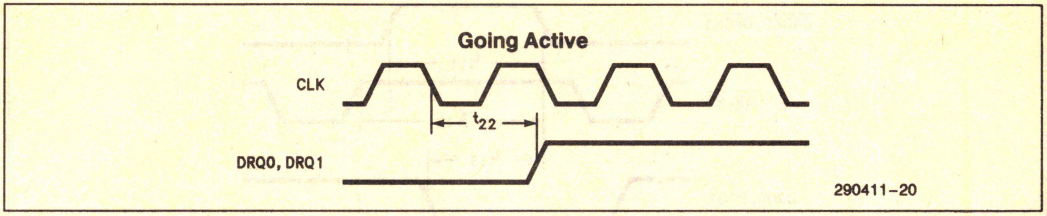
Write/Read Timing Diagrams

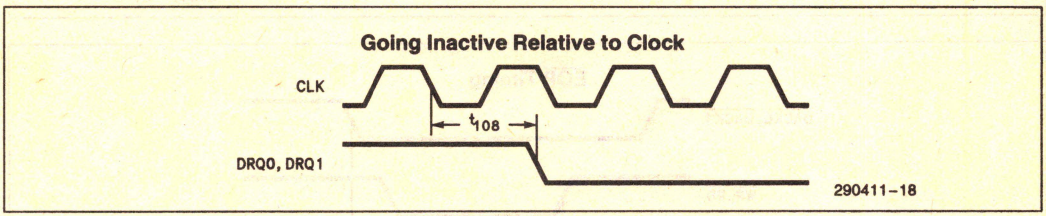


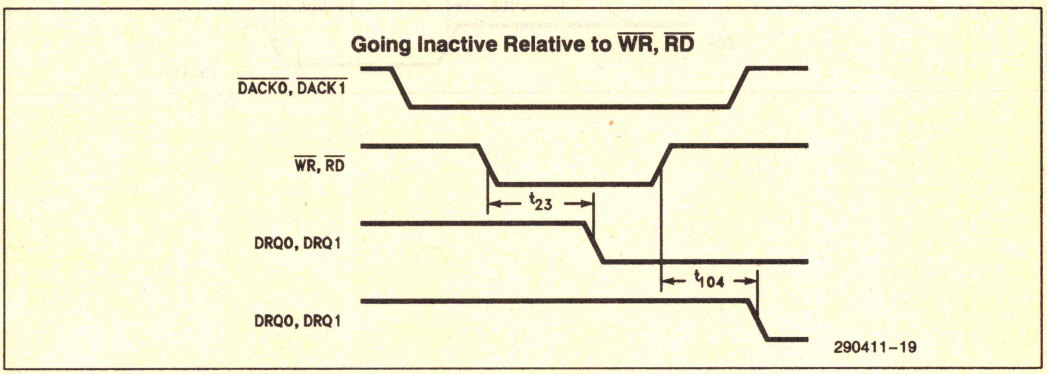


DRQ, EOP Timing Diagrams

DMA REQUEST

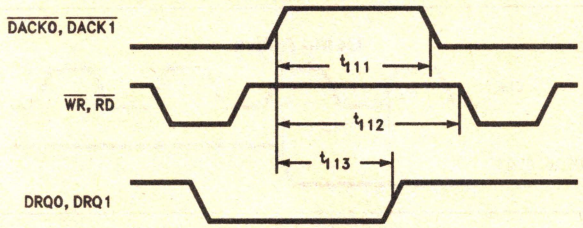






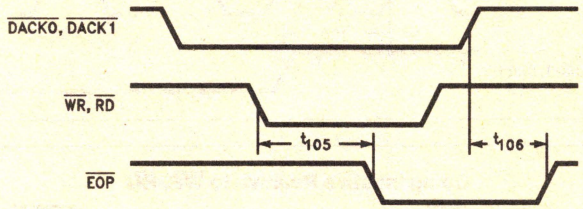
DRQ, EOP Timing Diagrams (Continued)

DMA Acknowledge Inactive Timing



290411-21

EOP Timing



290411-22

SYSTEM INTERFACE TIMING CHARACTERISTIC VALUES

C1 on all outputs is 20 pF–125 pF for D0–D15 and 20 pF–50 pF for other pins.

Symbol	Parameter	Min	Max	Units	Note
CLOCK INPUT PARAMETERS					
t1 t1a	CLK Cycle Period (16 MHz) CLK Cycle Period (20 MHz)	62.5 50.0	1000 1000	ns ns	
t2 t2a	CLK Low Time (16 MHz) CLK Low Time (20 MHz)	24 20		ns ns	5 5
t3 t3a	CLK High Time (16 MHz) CLK High Time (20 MHz)	24 20		ns ns	5 5
t4	CLK Rise Time		5	ns	1
t5	CLK Fall Time		5	ns	2
RESET PARAMETERS					
t6	Reset Active to Clock High	16		ns	3
t7	Reset Pulse Width	4*t1		ns	
t9 t9a	CTRL Inact aft Reset (16 MHz) CTRL Inact aft Reset (20 MHz)		125 100	ns ns	
INTERRUPT PARAMETERS					
t10	CLK High to Interrupt Active		45	ns	
t11	$\overline{WR}$ Idle to Interrupt Idle		45	ns	
t103	Int Low to Int High Gap	2*t1		ns	
t107	$\overline{WR}$ Idle to Interrupt Active		45	ns	
WRITE PARAMETERS					
t12	$\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$, or $\overline{DACK1}$ Setup to $\overline{WR}$ Low	0		ns	
t13 t13a	$\overline{WR}$ Pulse Width (16 MHz) $\overline{WR}$ Pulse Width (20 MHz)	55 45		ns ns	
t14	$\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$ or $\overline{DACK1}$ Hold after $\overline{WR}$ High	0		ns	
t15	Data Setup to $\overline{WR}$ High	25		ns	
t16	Data Hold after $\overline{WR}$ High	0		ns	
t96 t96a	CTRL/$\overline{CTRL}$ Inactive (16 MHz) CTRL/$\overline{CTRL}$ Inactive (20 MHz)	55 45		ns ns	10 10
READ PARAMETERS					
t17	$\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$ or $\overline{DACK1}$ Setup to $\overline{RD}$ Low	0		ns	
t18 t18a	$\overline{RD}$ Pulse Width (16 MHz) $\overline{RD}$ Pulse Width (20 MHz)	55 45		ns ns	
t19	$\overline{CS0}$, $\overline{CS1}$, $\overline{DACK0}$ or $\overline{DACK1}$ Hold after $\overline{RD}$ High	0		ns	

SYSTEM INTERFACE TIMING CHARACTERISTIC VALUES (Continued)

C1 on all outputs is 20 pF–125 pF for D0–D15 and 20 pF–50 pF for other pins.

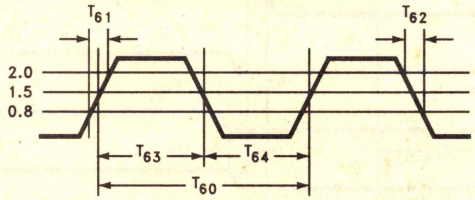
Symbol	Parameter	Min	Max	Units	Note
READ PARAMETERS (Continued)					
t20 t20a	$\overline{RD}$ Low to Data Valid (16 MHz) $\overline{RD}$ Low to Data Valid (20 MHz)		45 35	ns ns	6 6
t21	Data Float after $\overline{RD}$ High	2	30	ns	
DMA PARAMETERS					
t22	CLK Low to DRQ0/1 Active		45	ns	
t23	$\overline{WR}$/$\overline{RD}$ Low to DRQ0/1 Inactive		33	ns	
t104	$\overline{WR}$/$\overline{RD}$ High to DRQ0/1 Inactive, NOK TCI Signal	5	45	ns	
t105	$\overline{WR}$ or $\overline{RD}$ Low to $\overline{EOP}$ Active		30	ns	7
t106	$\overline{EOP}$ Float after $\overline{DACK0}$ or $\overline{DACK1}$ Going Inactive	2	40	ns	7
t108	CLK Low to DRQ0 or DRQ1 Inactive		45	ns	8
THROTTLE PARAMETERS					
t111	$\overline{DACK}$ High to $\overline{DACK}$ Low	2*t1		ns	9
t112	$\overline{DACK}$ High to Next DMA $\overline{WR}$/$\overline{RD}$	2.5*t1		ns	9
t113	$\overline{DACK}$ High to DRQ Reassertion	1*t1		ns	

NOTES:
1. 0.8V to 2.0V.
2. 2.0V to 0.8V.
3. To guarantee recognition at next clock.
5. Measured at 1.5V.
6. 60 ns with up to 200 pF load (NMOS compatible).
7. Open collector IO pin.
8. Valid for ABORT only.
9. None of the A.C. parameters related to the CLK out pin.
10. For Command to Command $\overline{WR}$ minimum is 9 t1 + t96.
    For $\overline{WR}$ to $\overline{RD}$, minimum is 3 t1 + t96.
    For $\overline{CS0/1}$ $\overline{WR}$ to $\overline{CS0/1}$ $\overline{WR}$, minimum is 9 t1 + t96.
    For $\overline{CS0/1}$ $\overline{RD}$ to $\overline{CS0/1}$ $\overline{WR}$, minimum is 3 t1 + t96.
    For DMA access to CS0/1# access, minimum is 2 t1.
    For $\overline{CS0/1}$ access to DMA access, minimum is 2 t1.
    For Status 2 to 3 $\overline{RD}$ to $\overline{RD}$ access, minimum is 2 t1 + t96.
    Maximum DMA rate is 1 Transfer for each 2 t1.

SERIAL INTERFACE A.C. TIMINGS

Clock Timing

Serial Input Clock Timing

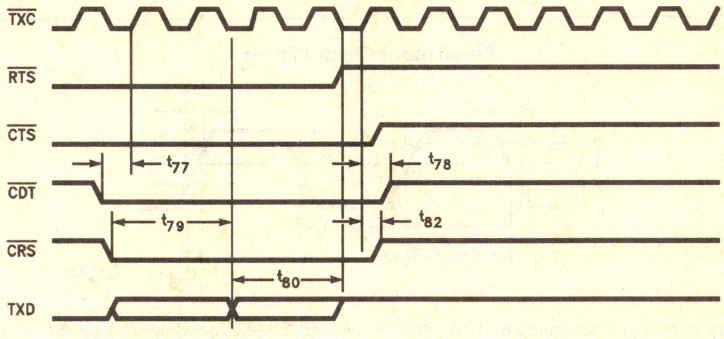


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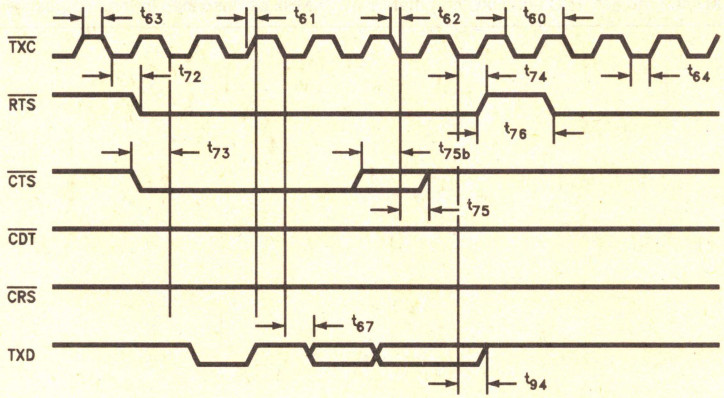
NOTES:
High level may vary with V_{CC}. A tolerance of ±100 PPM is required for Ethernet only. The 82593 can operate with the 82501 $\overline{RXC}$ and $\overline{TXC}$ and the SIA TXC and RXC parameters at 10 MHz as described in their respective data sheet.

Transmit Data Timing Diagrams—82C501 Mode

Transmit Data Waveforms

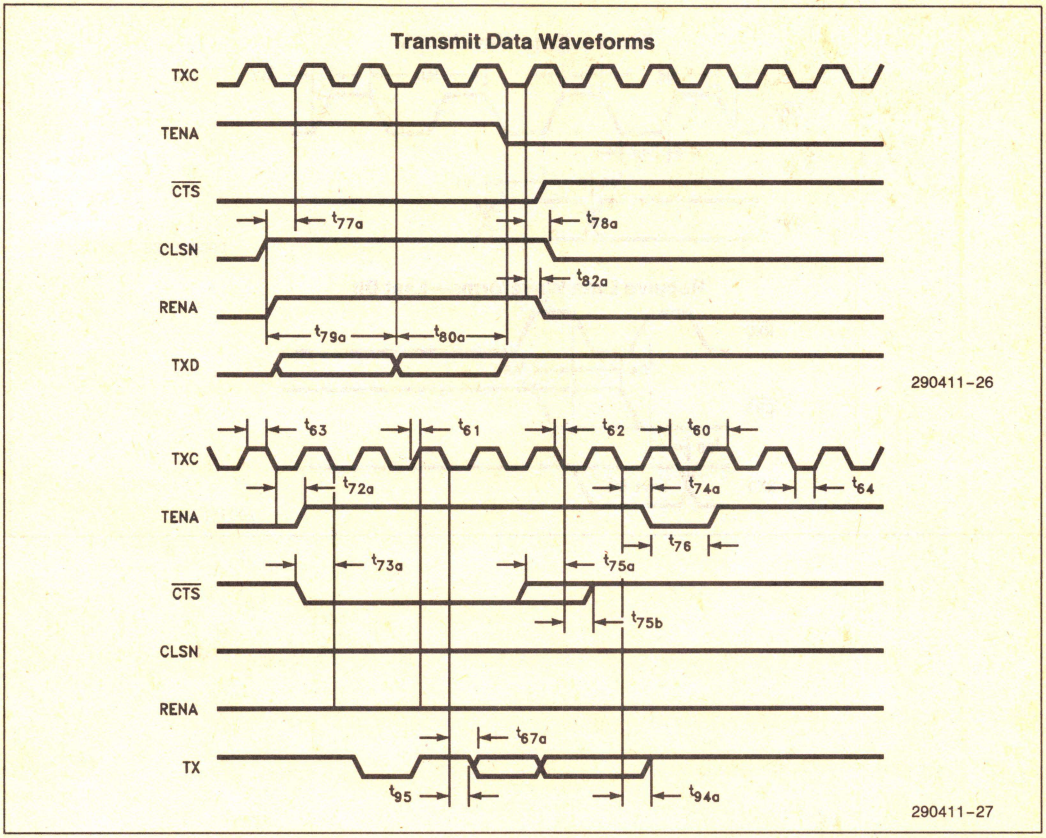


290411-24

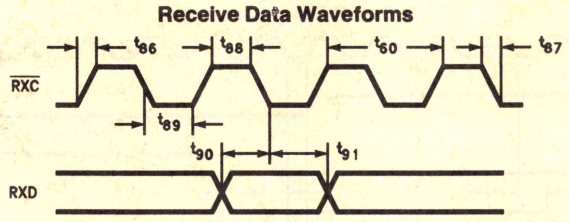


290411-25

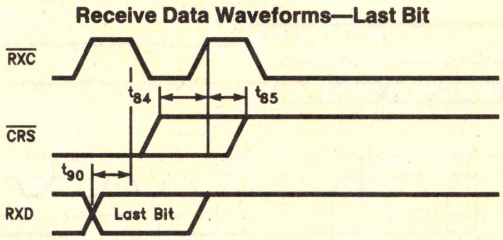
Transmit Data Timing Diagrams—Foreign ESI Mode



Receive Data Timing Diagrams—82C501 Mode



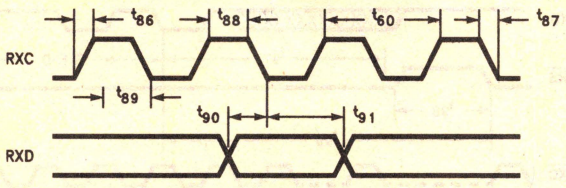
290411-28



290411-29

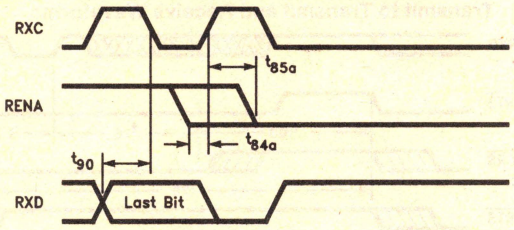
Receive Data Timing Diagrams—Foreign ESI Mode

Receive Data Waveforms



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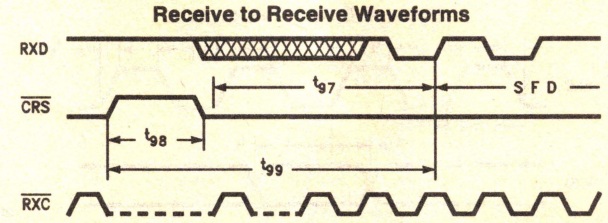
Receive Data Waveforms—Last Bit



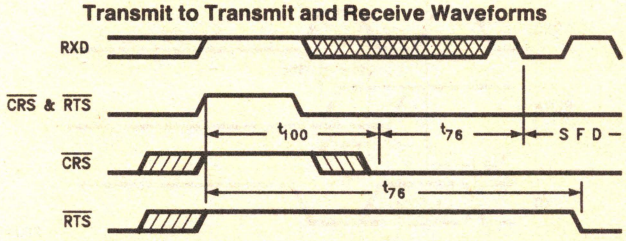
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Interframe Spacing Timings

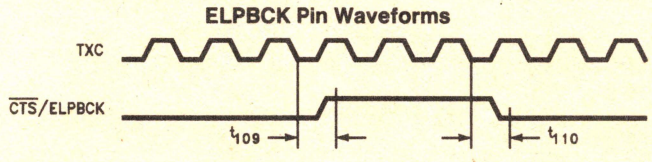


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290411-33

External Loopback Timings



290411-34

SERIAL A.C. TIMING CHARACTERISTIC VALUES

Symbol	Parameter	16 MHz		20 MHz		Units	Notes	ESI
		Min	Max	Min	Max			
TRANSMIT/RECEIVE CLOCK PARAMETERS								
t60	$\overline{RXC}$, $\overline{TXC}$ Cycle	62.5		50		ns	1	B
t61	$\overline{TXC}$ Rise Time		4		5	ns	1	B
t62	$\overline{TXC}$ Fall Time		4		5	ns	1	B
t63	$\overline{TXC}$ High Time	23		19		ns	1	B
t64	$\overline{TXC}$ Low time	23		18		ns	1	B
TRANSMIT DATA PARAMETERS								
t65	TXD Rise Time		10		10	ns	4	B
t66	TXD Fall time		10		10	ns	4	B
t67	$\overline{TXC}$ Low to TXD Valid		30		25	ns	4	I
t94	$\overline{TXC}$ Low to TXD High (At The Transmission End)		30		25	ns	4	I
t94a	TXC Low to TXD High (At The Transmission End)				25	ns	4	A
t67a	TXC Low to TXD Valid				25	ns	4	A
t95	TX Hold after TXC Low			5		ns	4	A
RTS, CTS PARAMETERS								
t72	$\overline{TXC}$ Low to $\overline{RTS}$ Low Time to Activate $\overline{RTS}$		30		25	ns	5	I
t73	$\overline{CTS}$ Low to $\overline{TXC}$ Low $\overline{CTS}$ Setup Time		25		20	ns	2	I
t73a	$\overline{CTS}$ Low to TXC Low $\overline{CTS}$ Setup Time		25		20	ns	2	A
t74	$\overline{TXC}$ Low to $\overline{RTS}$ High		30		25	ns	5	I
t75	$\overline{TXC}$ Low to $\overline{CTS}$ Invalid $\overline{CTS}$ Hold Time			10		ns	7 2	I
t75b	$\overline{CTS}$ High to $\overline{TXC}$ Low $\overline{CTS}$ Setup Time to Stop Trans.	25		20		ns	7 2	I
t72a	TXC Low to TENA High Time to Activate TENA				25	ns	5	A
t74a	TXC Low to TENA Low				25	ns	5	A
t75a	TXC Low to $\overline{CTS}$ Invalid $\overline{CTS}$ Hold Time			10		ns	7 2	A
t96	TENA Hold after TXC Low			5		ns		A

SERIAL A.C. TIMING CHARACTERISTIC VALUES (Continued)

Symbol	Parameter	16 MHz		20 MHz		Units	Notes	ESI
		Min	Max	Min	Max			
CRS, CDT PARAMETERS								
t77	$\overline{CDT}$, Low to $\overline{TXC}$ High External Coll. Detect Setup Time	25		20		ns		I
t78	$\overline{TXC}$ High to $\overline{CDT}$ Inactive $\overline{CDT}$ Hold Time	10		10		ns	14	I
t79	$\overline{CDT}$ Low to Jam Start					ns	10	I
t77a	CLSN High to TXC High External Coll.			20		ns	15	A
t78a	TXC High to CLSN Inactive CLSN Hold time			10		ns	14 15	A
t79a	CLSN High to Jam Start					ns	10, 15	A
t80	Jamming Period					ns	11	B
t81	$\overline{CRS}$ Low to $\overline{TXC}$ High Carrier Sense Setup Time	25		20		ns		I
t82	$\overline{TXC}$ High to $\overline{CRS}$ Inactive $\overline{CRS}$ Hold Time	10		10		ns	14	I
t81a	RENA High to TXC High Carrier Sense Setup time			20		ns	15	A
t82a	TXC High to RENA Inactive RENA Hold Time			10		ns	14	A
t83	$\overline{CRS}$ High to Jamming Start (Internal Collision Detect)					ns	12	B
CRS, CDT PARAMETERS								
t84	$\overline{CRS}$ High to $\overline{RXC}$ High $\overline{CRS}$ Inactive Setup Time	35		30		ns		I
t85	$\overline{RXC}$ High to CRS High $\overline{CRS}$ Inactive Hold Time	10		10		ns		I
t84a	RENA Low to RXC High RENA Inactive Setup Time			10		ns	15	A
t85a	RXC High to RENA Low RENA Inactive Hold Time			10		ns	15	A

SERIAL A.C. TIMING CHARACTERISTIC VALUES (Continued)

Symbol	Parameter	16 MHz		20 MHz		Units	Notes	ESI
		Min	Max	Min	Max			
RECEIVE CLOCK PARAMETERS								
t86	$\overline{RXC}$ Rise Time		4		5	ns	1	B
t87	$\overline{RXC}$ Fall time		4		5	ns	1	B
t88	$\overline{RXC}$ High Time	23		19		ns	1	B
t89	$\overline{RXC}$ Low Time	23		18		ns	1	B
RECEIVE DATA PARAMETERS								
t90	RXD Setup Time	15		15		ns		I
t91	RXD Hold Time	15		15		ns		I
t90a	RX Setup Time	12		12		ns	15	A
t91a	RX Hold Time	10		10		ns	15	A
t92a	RXD Rise Time		10		10	ns		B
t93	RXD Fall Time		10		10	ns		B
EXTERNAL LOOP BACK PIN PARAMETERS								
t109	$\overline{TXC}$/ Low to ELPBCK Valid		35		35	ns	4	B
t110	$\overline{TXC}$/ Low to ELPBCK Float		35		35	ns	4	B

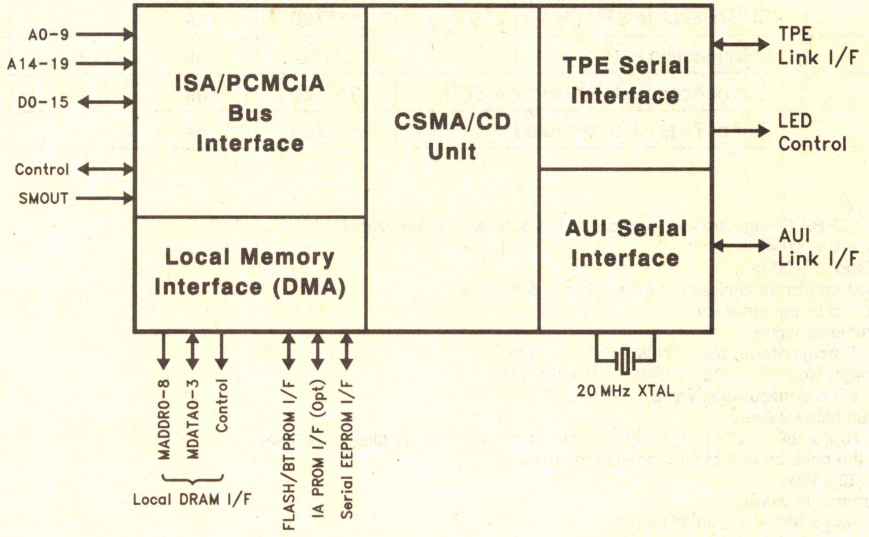
Symbol	Parameter	Min	Max	Units	Notes	ESI
INTERFRAME SPACING PARAMETERS						
t76	Inter Frame Delay				9	B
t97	CRS/RENA to SFD Min	8Trcy	11*T60	ns		B
t98	CRS Inactive to Active		8*T60	ns		B
t99	End of Accepted RCV to Next SFD		34*T60	ns		B
t100	End of Tx to CRS Accepted		42*T60	ns		B

NOTES:
1. MOS levels.
2. CTS and LPBK timings are independent of the polarity of these signals.
4. 1 TTL load + 50 pF.
5. 1 TTL load + 100 pF.
7. Abnormal end to transmission: CTS expires before RTS.
8. Normal end to transmission.
9. Programmable value:
   For non-Foreign Mode: t76 = Nifs x t60 (ns)
   For Foreign Mode: t76 = (Nifs + 1) x t60 (ns)
   Nifs—the IFS configuration value.
10. Programmable value:
    t79 = N_{cdf} x t60 + (12 to 15) x t60 (ns) (if collision occurs after preamble)
    N_{cdf}—the collision detect filter configuration value.
11. t80 = 32 x t60
12. Programmable value:
    t83 = N_{csf} x t60 + (12 to 15) x t60
14. To guarantee recognition on the next clock.
15. For 10 Mb/s SIA, TxC and RxC are both 10 MHz.

ESI—I: INTEL 82C501
A: AMD 7992B (Foreign Mode)
B: Applies to both

82595
ISA/PCMCIA HIGH INTEGRATION ETHERNET CONTROLLER

- **Optimal Integration for Lowest Cost Solution**
  - — Glueless 8-Bit/16-Bit ISA/PCMCIA 2.0 Bus Interface
  - — Provides Fully 802.3 Compliant AUI and TPE Serial Interface
  - — Local DRAM Support up to 64 Kbytes
  - — FLASH/EPROM Boot Support
  - — Hardware and Software Portable between Motherboard, Adapter, and PCMCIA IO Card Solution
- **High Performance Networking Functions**
  - — 16-Bit IO Accesses to Local DRAM with Zero Added Wait-States
  - — Ring Buffer Structure for Continuous Frame Reception and Transmit Chaining
  - — Automatic Retransmission on Collision
  - — Automatically Corrects TPE Polarity Switching Problems
- **Low Power CHMOS IV Technology**
- **Ease of Use**
  - — Design Time Reduced by High Integration
  - — EEPROM Interface to Support Jumperless Design
  - — Software Structures Optimized to Reduce Processing Steps
  - — Automatically Maps into Unused PC IO Location to Help Eliminate LAN Setup Problems
  - — All Software Structures Contained in One 16-Byte IO Space
  - — Automatic or Manual Switching between TPE and AUI Ports
  - — JTAG Port for Reduced Board Testing Times
- **Power Management**
  - — SL Compatible $\overline{\text{SMOUT}}$ Power Down Input
  - — Software Power Down Command for non-SL Systems
- **144-Lead tQFP Package Provides Smallest Available Form Factor**
  (See Packaging Spec., Order No. 240800)



290458-1

Figure 1. 82595 Block Diagram

October 1993
Order Number: 290458-003

82595
ISA/PCMCIA High Integration Ethernet Controller

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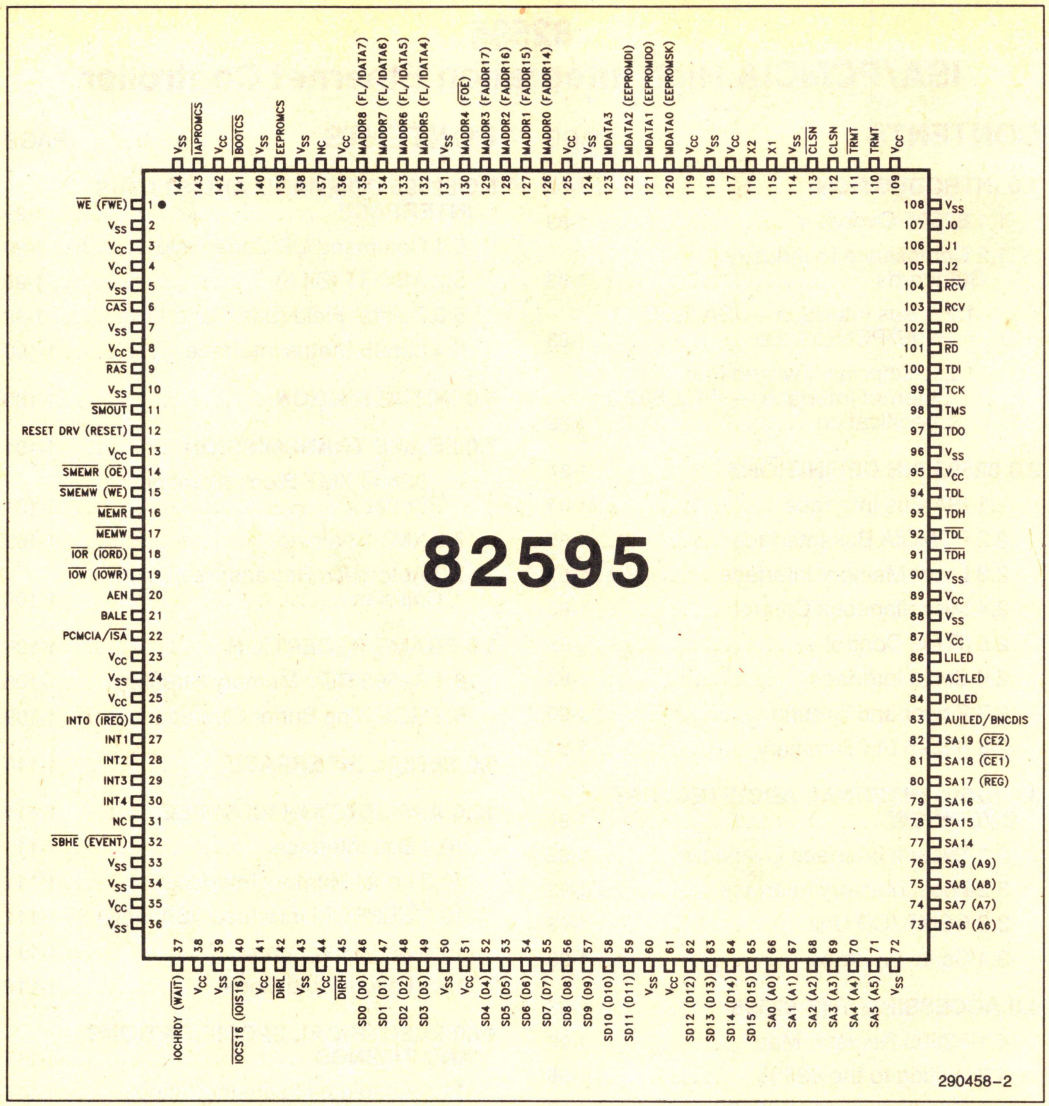


Figure 2. 82595 Pinout

1.0 INTRODUCTION

1.1 82595 Overview

The 82595 is a highly integrated LAN controller which provides a cost effective LAN solution for ISA compatible Personal Computer (PC) motherboards (both desktop and portable), add-on ISA adapter boards, and PCMCIA IO cards. The 82595 integrates all of the major functions of a buffered LAN solution into one chip with the exception of the local buffer memory which is implemented by adding one DRAM component to the LAN solution. The 82595's bus interface is a glueless attachment to either an ISA or PCMCIA version 2.0 bus. Its serial interface provides a Twisted Pair Ethernet (TPE) and an Attachment Unit Interface (AUI) connection. By integrating the majority of the LAN solution functions into one cost effective component, production cost savings can be achieved as well as significantly decreasing the design time for a solution. This level of integration also allows an 82595 solution to be ported between different applications (PC motherboards, adapters, and PCMCIA IO cards), while maintaining a compatible hardware and software base. This results in further savings in both hardware and software development costs for manufacturers expanding into different applications i.e., an ISA adapter vendor moving into producing PCMCIA IO cards, etc.

The 82595's software interface is optimized to reduce the number of processing steps that are required to interface to the 82595 solution. The 82595's initialization and control registers are directly addressable within one 16 byte IO address block. The 82595 can automatically resolve any conflicts to an IO block by moving its IO offset to an unused location in the case that a conflict occurs. The 82595's local memory is arranged in a simple ring buffer structure for efficient transfer of transmit and receive packets. The local memory, up to 64 Kbytes of DRAM, resides as an IO port in the host system's IO map. The 82595 provides direct control over the local DRAM, including refresh. The 82595 performs a prefetch to the DRAM memory allowing CPU IO cycles to this data with no added wait-states. The 82595 also provides an interface to up to 256 Kbytes of FLASH or EPROM memory. An interface to an EEPROM, which holds solution configuration values and also can contain the Node ID, allows for the implementation of a "jumperless" design.

The 82595's packaging and power management features are designed to consume minimal board real estate and system power. This is required for applications such as portable PC motherboard designs and PCMCIA IO cards which require a solution with very low real estate and power consumption. The 82595 package is a 144-lead tQFP (thin Quad Flat Pack). Its dimensions are 20mm by 20mm, and 1.7mm in height (roughly the same area as a US Nickel, and the same height as a US Dime). The 82595 contains two power down modes; an SL compatible power down mode which utilizes the SL SMOUT input, and a POWER DOWN command for non-SL systems.

1.2 Compliance to Industry Standards

The 82595 has two interfaces; the host system interface, which is an ISA or PCMCIA bus interface, and the serial, or network interface. Both interfaces have been standardized by the IEEE.

1.2.1 BUS INTERFACE—ISA IEEE P996/ PCMCIA 2.0

The 82595 implements the full ISA bus interface. It is compatible with the IEEE spec P996. The 82595 also interfaces to ISA bus implementations that deviate from the IEEE spec by requiring early assertion of the IOCHRDY signal and alternate host address decode timing. This alternate timing can be configured in the 82595 after a software test which is run at initialization time. The 82595 can also be configured for a PCMCIA bus interface depending on the state of the PCMCIA/ISA input pin. In this case the 82595 implements the complete PCMCIA interface, compatible to the PCMCIA revision 2.0 specification.

1.2.2 ETHERNET/TWISTED PAIR ETHERNET INTERFACE—IEEE 802.3 SPECIFICATION

The 82595's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop providing a fully compliant IEEE 802.3 AUI interface. The TPE port provides a fully compliant IEEE 10BASE-T interface. The 82595 can automatically switch to whichever port (TPE or AUI) is active.

2.0 82595 PIN DEFINITIONS

2.1 ISA Bus Interface

The ISA bus interface consists of three sections: an Address Bus, a Data Bus, and a Control section.

Symbol	Pin No.	Type	Name and Function
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9	66 67 68 69 70 71 73 74 75 76	I	**ADDRESS BUS:** These pins provide address decoding for up to 1 Kbyte of address.
SA14 SA15 SA16 SA17 SA18 SA19	77 78 79 80 81 82	I	**ADDRESS BUS:** These pins provide address decoding between the 16 Kbyte and 1 Mbyte memory space. This allows for decoding of a Boot EPROM or a FLASH in 16K increments.
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15	46 47 48 49 52 53 54 55 56 57 58 59 62 63 64 65	I/O	**DATA BUS:** This is the data interface between the 82595 and the host system. This data is buffered by one (8-bit design) or two (16-bit design) transceivers. The 82595's data lines should always be connected to the B side of the data bus transceiver.
AEN	20	I	**ADDRESS ENABLE:** Active high signal, indicates a DMA cycle is active.
BALE	21	I	**BUFFERED ADDRESS LATCH ENABLE:** Falling edge used to latch a valid system address.
$\overline{\text{SMEMR}}$	14	I	**MEMORY READ** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{SMEMW}}$	15	I	**MEMORY WRITE** for system memory accesses below 1 Mbyte. Active low.
$\overline{\text{MEMR}}$/ 8/16 Detect	16	I	**MEMORY READ** for system memory accesses above or below 1 Mbyte. Active low. This pin also determines if the 82595 is operating in an 8- or 16-bit system. For 16-bit systems, it should always be connected.
$\overline{\text{MEMW}}$	17	I	**MEMORY WRITE** for system memory accesses above or below 1 Mbyte. Active low.
$\overline{\text{IOR}}$	18	I	**IO READ:** Active low.

2.1 ISA Bus Interface (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{IOW}$	19	I	**IO WRITE:** Active low.
$\overline{IOCS16}$	40	O	**IO CHIP SELECT 16:** Active low, open drain output which indicates that an IO cycle access to the 82595 solution is 16-bit wide. Driven for IO cycles to the local memory or to the 82595.
IOCHRDY	37	O	**IO CHANNEL READY:** Active high, open drain output. When driven low, it extends host cycles to the 82595 solution.
$\overline{SBHE}$	32	I	**SYSTEM BUS HIGH ENABLE:** Active low input indicates a data transfer on the high byte (D8–D15) of the system bus (a 16-bit transfer).
INT0 INT1 INT2 INT3 INT4	26 27 28 29 30	O	**82595 INTERRUPT 0–4:** One of these five pins is selected to be active at a time (the other four are in Hi-Z state) by configuration. These active high outputs serve as interrupts to the host system.
RESET DRV	12	I	**RESET DRIVE:** Active high reset signal.

2.2 PCMCIA Bus Interface

The PCMCIA bus interface consists of three sections: an Address Bus, a Data Bus, and a Control section.

Symbol	Pin No.	Type	Name and Function
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9	66 67 68 69 70 71 73 74 75 76	I	**ADDRESS BUS:** These pins provide IO address decoding for up to 1 Kbyte.
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	46 47 48 49 52 53 54 55 56 57 58 59 62 63 64 65	I/O	**DATA BUS:** This is the data interface between the 82595 and the host system.

2.2 PCMCIA Bus Interface (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{OE}$	14	I	**OUTPUT ENABLE (Memory Read):** Active low.
$\overline{WE}$	15	I	**WRITE ENABLE (Memory Write):** Active low.
$\overline{IORD}$	18	I	**IO READ:** Active low.
$\overline{IOWR}$	19	I	**IO WRITE:** Active low.
$\overline{IOIS16}$	40	O	**IO IS 16:** Active low output which indicates that an IO cycle access to the 82595 solution is 16-bit wide. $\overline{IOIS16}$ should be asserted prior to Card Enable or CMD ($\overline{IORD}$ or $\overline{IOWR}$) assertion.
$\overline{WAIT}$	37	O	**WAIT:** Active low output when driven low, extends host cycles to the 82595.
$\overline{IREQ}$	26	O	**82595 INTERRUPT:** Active low output.
RESET	12	I	**RESET:** Active high reset signal.
$\overline{CE1}$ $\overline{CE2}$	81 82	I	**Card Enable 1** and **Card Enable 2** are active low signals driven by the host. These signals provide a card select based on an address decode (decode done by the host) and also byte lane enables. When both $\overline{CE1}$ and $\overline{CE2}$ are high, no host accesses are made to the card. If $\overline{CE1}$ is low (active) and CE2 is high (inactive), the device operates in byte access mode with valid data being driven on D0–D7 and A0 determines the selection of an odd or even byte. When both $\overline{CE1}$ and $\overline{CE2}$ are low, a word access is taking place. In this case A0 is ignored, and the data is transferred on D0–D15. Odd-byte-only accesses can occur when $\overline{CE1}$ is high and $\overline{CE2}$ is low. In this case the data is driven on D8–D15 and A0 is ignored. See Section 4.9 for a summary of the PCMCIA decode functions.
$\overline{REG}$	80	I	$\overline{REG}$ is an active low input used to determine whether a host access is to Attribute memory (the 1st 1K of FLASH or CONF Regs) or to Common memory (FLASH above 1K). If $\overline{REG}$ is low the access is to Attribute memory, if $\overline{REG}$ is high the access is to Common memory. $\overline{REG}$ is also asserted low for all accesses to the 82595's IO Registers (including the access to the local DRAM via the 82595's Local Memory IO Port). See Section 4.9 for a summary of the PCMCIA decode functions.
$\overline{EVENT}$	32	O	$\overline{EVENT}$ is an active low output which, when enabled, will be asserted whenever a frame has been received by the 82595. This allows the 82595 to "wake up" a system which has powered down (with the exception of powering down the LAN). This output will remain asserted until the 82595's RCV Interrupt (for the frame which woke up the system) has been acknowledged.

2.3 Local Memory Interface

Symbol	Pin No.	Type	Name and Function
MADDR0 MADDR1 MADDR2 MADDR3 MADDR4 MADDR5 MADDR6 MADDR7 MADDR8	126 127 128 129 130 132 133 134 135	O	**LOCAL MEMORY ADDRESS (MADDR0–MADDR8):** These outputs contain the multiplexed address for the local DRAM.
MDATA0 MDATA1 MDATA2 MDATA3	120 121 122 123	I/O	**LOCAL DATA BUS (MDATA0–MDATA3):** The four I/O signals, comprising the local data bus, are used to read or write data to or from the 4-bit wide DRAM. These signals also provide the lower 4 bits of data for accesses to an 8-bit FLASH/EPROM or IA PROM if these components are used.
$\overline{RAS}$	9	O	This active low output is the **Row Address Strobe** signal to the DRAM.
$\overline{CAS}$	6	O	This active low output is the **Column Address Strobe** signal to the DRAM.
$\overline{WE}$	1	O	This active low output is the **Write Enable** to the DRAM.
FADDR14 FADDR15 FADDR16 FADDR17	126 127 128 129	O	**FLASH ADDRESS 14–17 :** These pins control the FLASH addressing from 16K to 256K to allow paging of the FLASH in 16K spaces. These addresses are under direct control of the FLASH PAGING configuration register. **NOTE:** ISA Bus I/F Only
$\overline{FOE}$	130	O	This output provides the active low **Output Enable** control to the **FLASH.**
$\overline{FWE}$	1	O	This output provides the active low **Write Enable** control to the **FLASH.**
$\overline{BOOTCS}$	141	O	**BOOT EPROM/FLASH $\overline{CS}$**
$\overline{IAPROMCS}$	143	O	**IA PROM $\overline{CS}$**
FL/IADATA4 FL/IADATA5 FL/IADATA6 FL/IADATA7	132 133 134 135	I/O	Provides the upper 4 bits of an 8 bit data path for both the Boot EPROM/ FLASH and IA PROM, for CPU accesses.
EEPROMCS	139	I/O	**EEPROM CS:** Active high signal. If no EEPROM is connected, this pin should be connected to V_{CC}. In this case it will function as an input to the 82595 to indicate no EEPROM is connected.
EEPROMSK	120	O	**EEPROM SHIFT CLOCK:** This output is used to shift data into and out of the serial EEPROM.
EEPROMDO	121	I	**EEPROM DATA OUT**
EEPROMDI	122	O	**EEPROM DATA IN**

2.4 Miscellaneous Control

Symbol	Pin No.	Type	Name and Function
$\overline{DIRL}$	42	O	**DIRECTION LOW:** Controls the direction of the low byte data bus transceiver. The direction defaults to always point in from the ISA bus to the 82595 ($\overline{DIRL}$ = 1). This direction is turned around (82595 out to ISA bus, $\overline{DIRL}$ = 0) only in the case of a read access to the 82595 based solution.
$\overline{DIRH}$	45	O	**DIRECTION HIGH:** Controls the direction of the high byte data bus transceiver. The direction defaults to always point in from the ISA bus to the 82595 ($\overline{DIRH}$ = 1). This direction is turned around (82595 out to ISA bus, $\overline{DIRH}$ = 0) only in the case of a read access to the 82595 based solution. This signal is active for 16-bit accesses only.
$\overline{SMOUT}$	11	I/O	This active LOW signal, when asserted, places the 82595 into a Power Down mode. The 82595 will remain in power down mode until $\overline{SMOUT}$ is unasserted. If this line is unconnected to $\overline{SMOUT}$ from the system bus, it can be used as an active low output which, when a POWER DOWN command is issued to the 82595, can be used to power down other external components (this output function is enabled by configuration).
PCMCIA/$\overline{ISA}$	22	I	This pin, when strapped low, selects an ISA bus interface. Strapped high selects PCMCIA.
J0 J1 J2	107 106 105	I	**JUMPER** input for selecting between 7 IO spaces (also selects whether the IO location should be read from the EEPROM). These pins should be connected to either V_{CC} or GND. The 82595 reads the Jumper block during its initialization sequence. **J0 J1 J2 IO Address** GND GND GND Address Contained in EEPROM V_{CC} GND GND 2A0h GND V_{CC} GND 280h V_{CC} V_{CC} GND 340h GND GND V_{CC} 300h V_{CC} GND V_{CC} 360h GND V_{CC} V_{CC} 350h V_{CC} V_{CC} V_{CC} 330h

2.5 JTAG Control

Symbol	Pin No.	Type	Name and Function
TDO	97	O	**JTAG TEST DATA OUT**
TMS	98	I	**JTAG TEST MODE SELECT**
TCK	99	I	**JTAG TEST CLOCK**
TDI	100	I	**JTAG TEST DATA IN**

2.6 Serial Interface

Symbol	Pin No.	Type	Name and Function
TRMT	110	O	Positive side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out A).
$\overline{\text{TRMT}}$	111	O	Negative side of the differential output driver pair that drives 10 Mb/s Manchester Encoded data on the TRMT pair of the AUI cable (Data Out B).
RCV	103	I	The positive input to a differential amplifier connected to the RCV pair of the AUI cable (Data In A). It is driven with 10 Mb/s Manchester Encoded data.
$\overline{\text{RCV}}$	104	I	The negative input to a differential amplifier connected to the RCV pair of the AUI cable (Data In B). It is driven with 10 Mb/s Manchester Encoded data.
CLSN	112	I	The positive input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In A).
$\overline{\text{CLSN}}$	113	I	The negative input to a differential amplifier connected to the CLSN pair of the AUI cable (Collision In B).
TDH	93	O	**TRANSMIT DATA HIGH:** Active high Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, $\overline{\text{TDH}}$, and $\overline{\text{TDL}}$ to generate the pre-conditioned twisted pair output waveform.
TDL	94	O	**TRANSMIT DATA LOW:** Twisted Pair Output Driver. Active high Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDH, $\overline{\text{TDH}}$, and $\overline{\text{TDL}}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{\text{TDH}}$	91	O	**TRANSMIT DATA HIGH INVERT:** Twisted Pair Output Driver. Active low Manchester Encoded data to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{\text{TDL}}$ to generate the pre-conditioned twisted pair output waveform.
$\overline{\text{TDL}}$	92	O	**TRANSMIT DATA LOW INVERT:** Twisted Pair Output Driver. Active low Manchester Encoded data with embedded pre-distortion information to be transmitted onto the twisted pair. This signal is used in conjunction with TDL, TDH, and $\overline{\text{TDH}}$ to generate the pre-conditioned twisted pair output waveform.
RD	102	I	Active high Manchester Encoded data received from the twisted pair.
$\overline{\text{RD}}$	101	I	Active low Manchester Encoded data received from the twisted pair.
X1	115	I	**20 MHz CRYSTAL INPUT:** This pin can be driven with an external MOS level clock when X2 is left floating. This input provides the timing for all of the 82595 functional blocks.
X2	116	O	**20 MHz CRYSTAL OUTPUT:** If X1 is driven with an external MOS level clock, X2 should be left floating.

2.6 Serial Interface (Continued)

Symbol	Pin No.	Type	Name and Function
AUI LED/BNC DIS	83	O	**AUI LED INDICATOR:** This output, when the 82595 is used for as a TPE/AUI solution, will turn on an LED when the 82595 is actively interfaced to its AUI serial port. When the 82595 is used as a BNC/AUI solution, this output becomes the **BNC DIS** output, which can be used to power down the BNC Transceiver section (the Transceiver and the DC to DC Converter) of the solution when the BNC port is unconnected.
LILED	86	O	**LINK INTEGRITY LED:** Normally on (low) ouput which indicates a good link integrity status when the 82595 is connected to an active TPE port. This output will remain on when the Link Integrity function has been disabled. It turns off (driven high) when Link Integrity fails, or when the 82595 is actively interfaced to an AUI port. The minimum off time is 100 ms.
ACTLED	85	O	**LINK ACTIVITY LED:** Normally off (high) output turns on to indicate activity for transmission, reception, or collision. Flashes at a rate dependent on the level of activity on the link.
POLED	84	O	**POLARITY LED:** If the 82595 detects that the receive TPE wires are reversed, POLED will turn on (low) to indicate the fault. POLED remains on even if automatic polarity correction is enabled, and the 82595 has automatically corrected for the reversed wires.

2.7 Power and Ground

Symbol	Pin No.	Type	Name and Function
V_{CC}	3, 4, 8, 13, 23, 25, 35, 38, 41, 44, 51, 61, 87, 89, 95, 109, 117, 119, 125, 136, 142	I	**POWER**: +5V ±5%.
V_{SS}	2, 5, 7, 10, 24, 33, 34, 36, 39, 43, 50 60, 72, 88, 90, 96, 108, 114, 118, 124, 131, 138, 140, 144	I	**GROUND**: 0V.

2.8 82595 Pin Summary

ISA/PCMCIA Bus Interface

ISA Pin Name	MUXed PCMCIA Pin Name	Pin Type	P-Down State
SA0–SA9 (In)	A0–A9 (In)		Inactive
SA14–16 (In)			Inactive
SA17 (In)	$\overline{REG}$ (In)		Inactive/Act(1)
SA18 (In)	$\overline{CE1}$ (In)		Inactive/Act(1)
SA19 (In)	$\overline{CE2}$ (In)		Inactive
SD0–SD15 (I/O)	D0–D15 (I/O)	TS	TS
$\overline{SMEMR}$ (In)	$\overline{OE}$ (In)		Inactive
$\overline{SMEMW}$ (In)	$\overline{WE}$ (In)		Inactive
$\overline{IOR}$ (In)	$\overline{IORD}$ (In)		Inactive
$\overline{IOW}$ (In)	$\overline{IOWR}$ (In)		Inactive/Act(1)
INT0 (Out)	$\overline{IREQ}$ (Out)	TS	TS
INT1–4 (Out)		TS	TS
RESET DRV (In)	RESET (In)		Act
$\overline{IOCS16}$ (Out)	$\overline{IOIS16}$ (Out)	OD/TS	TS
BALE (In)			Inactive
IOCHRDY (Out)	$\overline{WAIT}$ (Out)	OD/2S	TS
$\overline{SBHE}$ (In)	$\overline{EVENT}$ (Out)	2S	Inactive/TS
AEN (In)			Inactive/Act(1)
$\overline{MEMR}$ (In)			Inactive
$\overline{MEMW}$ (In)			Inactive

NOTE:
1. For hardware powerdown using $\overline{SMOUT}$, these pins will be inactive. For software powerdown, these pins remain active.

Local Memory Interface

Pin Name	MUXed Pin Name	Pin Type	P-Down State
MADDR0–3 (Out)	FADDR14–17 (Out)	2S	TS
MADDR4 (Out)	$\overline{FOE}$ (Out)	2S	TS
MADDR5–8 (Out)	FL/IADATA4–7 (In)	TS	TS
MDATA0 (I/O)	EEPROMSK (Out)	TS	TS
MDATA1 (I/O)	EEPROMDO (In)	TS	TS
MDATA2 (I/O)	EEPROMDI (Out)	TS	TS
MDATA3 (I/O)		TS	TS
$\overline{WE}$ (Out)	$\overline{FWE}$ (Out)	2S	TS
$\overline{RAS}$ (Out)		2S	PU
$\overline{CAS}$ (Out)		2S	PU
$\overline{BOOTCS}$ (Out)		2S	PU
$\overline{IAPROMCS}$ (Out)		2S	PU
EEPROMCS (I/O)		TS	PD

Miscellaneous Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State
$\overline{DIRL}$ (Out)		2S	PU
$\overline{DIRH}$ (Out)		2S	PU
J0–J2 (In)			
$\overline{SMOUT}$ (I/O)		TS	ACT/TS
PCMCIA/$\overline{ISA}$ (In)			ACT

JTAG Control

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TMS (In)			In Act
TCK (In)			In Act
TDI (In)			In Act
TDO (Out)		2S	

Serial Interface

Pin Name	MUXed Pin Name	Pin Type	P-Down State
TRMT (Out)		Ana	TS
$\overline{TRMT}$ (Out)		Ana	TS
RCV (In)		Ana	In Act
$\overline{RCV}$ (In)		Ana	In Act
CLSN (In)		Ana	In Act
$\overline{CLSN}$ (In)		Ana	In Act
TDH (Out)		Ana	TS
TDL (Out)		Ana	TS
$\overline{TDH}$ (Out)		Ana	TS
$\overline{TDL}$ (Out)		Ana	TS
RD (In)		Ana	In Act
$\overline{RD}$ (In)		Ana	In Act
X1 (In)			In Act
X2 (Out)		2S	TS
LILED (Out)		2S	TS
POLED (Out)		2S	TS
ACTLED (Out)		2S	TS
AUILED (Out)	BNC DIS (Out)	2S	TS

Legend:
TS—TriState.
OD—Open Drain.
2S—Two State, will be found in either a 1 or 0 logic level.
Ana—Analog pin (all serial interface signals).
Act—Input buffer is active during Power Down.
In Act—Input buffer is inactive during Power Down.
PU—Output in inactive state with weak internal Pullup during Power Down.
PD—Output in inactive state with weak internal Pulldown during Power Down.

3.0 82595 INTERNAL ARCHITECTURE OVERVIEW

Figure 1 shows a high level block diagram of the 82595. The 82595 is divided into four main subsections; a system interface, a local memory subsystem interface, a CSMA/CD unit, and a serial interface.

3.1 System Interface Overview

The 82595's system interface subsection includes a glueless ISA or PCMCIA bus interface (selectable by strapping), and the 82595's IO registers (including the 82595's command, status, and Data In/Out registers). The system interface block also interfaces with the 82595's local memory interface subsystem and CSMA/CD subsystem.

The bus interface logic provides the control, address, and data interface to either an ISA compatible or a PCMCIA revision 2.0 bus. The 82595 decodes up to 1M of memory address space within 16K block increments (A0–9, A14–19). It decodes IO accesses throughout the 1 Kbyte PC IO address range. The 82595 data bus interface provides either an 8- or 16-bit interface to the host system's data bus. The control interface provides complete handshaking interface with the system bus to enable transfer of data between the 82595 solution and the host system. This logic also controls the direction of the Data Bus transceivers.

The 82595's IO registers provide 3 banks of directly addressable registers which are used as the control and data interface to the 82595. There are 16 IO registers per bank, with only one bank enabled at a time. This allows the complete 82595 software interface to be contained in one 16-byte IO space. The base address of this IO space is selectable via either software (which can be stored in a serial EEPROM interfaced to the 82595), or by strapping the 82595 IO Jumper block (J0–J2). The 82595 can also detect conflicts to its base IO space, and automatically resolve these conflicts by mapping itself into an unused IO space. Included in the 82595 IO register set are the Command Register, the Status Register, and the Local Memory IO Port register which provides the data interface to the local DRAM buffer contained in an 82595 solution. Functions such as IO window mapping, Interrupt enable, RCV and XMT buffer initialization, etc. are also configured and controlled through the IO registers.

3.2 Local Memory Interface

The 82595's local memory interface includes a DMA unit which controls data transfers to or from the 82595 solutions local DRAM, control for access to an IA PROM and a Boot EPROM/FLASH, and an interface to a serial EEPROM. The local memory interface subsection also arbitrates accesses to the local memory by the host CPU and the 82595.

Data transfers between the 82595 and the local DRAM are always through the 82595's Local Memory IO Port. This allows the entire DRAM memory (up to 64 Kbytes) to be mapped into one IO location in the host systems IO map. The CPU always accesses this port for Receive or Transmit data transfers, while the 82595 automatically increments the address to the DRAM after each CPU access. The DRAMs data path is a 4-bit interface (typically 64K by 4-bits wide, or 256K by 4-bits wide) to allow for the lowest possible solution cost. The 82595 implements a prefetch mechanism to the local DRAM so that the data is always available to the CPU as either an 8- or 16-bit word. In the case of the CPU reading from the DRAM, the 82595 reads the next four 4-bit nibbles from the DRAM between CPU cycles so that the data is always available as a word in the 82595's Local Memory IO Port register. In the case of the CPU writing to the DRAM, the data is written into the 82595's Local Memory IO Port and then transfered to the DRAM by the 82595 between CPU cycles. This prefetch mechanism of the 82595 allows for IO reads and writes to the local memory to be performed with no additional wait-states (3 clocks per data transfer cycle).

The DMA unit provides addressing and control to move RCV or XMT data between the 82595 and the local DRAM. For transmission, the CPU is required only to copy the data to the local memory, initialize the 82595's DMA Current Address Register (CAR) to point to the beginning of the frame, and issue a Transmit command to the 82595. The DMA unit facilitates the transfers from the local memory to the 82595 as transmission takes place. The DMA unit will reset upon collision during a transmission, enabling automatic retransmission of the transmit frame. During reception, the DMA unit implements a recyclable ring buffer structure which can receive continuous back to back frames without CPU intervention on a per frame basis.

The 82595 provides address decoding and control to allow access to an external Boot EPROM/FLASH or an IA PROM if these components are utilized in a 82595 design. The 82595 also provides a complete interface to a serial EEPROM. The EEPROM is used to store configuration information such as IO Mapping Window, Interrupt line selection, etc. The EEPROM can be used to replace jumper blocks which previously contained this information.

The 82595 arbitrates accesses to the local memory subsystem by the CPU and the 82595. The arbitration unit will hold off a 82595 DMA cycle to the local memory if a CPU cycle is already in progress. Likewise, it will hold off the CPU if a 82595 cycle is al-

ready in progress. The cycle which is held off will be completed on termination of the preceding cycle.

3.3 CSMA/CD Unit

The CSMA/CD unit implements the IEEE 802.3 CSMA/CD protocol. It performs such functions as transmission deferral to link traffic, interframe spacing, exponential backoff for collision handling, address recognition, etc. The CSMA/CD unit serves as the interface between the local memory and the Serial interface. It serializes data transferred from the local memory before it is passed to the serial interface unit for transmission. During frame reception, it converts the serial data received from the serial interface to a byte format before it is transferred to the local memory. The CSMA/CD unit strips framing parameters such as the Preamble and SFD fields before the frame is passed to memory for reception. For transmission, the CSMA/CD unit builds the frame format before the frame is passed to the serial interface for transmission.

3.4 Serial Interface

The 82595's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also be interfaced to a transceiver device to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595 automatically enables either the AUI or TPE interface depending on which medium is connected to the chip. This automatic selection can be overridden by software configuration.

4.0 ACCESSING THE 82595

All accesses to the 82595 are made through one of three banks of IO registers. Each bank contains 16 registers. Each register in a bank is directly accessable via addressing. Through the use of bank switching, the 82595 utilizes only 16 IO locations in the host system's IO map to access each of its registers. The different banks are accessed by setting the POINTER field in the 82595 Command Register to select each bank. The Command Register is Register 0 for each bank.

4.1 82595 Register Map

The 82595 registers are contained in three banks of 16 IO registers per bank. These three banks are shown in the following three pages.

4.1.1 IO BANK 0

The format for IO Bank 0 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
RCV States		EXEC States		EXEC INT	TX INT	RX INT	RX STP INT	Reg 1
(Counter)		1	ID REGISTER (Auto En)	0	1	0 RESERVED		Reg 2
0 Resvrd	0 Resvrd	Base/ $\overline{\text{Cur}}$	0 Resvrd	EXEC Mask	TX Mask	RX Mask	RX STP Mask	Reg 3
RCV CAR/BAR (Low)								Reg 4
RCV CAR/BAR (High)								Reg 5
RCV STOP REG (Low)								Reg 6
RCV STOP REG (High)								Reg 7
0	0	0	0	0 (Reserved)	0	0	0	Reg 8
0	0	0	0	0 (Reserved)	0	0	0	Reg 9
XMT CAR/BAR (Low)								Reg 10
XMT CAR/BAR (High)								Reg 11
Host Address Reg (Low)							0	Reg 12
Host Address Reg (High)								Reg 13
Local Memory IO Port (Low)								Reg 14
Local Memory IO Port (High)								Reg 15

4.1.2 IO BANK 1

The format for IO Bank 1 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
Tri-ST INT	Alt RDY Tm	0 Resvrd	0 Resvrd	0 Resvrd	0 Resvrd	Host Bus Wd	0 Resvrd	Reg 1
0 Resvrd	Boot EPROM/FLASH Decode Window			0 Resvrd	INT Select			Reg 2
0	0	I/O Mapping Window						Reg 3
0	0	0	0	0	0	0	0	Reg 4
(Reserved)								
0	0	0	0	0	0	0	0	Reg 5
(Reserved)								
0	0	0	0	0	0	0	0	Reg 6
(Reserved)								
0	0	0	0	0	0	0	0	Reg 7
(Reserved)								
RCV LOWER LIMIT REG (High Byte)								Reg 8
RCV UPPER LIMIT REG (High Byte)								Reg 9
XMT LOWER LIMIT REG (High Byte)								Reg 10
XMT UPPER LIMIT REG (High Byte)								Reg 11
0	0	FLASH WRITE ENABLE		FLASH PAGE SELECT				Reg 12
0	0	0	0	0	$\overline{\text{SMOUT}}$ OUT EN	AL RDY TEST	AL RDY PAS/FL	Reg 13
0	0	0	0	0	0	0	0	Reg 14
(Reserved)								
0	0	0	0	0	0	0	0	Reg 15
(Reserved)								

1

4.1.3 IO BANK 2

The format for IO Bank 2 is shown below.

7	6	5	4	3	2	1	0	
POINTER		ABORT	COMMAND OP CODE					Reg 0 (CMD Reg)
Disc Bad Fr	Tx Chn $\overline{\text{ErStp}}$	Tx Chn Int Md	PCMCIA/ $\overline{\text{ISA}}$	0	0	0	0	Reg 1
LoopBack		Multi IA	No SA Ins	0	RX CRC $\overline{\text{InMem}}$	BC DIS	PRMSC Mode	Reg 2
Test1	Test2	BNC/ $\overline{\text{AUI}}$	$\overline{\text{APORT}}$	Jabber Disabl	TPE/ $\overline{\text{AUI}}$	Pol $\overline{\text{Corr}}$	Lnk In Dis	Reg 3
INDIVIDUAL ADDRESS REGISTER 0								Reg 4
INDIVIDUAL ADDRESS REGISTER 1								Reg 5
INDIVIDUAL ADDRESS REGISTER 2								Reg 6
INDIVIDUAL ADDRESS REGISTER 3								Reg 7
INDIVIDUAL ADDRESS REGISTER 4								Reg 8
INDIVIDUAL ADDRESS REGISTER 5								Reg 9
STEPPING			Trnoff Enable	EEDO	EEDI	EECS	EESK	Reg 10
RCV NO RESOURCE COUNTER								Reg 11
IAPROM IO Port								Reg 12
0	0	0	0	0	0	0	0	Reg 13
(Reserved)								
0	0	0	0	0	0	0	0	Reg 14
(Reserved)								
0	0	0	0	0	0	0	0	Reg 15
(Reserved)								

4.2 Writing to the 82595

Writing to the 82595 is accomplished by an IO Write instruction (such as an OUT instruction) from the host processor to one of the 82595 registers. The 82595 registers reside in a block of 16 contiguous addresses contained within the PC IO address space. The mapping of this address block is programmable throughout the 1 Kbyte PC IO address map.

The 82595 registers are contained within three banks of IO registers. When writing to a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once a bank is selected, all register accesses are made in that bank until a switch to another bank is performed. Switching banks is accomplished by writing to the PTR field of Reg 0 in any bank. Reg 0 is the command register of the 82595 and its functionality is identical in each bank. Once in the appropri-

ate bank, the processor can write directly to any of the 82595 registers by simply issuing an OUT instruction to the IO address of the register.

4.3 Reading from the 82595

Reading from the 82595 is accomplished by an IO Read instruction (such as an IN instruction) from the host processor to one of the 82595 registers. When reading from a particular register, the processor must first select the correct bank (Bank 0, 1 or 2) in which the register resides. Once in the appropriate bank, the processor can read directly from any of the 82595 registers by simply issuing an IN instruction to the IO address of the register.

4.4 Local DRAM Accesses

IO mapping the local DRAM memory of an 82595 solution allows it to appear as simply an IO Port to the host system. This allows an 82595 solution to work in PCs which do not have enough space in their system memory map to accommodate the addition of LAN buffer memory (typically 16 Kbytes to 64 Kbytes) into the map. The entire local memory (up to 64 Kbytes) is mapped into one 16-bit IO Port location. For all IO mapped accesses to the local memory of a 82595 solution, the 82595 performs the IO address decoding, the ISA Bus interface handshake, and asserts the address and control signals to the local memory.

4.4.1 WRITING TO LOCAL MEMORY

The local memory of a 82595 solution is written to whenever the host CPU performs a Write operation to the 82595 Local Memory IO Port. Prior to writing a block of data to the local memory, the CPU should update the 82595 Host Address Register with the first address to be written. The CPU then copies the data to the local memory by writing it to the 82595 Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82595 upon completion of each write cycle. This allows sequential accesses to the local memory, even though the IO port address accessed does not change.

4.4.2 READING FROM LOCAL MEMORY

The local memory of a 82595 solution is read from whenever the host CPU performs a Read operation from the 82595 Local Memory IO Port. Prior to reading a block of data from the local memory, the CPU should utilize the 82595 Host Address Register to point to first address to be read. The CPU then reads the data from the local memory through the 82595 Local Memory IO Port. The addressing to the local memory is provided by the Host Address Register which is automatically incremented by the 82595 upon completion of each read cycle.

4.5 Serial EEPROM Interface

The Serial EEPROM, a Hyundai HY93C46 or equivalent IC, stores configuration data for the 82595. The use of an EEPROM enables 82595 designs to be implemented without jumpers (the use of jumpers to select IO windows is optional). The EEPROM contains solution configuration parameters that are typically specified by jumper blocks such as IO Mapping Window, Interrupt Selects, etc.

The 82595 automatically accesses Register 0 of the EEPROM upon a RESET in ISA Bus Interface mode. Register 0 contains the information that the 82595 must be configured with to allow CPU accesses to it (IO Mapping Window, Boot EPROM/FLASH Window, and Host Bus Width) following a system Boot. The format for EEPROM Register 0 is as follows. Note that all 0's are assumed to be reserved.

EEPROM Register 0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IO Mapping Window						0	0	0	Auto	BT/FLSH Window			Hst	0	0
MSb					LSb				I/O En	MSb		LSb	Wdt		

4.6 Boot EPROM/FLASH Interface

The Boot EPROM/FLASH of a 82595 solution is read from or written to (FLASH only) whenever the host CPU performs a Read or a Write operation to a memory location that is within the Boot EPROM/FLASH mapping window. This window is programmable throughout the ISA PROM address range (C8000–DFFFF) by configuring the 82595 Boot EPROM Decode Window register (Bank 1, Register 2, bits 4–6). The 82595 asserts the BT/FLSHCS signal when it decodes a valid access. Boot EPROM/FLASH decodes are disabled by programming the Boot EPROM/FLASH Decode Window register to a value of either 000 or 001 (binary).

4.7 IA PROM Interface

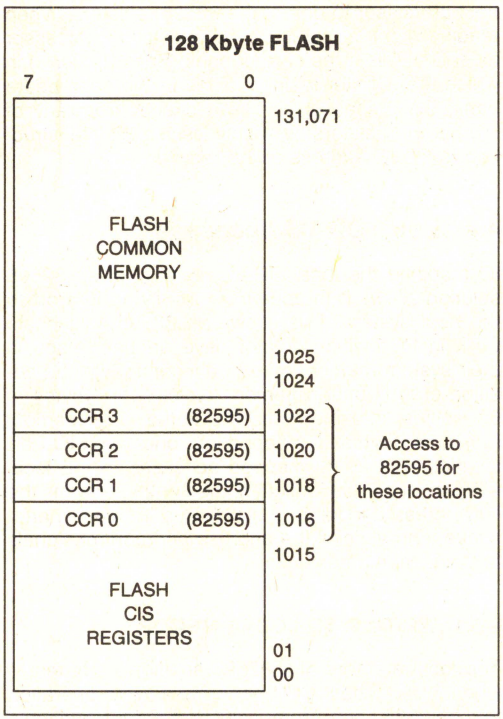
The 82595 supports an IA PROM interface. Implementation of an IA PROM in a 82595 solution is optional. The IA can also be stored in the serial EEPROM. In this case the IA PROM is not needed.

4.8 PCMCIA CIS Structures

The 82595 supports access to 1K of Attribute Memory when configured for PCMCIA support. Attribute memory is defined by the PCMCIA standard to be comprised of the Card Information Structure (FLASH memory referred to as CIS residing at memory offset 0 to 1015:decimal) and 4 8-bit Card Configuration Registers which reside at memory offset 1016 to 1022 on even boundaries only (1016, 1018, 1020, 1022). These four registers are contained in the 82595. They are memory mapped, and are accessed when $\overline{CE1}$ and $\overline{REG}$ are asserted low along with the decode of A0–A9 and assertion of either a $\overline{MEMR}$ or $\overline{MEMW}$. The 82595 Card Configuration Registers are shown below:

4.9 PCMCIA Decode Functions

The Attribute Memory and Common Memory map for a PCMCIA card is shown below. Attribute Memory is defined as the CIS structures (residing in FLASH below 1K) and the CCR Registers (residing in the 82595). Common Memory is defined as the FLASH memory above 1K.



82595 Card Configuration Registers

7	6	5	4	3	2	1	0	
RESET	0	0	0	0	0	XIP En	IO En	CCR 0 (Addr 1016)
0	0	IOIS8	EvntWk	0	0	IREQ	0	CCR 1 (Addr 1018)
0	0	0	0	0	0	0	0	CCR 2 (Addr 1020)
0	0	0	0	0	0	0	0	CCR 3 (Addr 1022)

NOTE:
All 0's in the above registers are reserved.

5.0 COMMAND AND STATUS INTERFACE

The format for the 82595 Command Register is shown in Figure 5-1. The Command Register resides in Register 0 of each of the three IO Banks of the 82595, and can be accessed in any of these banks. The Command Register is accessed by writing to or reading from the IO address for Register 0.

5.1 Command OP Code Field

Bits 0 through 4 of the Command Register comprise the Command OP Code field. A command is issued to the 82595 by writing it into the Command OP Code field. A command can be issued to the 82595 at any time, however in certain cases the command may be ignored (example; issuing a Transmit command while a Transmit is already in progress). In these cases the command is not performed, and no interrupt will result from it.

The Command OP Code field can also be read. In this case it will indicate an execution status event other than TRANSMIT DONE (TDR Done, DIAGNOSE Done, MC-SETUP Done, DUMP Done, INIT Done, and POWER-UP) has been completed. This field is valid only when the EXEC INT bit (Bank 0, Reg 1, Bit 3) is set.

5.2 ABORT (Bit 5)

This bit indicates if an execution command other than TRANSMIT was aborted while in progress. This bit provides status information only. It should be written to a 0 whenever the Command Register is written to.

5.3 Pointer Field (Bits 6 and 7)

The Pointer field controls which 82595 IO register bank is currently to be accessed (Bank 0, Bank 1, or Bank 2). Writing a 00:b to the Pointer field selects Bank 0, 01:b for Bank 1, and 10:b for Bank 2. The Pointer field is valid only when the SWITCH BANK (0h) command is issued. This field will be ignored for any other command. The 82595 will continue to operate in a current bank until a different bank is selected. Upon power up of the device or Reset, the 82595 will default to Bank 0.

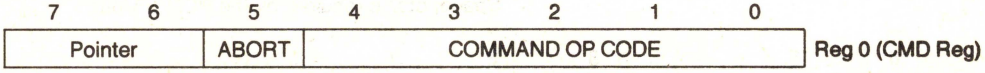


Figure 5-1. 82595 Command Register

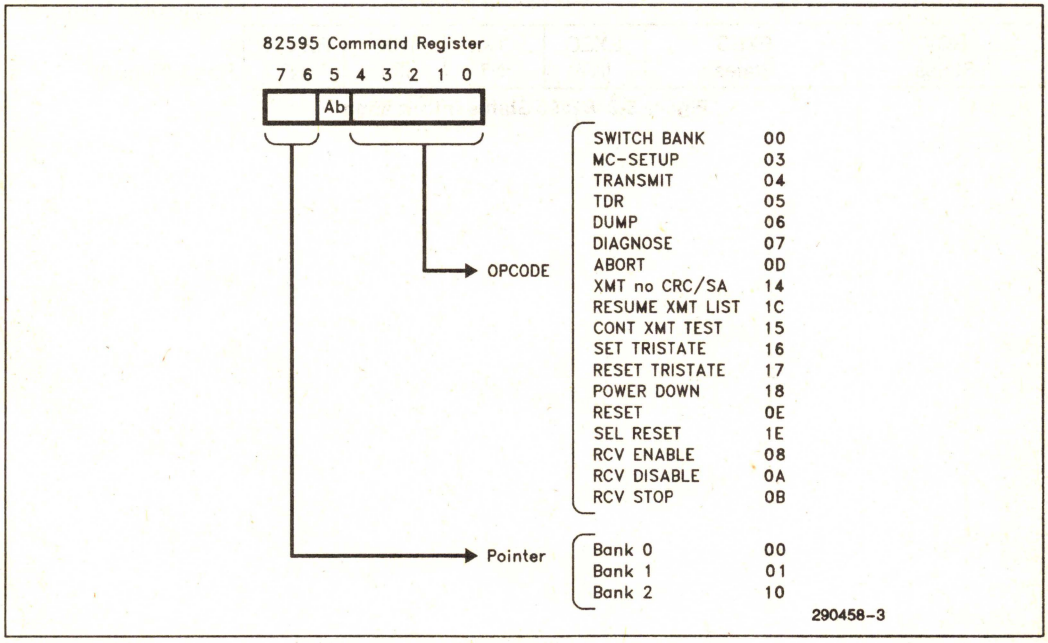


Figure 5-2. 82595 Command Interface

5.4 82595 Status Interface

The Status of the 82595 can be read from Register 1 of Bank 0, with additional status information contained in Register 0 (the Command Register). Figure 5-3 shows these registers. Other information concerning the configuration and initialization of the 82595 and its registers can be obtained by directly reading the 82595 registers.

When read, the Command OP Code field indicates which event (MC Done, Init Done, TDR Done, or DIAG Done) has been completed. This field is valid only when the EXEC INT Bit (Bank 0, Reg 1, Bit 3) is set to a 1. Reading the Pointer field indicates which bank the 82595 is currently operating in. Register 1 in Bank 0 contains the 82595 interrupts status as well as the current states of the RCV and Execution units of the 82595. Resultant status from events such as the completion of a transmission or the reception of an incoming frame is contained in the status field of the memory structures for these particular events.

6.0 INITIALIZATION

Upon either a software or hardware RESET, the 82595 enters into its initialization sequence. When the 82595 is interfaced to an ISA bus, the 82595 reads information from its EEPROM and Jumper block (if utilized) which configures critical parameters (IO Address mapping, etc.) to allow initial accesses to the 82595 during the host system's initialization sequence and also access by the software device driver. The 82595 can also be configured (via the EEPROM) to automatically resolve any conflicts to its IO address location by moving its IO address offset to an unused location in the case that a conflict occurs. This process eliminates a large majority of LAN end-user setup problems.

The 82595 can be configured to operate with ISA systems that require early deassertion of the IOCHRDY signal to its low (not ready) state. The 82595, along with its software driver, can perform a test at initialization to determine if early IOCHRDY deassertion is required.

The 82595, when interfaced to a PCMCIA bus, simply powers up with default PCMCIA configuration values enabled. This is the only step for PCMCIA initialization, since no selection of Interrupts, IO Space, etc. is required by the PCMCIA bus.

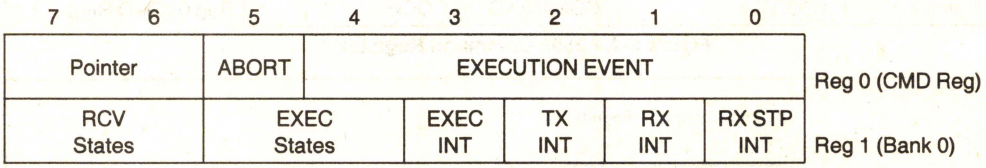


Figure 5-3. 82595 Status Information

7.0 FRAME TRANSMISSION

The 82595 performs all of the necessary functions needed to transmit frames from its local memory. The CPU must only copy a frame into the 82595's local memory (into the transmit buffer section of the local memory), setup the 82595's DMA Current Address Registers to point to the frame, and issue a XMT command to the 82595. The 82595 performs all the link management functions, DMA operations, and statistics keeping to handle transmission onto the link and communicate the status of the transmission to the CPU. The 82595 performs automatic retransmission on collision with no CPU interaction.

7.1 82595 XMT Block Memory Format

The format in which a XMT block is written to memory by the CPU is shown in Figure 7-1 for a 16-bit interface. Figure 7-2 shows this structure for an 8-bit interface.

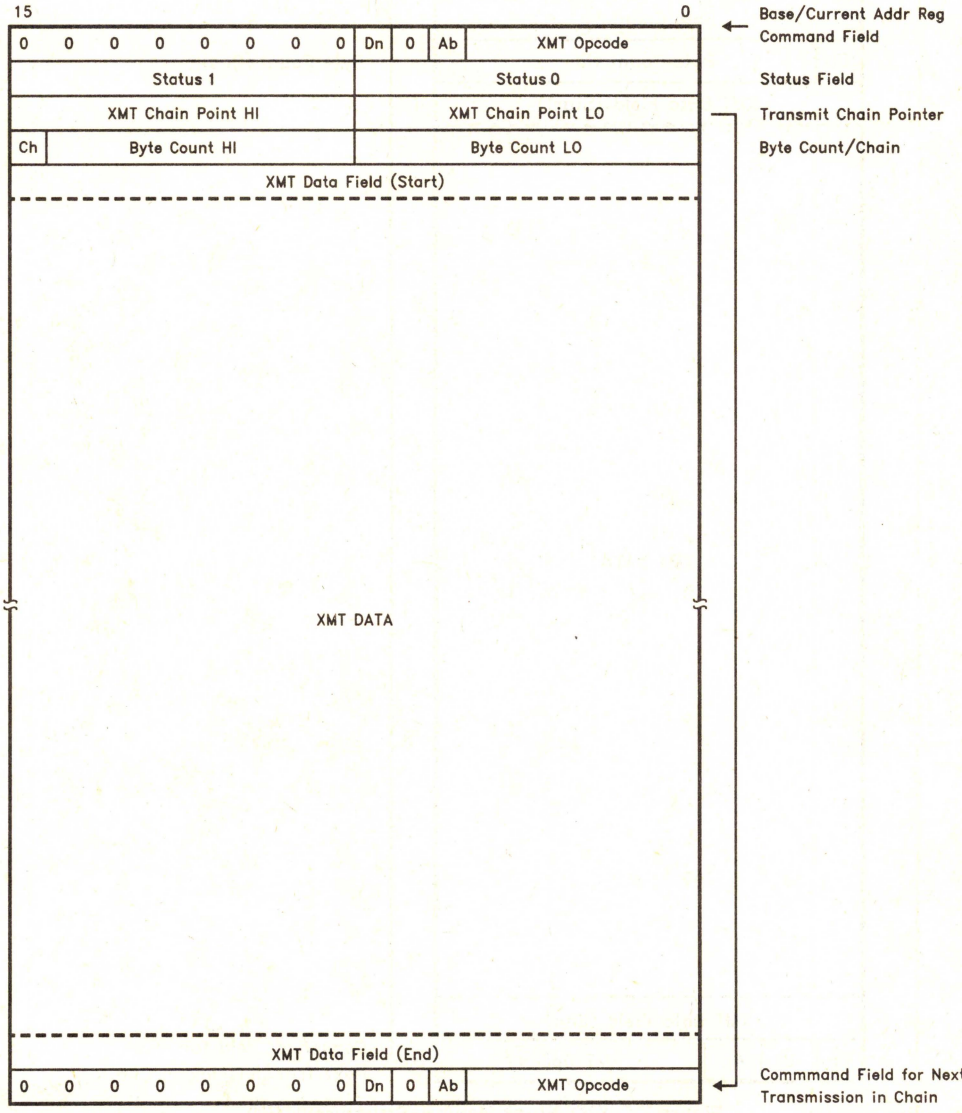


Figure 7-1. XMT Block Memory Structure (16-Bit)

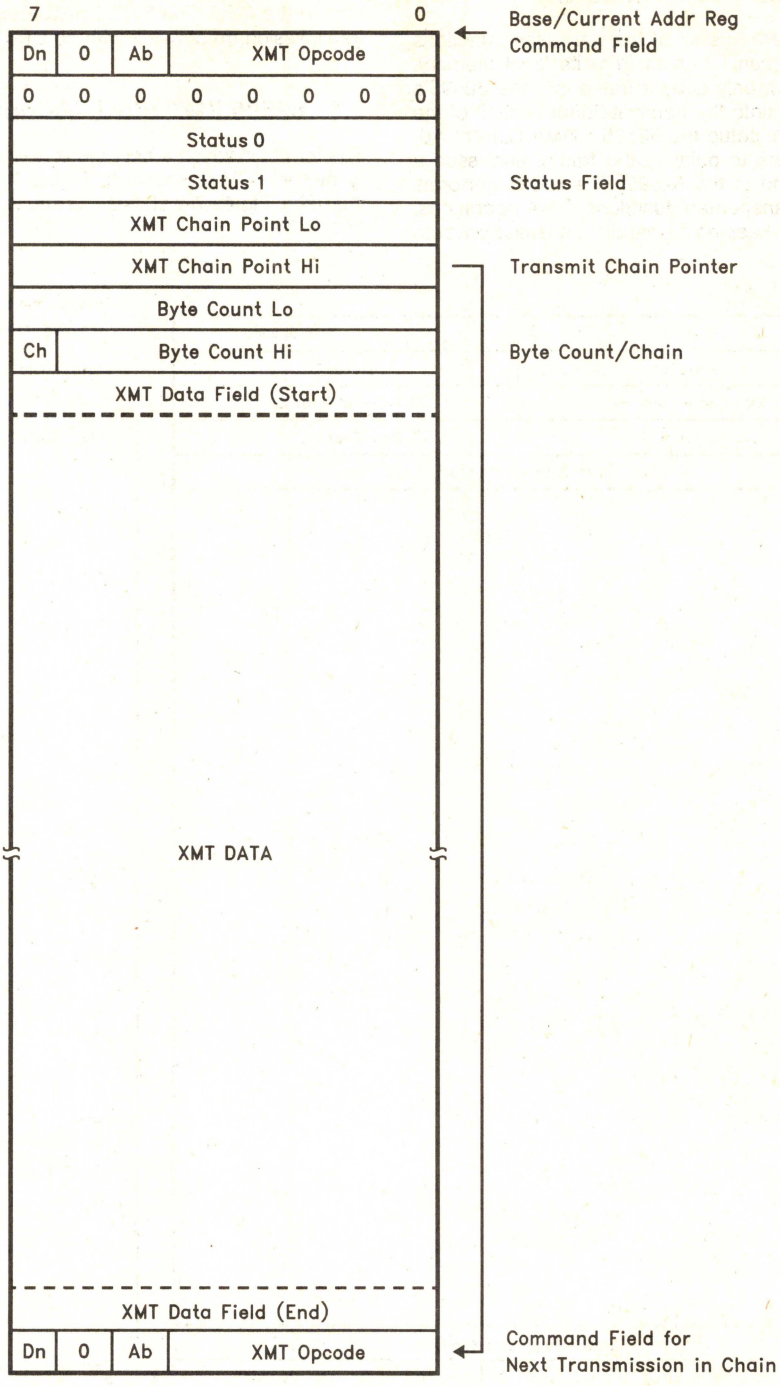


Figure 7-2. XMT Block Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 7-3. In a 16-bit wide interface, these two bytes will combine to form one word. This field is originally set to all 0's by the CPU as the XMT block is copied to memory. It is updated by the 82595 upon completion of the transmission.

7.2 XMT Chaining

The 82595 can transmit consecutive frames without the CPU having issued a seperate Transmit command for each frame. This is called Transmit Chaining. The 82595 Transmit Chaining memory structure for a 16-bit interface is shown in Figure 7-4, with an 8-bit interface shown in Figure 7-5. The 82595 registers which control the memory structure are also shown. The CPU places multiple XMT blocks in the Transmit buffer. The 82595 will transmit each frame in the chain, reporting the status for each frame in its Status field. This chain can be dynamically updated by the CPU to add more frames to the chain. The transmit chain can be configured to terminate upon an errored frame (maximum collisions, underrun, lost CRS, etc.) or it can continue to the next frame in the chain. The 82595 can be configured to interrupt upon completion of each transmission or to interrupt at the end of the transmit chain only (it would always interrupt upon an errored condition however).

7	6	5	4	3	2	1	0	
TX DEF	HRT BET	MAX COL	X	No OF COLLISIONS				Status 0
COLL	X	TX OK	0	LTCOL	LST CRS	X	UND RUN	Status 1

Figure 7-3. Transmit Result

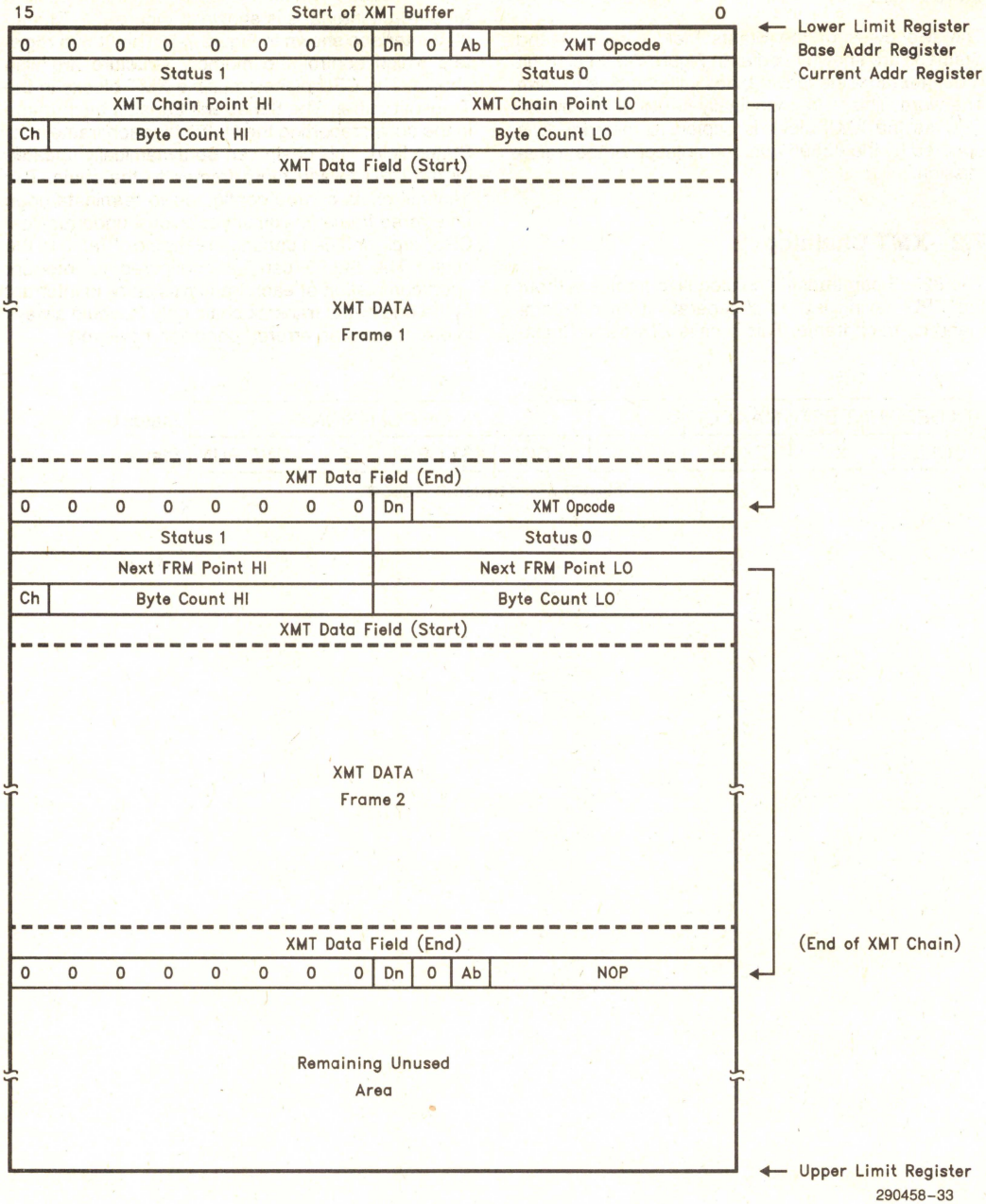


Figure 7-4. 82595 XMT Chaining Memory Structure

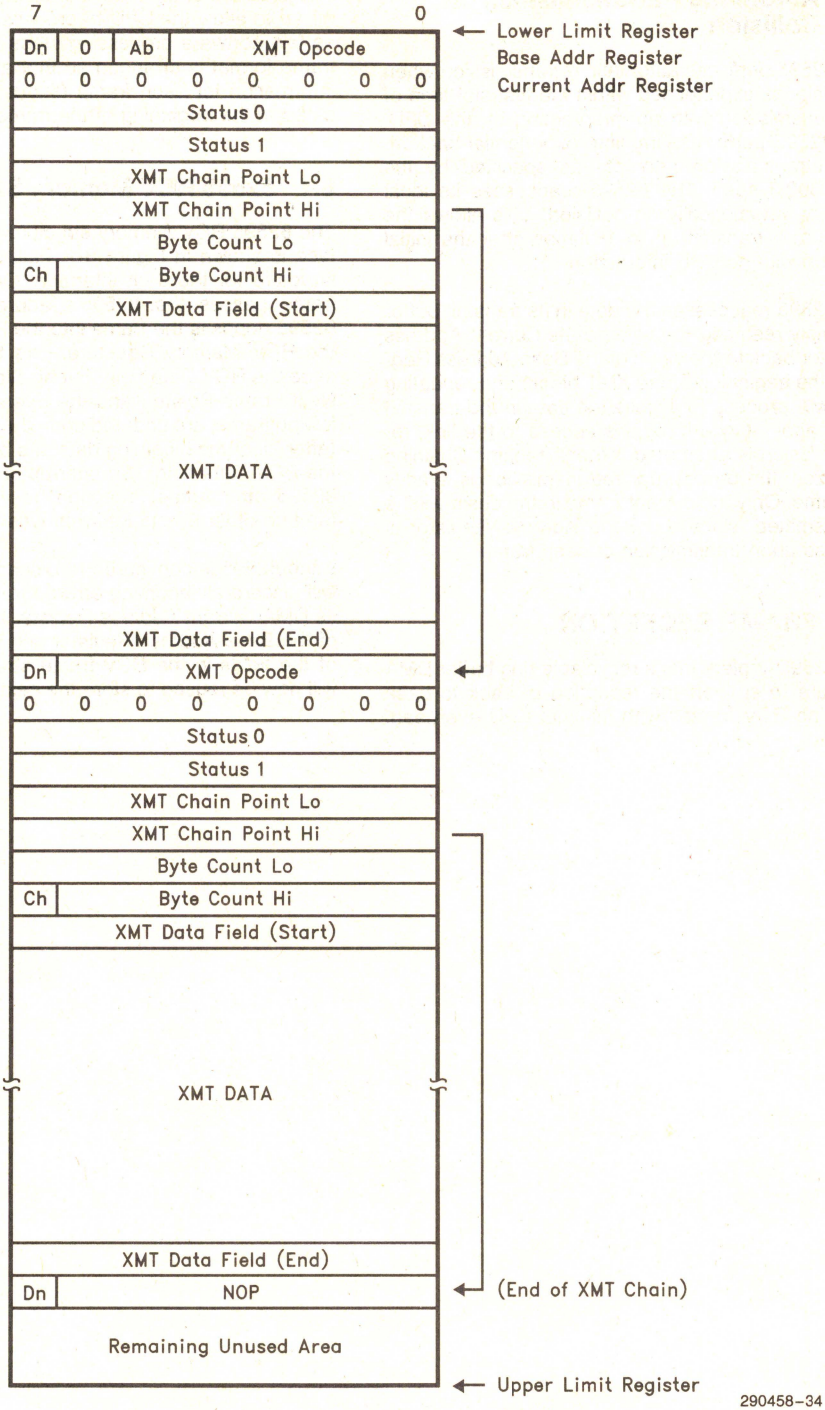


Figure 7-5. XMT Block Memory Structure (8-Bit)

7.3 Automatic Retransmission on Collision

The 82595 performs automatic retransmission when a collision is experienced within the first slot time of the transmission with no intervention by the CPU. The 82595 performs jamming, exponential backoff, and retransmission attempts as specified by the IEEE 802.3 spec. The 82595 reaccesses its local memory automatically on collision. This allows the 82595 to retransmit up to 15 times after the initial collision with no CPU interaction.

The 82595 reaccesses the data in its transmit buffer by simply resetting the value of its Current Address Register back to the value of the Base Address Register (the beginning of the XMT block) and repeating the DMA process to access the data in the transmit buffer again. Once it regains access to the link, retransmission is attempted. When Transmit Chaining is utilized, the process for retransmission is exactly the same. Only the current frame in the chain will be retransmitted, since the Base Address Register is updated upon transmission of each frame.

8.0 FRAME RECEPTION

The 82595 implements a recyclable ring buffer DMA structure to support the reception of back to back incoming RCV frames with minimal CPU overhead. The structure of the RCV frames in memory are optimized to allow the CPU to process each frame with as few software processing steps as possible. The frame format is arranged so that all of the required information for each frame (status, size, etc.) is located at the beginning of the frame.

8.1 82595 RCV Memory Structure

The 82595 RCV memory structure for a 16-bit interface is shown in Figure 8-1. Figure 8-2 shows this structure for the 8-bit interface. Once an incoming frame passes the 82595's address filtering, the 82595 deposits the frame into the RCV Data field of the RCV Memory Structure. The fields which precede the RCV Data field, Event, Status, Byte Count, Next Frame Pointer, and the Event field of the following frame, are updated upon the end of the frame (after all of the incoming data has been deposited in the RCV Data field). An Interrupt is asserted by the 82595 after frame reception has been completed (and no other 82595 Interrupt was pending).

If the 82595 is configured to Discard Bad Frames, it will discard all incoming errored frames by resetting its DMA Current Address Register back to the value of the Base Address Register and not updating any of the fields in the RCV frame structure. This area will now be reused to store the next incoming frame.

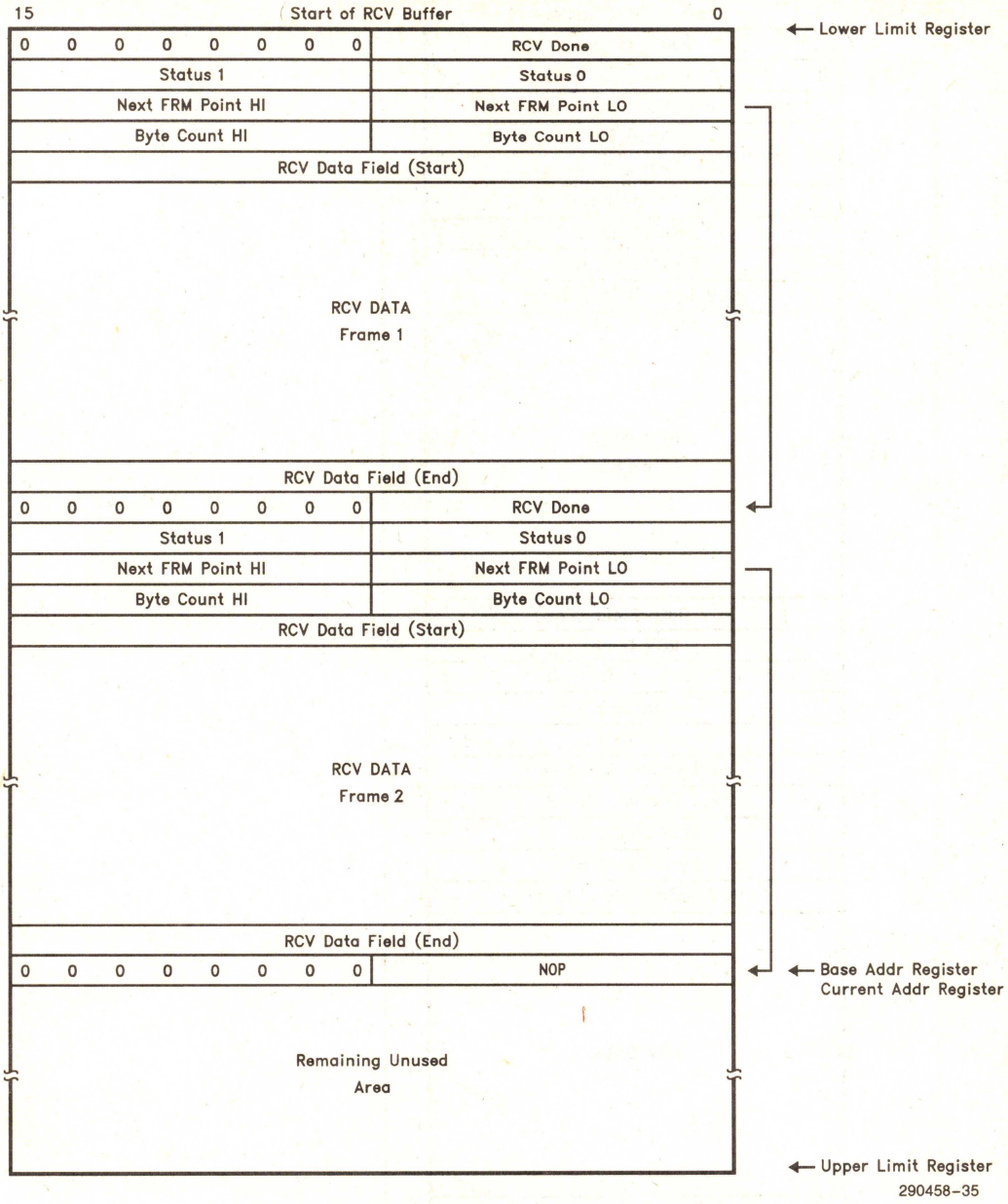


Figure 8-1. 82595 RCV Memory Structure (16-Bit)

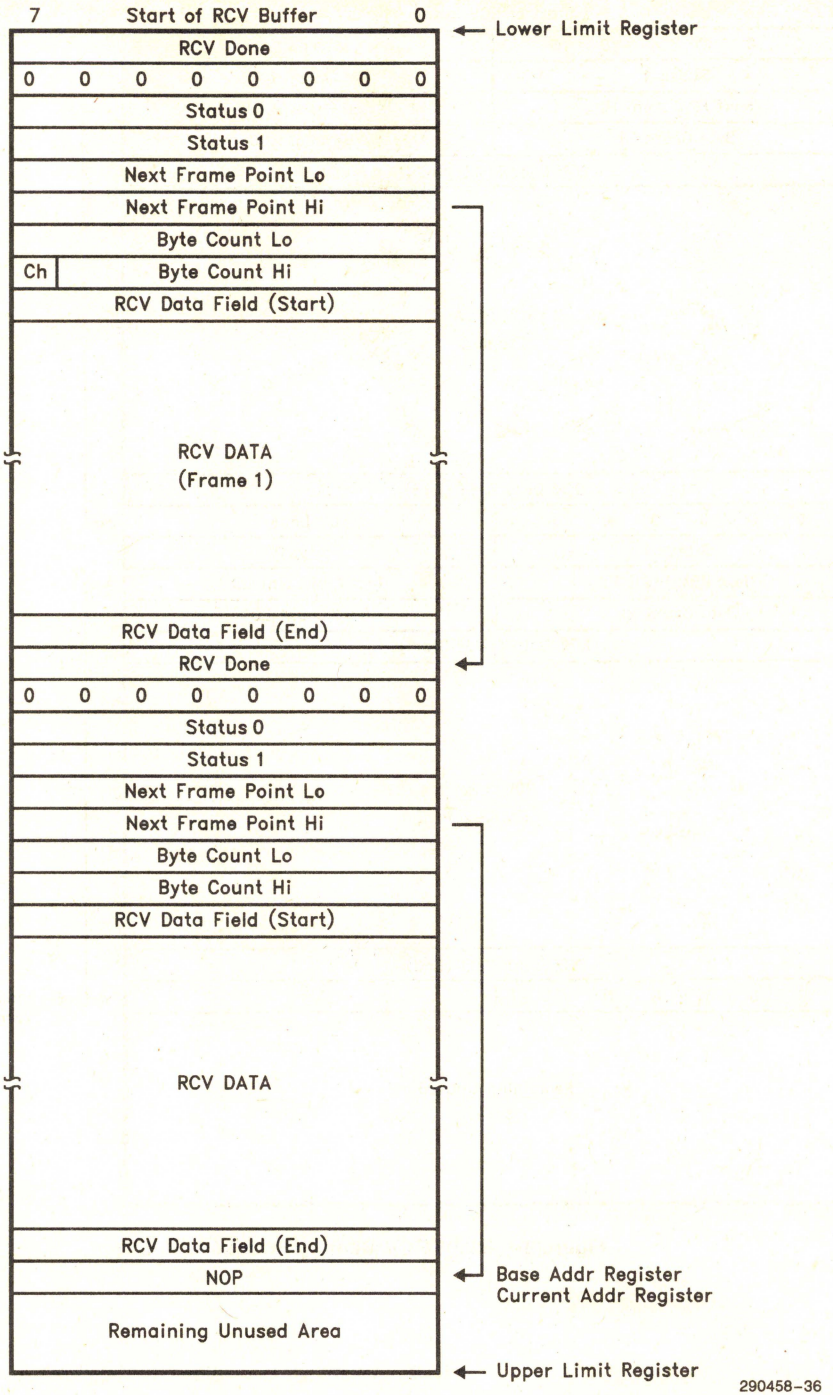


Figure 8-2. 82595 RCV Memory Structure (8-Bit)

Status Field

The two bytes of the Status Field (Status 0 and Status 1) are shown in detail in Figure 8-3. In a 16-bit wide interface, these two bytes will combine to form one word. The 82595 provides this field for each incoming frame.

8.2 RCV Ring Buffer Operation

The 82595 RCV Ring Buffer operation is illustrated in Figure 8-4. The 82595 copies received frames sequentially into the RCV Buffer area of the local memory. The CPU processes these frames by copying the frames from the local memory. After a frame is processed, the CPU updates the 82595's Stop Register to point to the last location processed. This indicates that the RCV Buffer memory which precedes the value programmed in the Stop Register is now free area (it has been processed by the CPU). When the 82595 reaches the end of the RCV Buffer (the Upper Limit Register value) it will now wrap around back to the beginning of the buffer, and continue to copy RCV frames into the buffer, beginning at the value pointed to by the Lower Limit Register. The 82595 will continue to copy frames into the RCV Buffer area as long as it does not reach the address pointed to by the Stop Register (if this does occur, the 82595 stops copying the frames into memory and issues an Interrupt to the CPU). As the CPU processes additional incoming frames, the Stop Register value continues to be moved. This action allows the CPU to keep ahead of the incoming frames and allows the Ring Buffer to be continually recycled as the memory space consumed by an incoming frame is reused as that frame is processed.

7	6	5	4	3	2	1	0	
SRT FRM	X	X	1	X	X	IA MCH	RCLD	Status 0
TYP/LEN	0	RCV OK	LEN ERR	CRC ERR	ALG ERR	0	OVR RN	Status 1

Figure 8-3. RCV Status Field

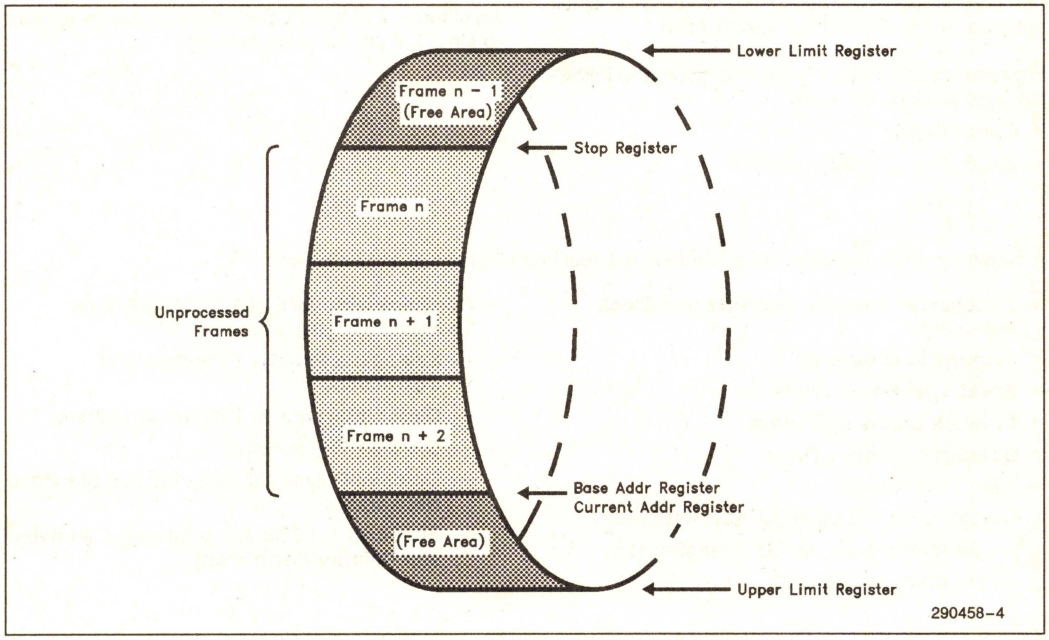


Figure 8-4. 82595 RCV Ring Buffer Operation

9.0 SERIAL INTERFACE

The 82595's serial interface subsystem incorporates all the active circuitry required to interface the 82595 to 10BASE-T networks or to the attachment unit (AUI) interface. It includes on-chip AUI and TPE drivers and receivers as well as Manchester Encoder/Decoder and Clock Recovery circuitry. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 AUI interface. The AUI port can also be interfaced to a transceiver to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595 automatically enables either the AUI or TPE interface, depending on which medium is active. This automatic selection can be overridden by software configuration. The TPE interface also features a polarity fault detection and correction circuit which will detect and correct a polarity error on the twisted pair wire, the most common wiring fault in twisted pair networks.

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ±0.01% clock required by the IEEE 802.3 specification.

We recommend that a crystal that meets the following specifications be used:

- Quartz Crystal
- 20.00 MHz ±0.002% at 25°C
- Accuracy ±0.005% over Full Operating Temperature, 0°C to +70°C
- Parallel resonant with 20 pF Load Fundamental Mode

Several vendors have such crystals; either off-the-shelf or custom made. Two possible vendors are:

1. M-Tron Industries, Inc.
   Yankton, SD 57078
   Specifications;
   Part No. HC49 with 20 MHz, 50 PPM over 0°C to +70°C, and 20 pF fundamental load.
2. Crystek Corporation
   100 Crystal Drive
   Ft. Myers, FL 33907
   Part No. 013212

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics, therefore it is advisable to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 pF and 35 pF.

An external 20 MHz MOS-level clock may be applied to pin X1, if pin X2 is left floating.

A summary of the 82595's serial interface subsections functions is shown below:

- **Manchester Encoder/Decoder and Clock Recovery**
- **Diagnostic Loopback**
- **Reset-Low-Power Mode**
- **Network Status Indicators**
- **Defeatable Jabber Timer**
- **User Test Modes**
- **Complies with IEEE 802.3 AUI Standard**
  - **— Direct Interface to AUI Transformers**
  - **— On-Chip AUI Squelch**
- **Complies with IEEE 802.3 10BASE-T for Twisted Pair Ethernet**
  - **— Selectable Polarity Detection and Correction**
  - **— Direct Interface to TPE Analog Filters**
  - **— On-Chip TPE Squelch**
  - **— Defeatable Link Integrity for Pre-Standard Networks**
  - **— Supports 3 LEDs (Link Integrity, Activity, and Polarity Correction)**

10.0 APPLICATION EXAMPLE

This section is intended to provide Ethernet LAN designers with a basic understanding of how the 82595 is used in a buffered LAN design. A design for both an ISA solution and a PCMCIA solution are illustrated. The majority of the functionality contained in these solutions is integrated into the 82595, resulting in a low cost, easily implemented design. This high level of integration also enables the design of the two different solutions, ISA and PCMCIA, to be very similar, which allows these two solutions to share a common software base, resulting in further cost savings.

Figure 10-1 shows an 8-bit/16-bit ISA design using the 82595. This same design could be implemented as either an ISA motherboard or ISA adapter solution. Figure 10-2 shows an 8-bit/16-bit PCMCIA IO Card design. As mentioned in the above paragraph, these two designs are very similar differing only in the following three ways:

- The ISA solution utilizes an EEPROM to enable the implementation of a jumperless design. The EEPROM is not used in the PCMCIA design (it is also not required for ISA motherboard designs).
- The PCMCIA solution utilizes a 256K x 8 FLASH to implement CIS structures and FLASH Common Memory required by PCMCIA rev 2.0 specifications. The FLASH is optional in an ISA design (it is shown in the ISA schematics however).
- The Data Bus is not buffered (no ALS245 Transceivers) in the PCMCIA design.

10.1 Bus Interface

The 82595 Bus Interface unit integrates the interface to both an ISA compatible bus and a PCMCIA rev 2.0 bus. Selection of the desired bus interface is done by strapping the PCMCIA/ISA pin accordingly. Two 74ALS245 transceivers are used to buffer the 82595's data bus, with the 82595 providing the control over the transceivers. The 82595 also provides the complete control and address interface to the host system bus. When the ISA bus interface is selected, it implements the complete ISA bus protocol. When PCMCIA interface is selected, the complete PCMCIA bus interface protocol is implemented.

10.2 Local Memory Interface

The 82595's local memory interface includes a DMA unit which controls data transfers between the 82595 and the local memory DRAM. The 82595 can support up to 64 Kbytes of local DRAM.

The 82595 provides address decoding and control to allow access to an external Boot EPROM or a FLASH. Addition of a Boot EPROM or FLASH to an ISA solution is optional. The FLASH is always contained as part of a PCMCIA solution. The 82595 also supports a separate IA PROM if one is desired. For this example the IA is assumed to be stored in the serial EEPROM for the ISA solution and in the FLASH for the PCMCIA solution.

10.3 EEPROM Interface (ISA Only)

The 82595 provides a complete interface to a serial EEPROM for ISA adapter designs. For ISA motherboard designs and PCMCIA designs, the EEPROM is not required. The EEPROM is used to store configuration information such as Memory and IO Mapping Window, Interrupt line selection, local bus width, etc. The EEPROM is used to replace jumper blocks which previously contained this type of information. The 82595 also contains an optional jumper interface (J0–J2). These jumpers can be used to select the IO mapping window of the solution. In the case of this design, the jumper block is grounded (disabled) with the IO mapping window being contained in the EEPROM.

10.4 Serial Interface

The 82595's serial interface provides either an AUI port interface or a Twisted Pair Ethernet (TPE) interface. The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully compliant IEEE 802.3 10BASE5 interface. The AUI port can also be interfaced to a transceiver device on the adapter to provide a fully compliant IEEE 802.3 10BASE2 (Cheapernet) interface. The TPE port provides a fully compliant 10BASE-T interface. The 82595 automatically enables either the AUI or TPE interface depending on which medium is connected to the chip. This automatic selection can be overridden by software configuration.

10.4.1 AUI CIRCUIT

When used in conjunction with pulse transformers, the 82595 provides a complete IEEE 802.3 AUI interface. In order to meet the 16V fault tolerance specification of IEEE 802.3, a pulse transformer is recommended. The transformer should be placed between the TRMT, RCV, and CLSN pairs of the 82595 and the DO, DI, and CI pairs of the AUI (DB-15) connector. The pulse transformer should have the following characteristics:

- 75 μH minimum inductance (100 μH recommended)
- 2000V isolation between the primary and secondary windings

- 2000V isolation between the primaries of separate transformers
- 1:1 Turns ratio

The RCV and CLSN input pairs should each be terminated by 78.7Ω ±1% resistors.

10.4.2 TPE CIRCUIT

The 82595 provides the line drivers and receivers needed to directly interface to the TPE analog filter network. The TPE receive section requires a 100Ω termination resistor, a filter section (filter, isolation transformer, and a common mode choke) as described by the 10BASE-T 802.3i-1990 specification.

The TPE transmit section is implemented by connecting the 82595's four TPE outputs (TDH, $\overline{\text{TDH}}$, TDL, $\overline{\text{TDL}}$) to a resistor summing network to form the differential output signal. The parallel resistance of R5 and R6 sets the transmitters maximum output voltage, while the difference (R5−R6)/R5+R6), is used to reduce the amplitude of the second half of the fat bit (100 ns) to a predetermined level. This predistortion reduces line overcharging, a major source of jitter in the TPE environment. The output of the summing network is then fed into the above mentioned filter and then to the 10BASE-T connector (RJ-45). Analog Front End solutions can be purchased in a single-chip solution from several manufacturers. The solution described in this data sheet uses the Pulse Engineering (PE65434) AFE.

10.4.3 LED CIRCUIT

The 82595's internal LED drivers support four LED indicators displaying node status and activity (i.e., Transmit data, receive data, collisions, link integrity, polarity correction, and port (TPE/AUI). To implement the LED indicators, connect the LED driver output to an LED in series with a 510Ω resistor tied to V_{CC}. Each driver can sink up to 10 mA of current with an output impedance of less than 50Ω.

10.5 Layout Guidelines

10.5.1 GENERAL

The analog section, as well as, the entire board itself should conform to good high-frequency practices and standards to minimize switching transients and parasitic interaction between various circuits. To achieve this, the following guidelines are presented.

Make power supply and ground traces as thick as possible. This will reduce high-frequency cross coupling caused by the inductance of thin traces.

Connect logic and chassis ground together.

All V_{CC} pins must be connected to the same power supply, all V_{SS} pins to the same ground plane. Separate decoupling and noise condition should be used per power-supply/ground pin.

Close signal paths to ground as close as possible to their sources to avoid ground loops and noise cross coupling.

Use high-loss magnetic beads on power supply distribution lines.

10.5.2 CRYSTAL

The crystal should be adjacent to the 82595 and trace lengths should be as short as possible. the X1 and X2 traces should be symmetrical.

10.5.3 82595 ANALOG DIFFERENTIAL SIGNALS

The differential signals from the 82595 to the transformers, analog front end, and the connectors should be symmetrical for each pair and as short as possible.

As a general rule, the trace widths should be one to three times the distance between the PCB layers to eliminate excessive trace inductance.

The differential signals should also be isolated from the high speed logic signals on the same layer as well as on any sublayers of the PCB.

Group each of the circuits together, but keep them separate from each other. Separate their grounds.

In layout, the circuitry from the connectors to the filter network, should have the ground and power planes removed from beneath it. This will prevent ground noise from being induced into the analog front end.

All trace bends should not exceed 45 degrees.

10.5.4 DECOUPLING CONSIDERATIONS

Four 0.1 μF ceramic capacitors should be used. Place one on each side in the center of the I.C. (V_{CC} pins 23, 51, 89, 125 are recommended) adjacent to the 82595. Connect the capacitors directly to the V_{CC} pins on the 82595 and then directly to the ground plane. In addition to the 0.1 μF capacitors, a 10 μF tantalum should be used near one of the 82595's V_{CC} pins. The proximity of this capacitor to the 82595 is not as critical as in the case of the 0.1 μF capacitors. Placement of this capacitor within approximately one inch of the 82595 is recommended.

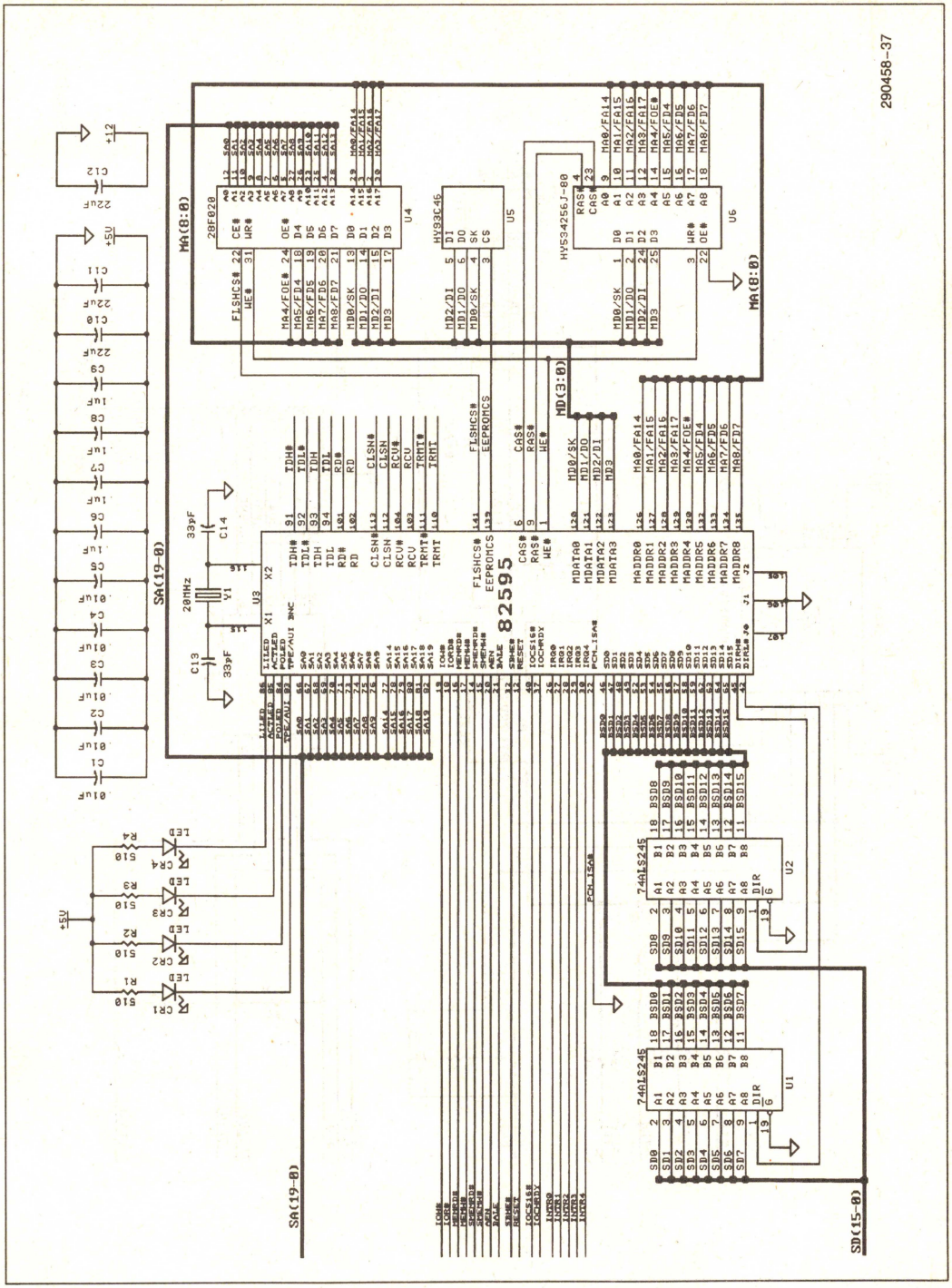


Figure 10-1. 82595 ISA Design Example

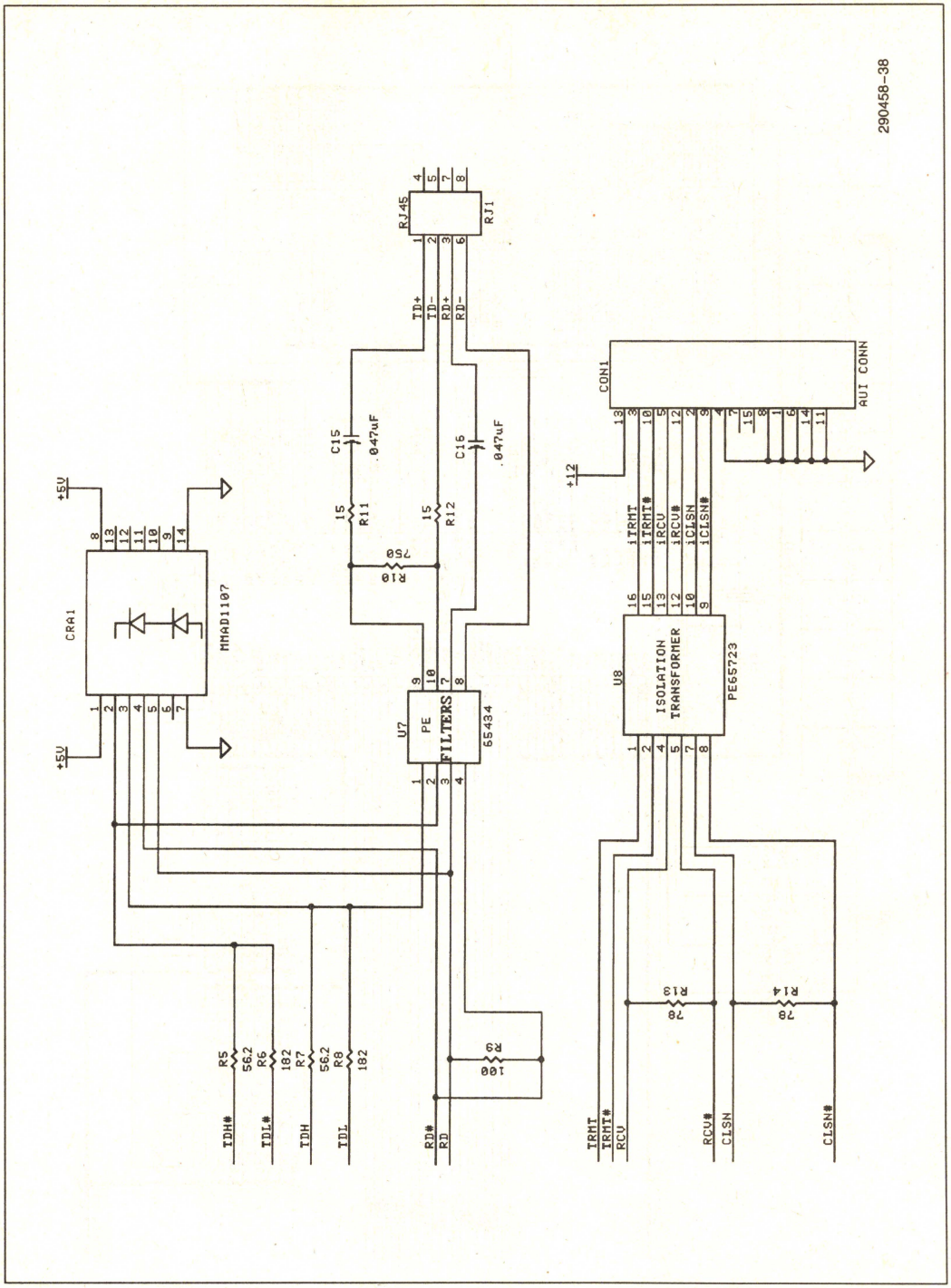


Figure 10-1. 82595 ISA Design Example (Continued)

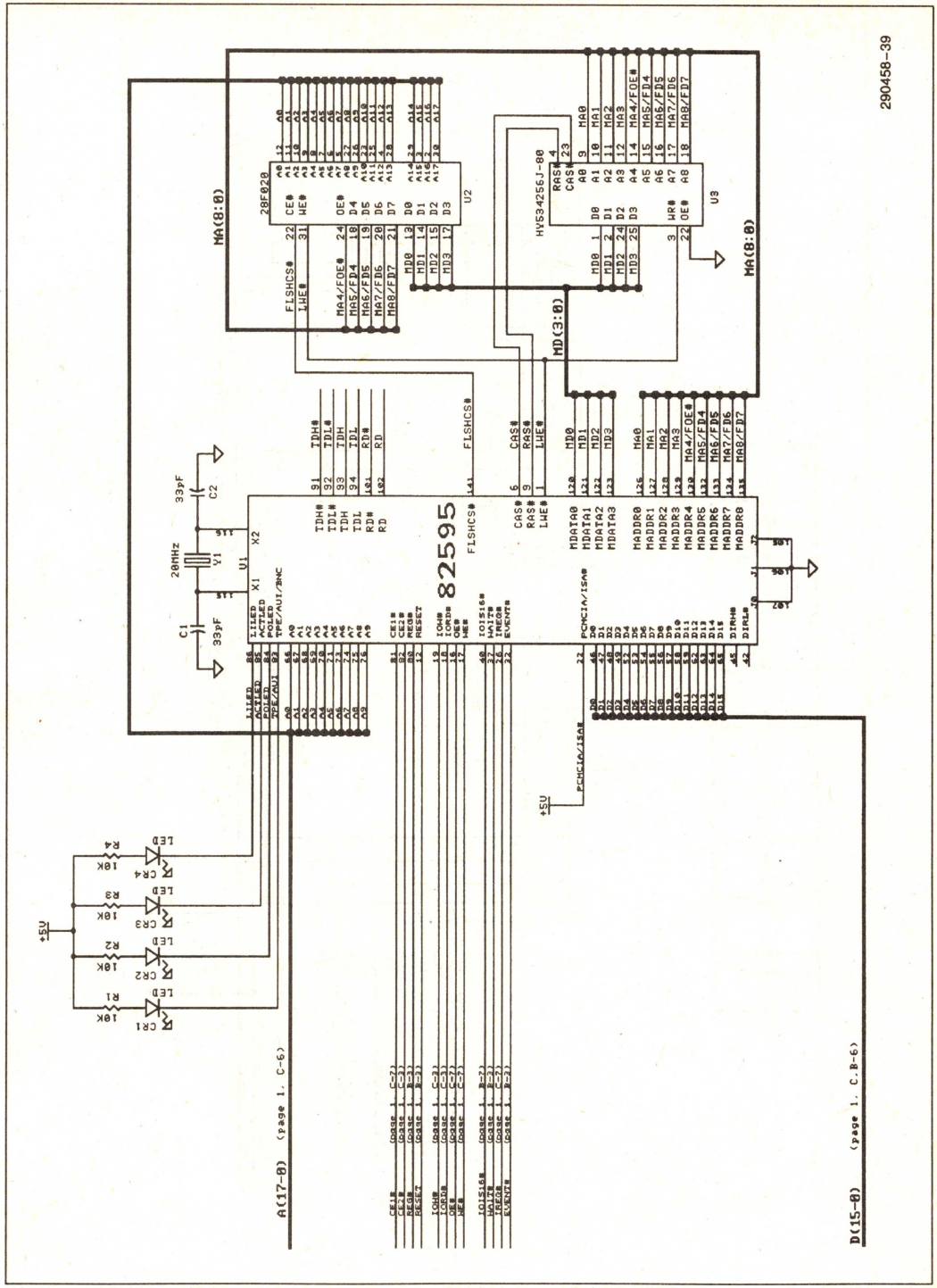


Figure 10-2. 82595 PCMCIA Design Example

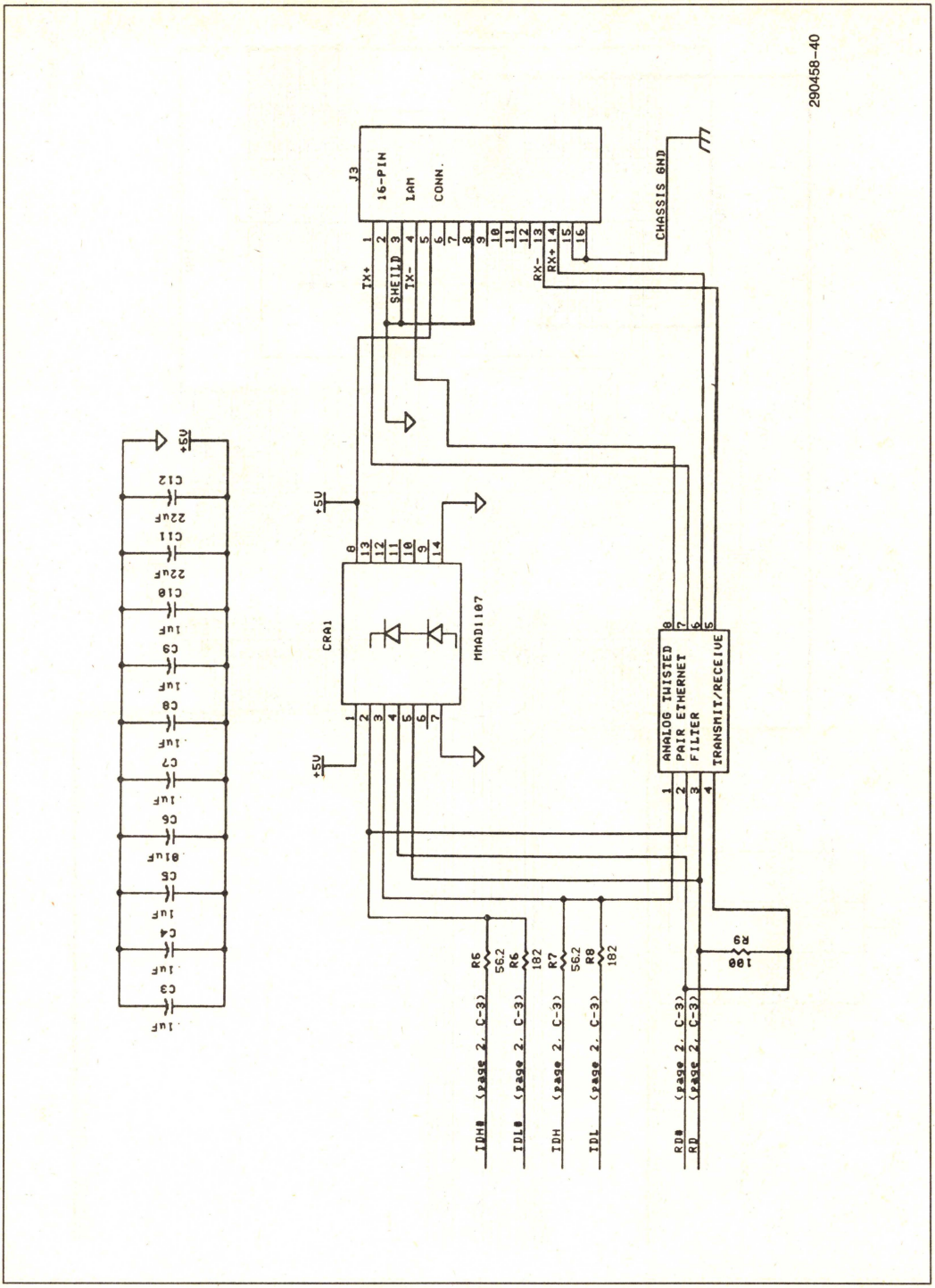


Figure 10-2. 82595 PCMCIA Design Example (Continued)

11.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

11.1 Absolute Maximum Ratings

Case Temperature under Bias .....0°C to +85°C
Storage Temperature .....−65°C to +140°C
All Output and Supply Voltages .....−0.5V to +7V
All Input Voltages .....−1.0V to +6.0V(1)

Further information on the quality and reliability of the 82595 may be found in the *Components Quality and Reliability Handbook*, Order Number 210997.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

1

Table 11-1. D.C. Characteristics (T_C = 0°C to +85°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input LOW Voltage (TTL)	−0.3	+0.8	V	
V_{IH}	Input HIGH Voltage (TTL)	2.0	V_{CC} + 0.3	V	
$V_{IH(JUMPR)}$	Input HIGH Voltage (Jumpers)	3.0	V_{CC}+0.3	V	
V_{OL1}	Output LOW Voltage(11)		0.45	V	I_{OL} = 2 mA
V_{OL2}	Output LOW Voltage(11)		0.45	V	I_{OL} = 6 mA
V_{OL3}	Output LOW Voltage(11)		0.45	V	I_{OL} = 12 mA
V_{OL4}	Output LOW Voltage(11)		0.45	V	I_{OL} = 17 mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −1 mA
V_{OL} (LED)(2)	Output Low Voltage		0.45	V	I_{OL} = 10 mA
V_{OH} (LED)	Output High Voltage	3.9		V	I_{OH} = −500 μA
I_{LP}	Leakage Current, Low Power Mode(3)		±10	μA	$0 \le V_I \le V_{CC}$
R_{DIFF}	Input Differential-Resistance(4)	10		KΩ	DC
V_{IDF} (TPE)(5)	Input Differential Accept Input Differential Reject	±0.5	±3.1 ±0.3	V_P V_P	5 MHz ≤ f ≤ 10 MHz
R_S (TPE)(6)	Output Source Resistance	4	11	Ω	$\|I_{LOAD}\|$ = 25 mA
V_{IDF} (AUI)(7)	Input Differential Accept Input Differential Reject	±0.3	±1.5 ±0.16	V_P V_P	
V_{ICM} (AUI)	AC Input Common Mode		±0.5 ±0.1	V_P V_P	f ≤ 40 KHz 40 KHz ≤ f ≤ 10 MHz
V_{ODF} (AUI)(8)	Output Differential Voltage	±0.45	±1.2	V	
I_{OSC} (AUI)	AUI Output Short Circuit Current		±150	mA	Short Circuit to V_{CC} or GND
VU (AUI)	Output Differential Undershoot		−100	mV	
V_{ODI} (AUI)	Differential Idle Voltage(9)		40	mV	
I_{CC}	Power Supply Current		150	mA	
I_{CCPD}	Power Supply Current– Power Down Mode		1	mA	
C_{IN}(10)	Input Capacitance		10	pF	@ f = 1 MHz

NOTES:
1. The voltage levels for RCV and CLSN pairs are −0.75V to +8.5V.
2. LED Pins: ACTLED, TPE_BNC_AUI, POLED, LILED.
3. Pins: ACTLED, TPE_BNC_AUI, POLED, LILED.
4. Pins: RD to $\overline{RD}$, RCV to $\overline{RCV}$ and CLNS to $\overline{CLSN}$.
5. TPE input pins: RD and $\overline{RD}$.
6. TPE output pins: TDH, $\overline{TDH}$, TDL and $\overline{TDL}$, R_S measure V_{CC} or V_{SS} to pin.
7. AUI input pins: RCV and CLSN pairs.
8. AUI output pins: TPMT pair.
9. Measured 8.0 μs after last positive transition of data packet.

NOTES: (Continued)
10. Characterized, not tested.
11. V_{OL1} is pins SD_{0-15}, $\overline{RAS}$, $\overline{CAS}$, EEPROMCS, $\overline{IAPROMCS}$, $\overline{FLASHCS}$, $\overline{DIRH}$, and $\overline{DIRL}$. V_{OL2} is pins $MDATA_{0-3}$, $MADDR_{0-8}$, TDO, $\overline{WE}$, $\overline{SBHE}$, and $\overline{SMOUT}$. V_{OL3} is pins IOCHRDY and INT_{0-4}. V_{OL4} is $\overline{IOCS16}$.

11.1.1 PACKAGE THERMAL SPECIFICATIONS

The 82595 is specified for operation when case temperature is within the range of 0°C to 85°C. The case temperature may be measured in any environment to determine whether the 82595 is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from the θ_{JA} and the θ_{JC} from the following equations:

$$T_J = T_C + P*\theta_{JC}$$
$$T_A = T_J - P*\theta_{JA}$$
$$T_C = T_A + P*(\theta_{JA} - \theta_{JC})$$

θ_{JA} and θ_{JC} values for the 144 tQFP package are as follows:

Thermal Resistance (°C/Watt)

θ_{JC}	θ_{JA} − VS − Airflow ft/min (m/Sec)	
	0 (0)	200 (1.01)
17	48	38

11.2 A.C. Timing Characteristics

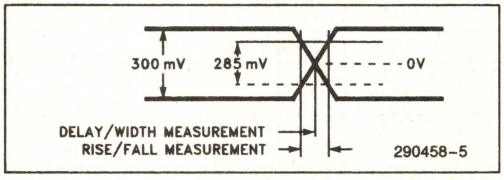


Figure 11-1. Voltage Levels for Differential Input Timing Measurements (RCV and CLSN Pairs)

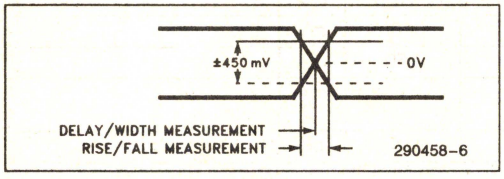


Figure 11-2. Voltage Levels for TDH, TDL, $\overline{TDH}$ and $\overline{TDL}$

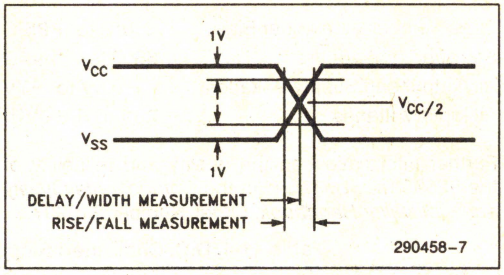


Figure 11-3. Voltage Levels for TRMT Pair Output Timing Measurements

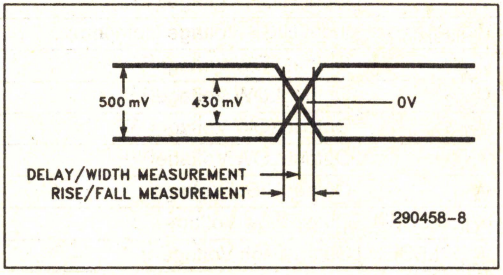


Figure 11-4. Voltage Levels for Differential Input Timing Measurements (RD Pair)

11.3 A.C. Measurement Conditions

1. T_C = 0°C to +85°C, V_{CC} = 5V ±5%
2. The signal levels are referred to in Figures 1, 2, 3 and 4.
3. A.C. Loads:
   a) AUI Differential: a 10 pF total capacitance from each terminal to ground and a load resistor of 78Ω ±1% in parallel with a 27 μH ±5% inductor between terminals.
   b) TPE: 20 pF total capacitance to ground.

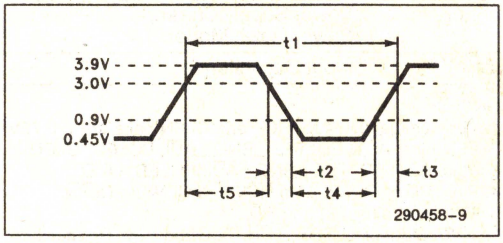


Figure 11-5. X1 Input Voltage Levels for Timing Measurements

Table 11-2. Clock Timing

Symbol	Parameter	Min	Max	Unit
t1	X1 Cycle Time	49.995	50.005	ns
t2	X1 Fall Time		5	ns
t3	X1 Rise Time		5	ns
t4	X1 Low Time	15		ns
t5	X1 High Time	15		ns

11.4 ISA Interface Timing

Table 11-3. ISA 16-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1a	BALE Active to Inactive	50		ns	
T2a	BALE Active from Command Inactive	35		ns	
T3a	AEN Valid to Falling Edge of BALE	20		ns	Applies for Early IOCHRDY
T4a	AEN Valid to I/O Command Active	100		ns	
T5a	AEN Valid from I/O Command Inactive	30		ns	
T6a	SA Valid to Falling BALE	20		ns	Applies for Early IOCHRDY
T7a	SA to CMD Active	63		ns	
T8a	SA Valid Hold from CMD Inactive	42		ns	
T9a	Valid SA to $\overline{\text{IOCS16}}$ Active		100	ns	
T10a	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T11a	CMD Active to Inactive	125		ns	
T12a	CMD Inactive to Active	92		ns	*Before* I/O Command
T13a	Active CMD to Valid IOCHRDY		18	ns	
T14a	IOCHRDY Inactive Pulse		12	μs	
T15a	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T16a	DATA Driven from READ CMD Active	0		ns	
T17a	Valid READ Data from CMD Active		54	ns	Applies for Standard Cycles Only
T18a	Valid READ Data from IOCHRDY Active		42	ns	Applies for Ready Cycles Only
T19a	READ Data Hold from CMD Inactive	0		ns	
T20a	READ CMD Inactive to Data Tristate		30	ns	
T21a	CMD to WRITE Data Active		62	ns	
T22a	WRITE Data Hold from CMD Inactive	25		ns	
T23a	WRITE CMD Inactive to Data Tristate		30	ns	
T24a	IOCHRDY Inactive to CMD Active	15		ns	Applies for Early IOCHRDY
T25a	BALE Inactive to CMD Active	55		ns	Applies for Early IOCHRDY
T26a	READ CMD Active to $\overline{\text{DIRx}}$ Active		34	ns	
T27a	READ CMD Inactive to $\overline{\text{DIRx}}$ Inactive		15	ns	

Table 11-4. ISA 8-Bit I/O Access

Parameter	Description	Min	Max	Units	Comments
T1b	BALE Active to Inactive	50		ns	
T2b	BALE Active from Command Inactive	35		ns	
T3b	AEN Valid to Falling Edge of BALE	20		ns	Applies for Early IOCHRDY
T4b	AEN Valid to I/O Command Active	100		ns	
T5b	AEN Valid from I/O Command Inactive	30		ns	
T6b	SA Valid to Falling BALE	20		ns	Applies for Early IOCHRDY
T7b	SA to CMD Active	63		ns	
T8b	SA Valid Hold from CMD Inactive	42		ns	
T9b	Valid SA to $\overline{\text{IOCS16}}$ Active		100	ns	
T10b	$\overline{\text{IOCS16}}$ Valid Hold from Valid SA	0		ns	
T11b	CMD Active to Inactive	125		ns	
T12b	CMD Inactive to Active	92		ns	*Before* I/O Command
T13b	Active CMD to Valid IOCHRDY		18	ns	
T14b	IOCHRDY Inactive Pulse		12	μs	
T15b	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T16b	DATA Driven from READ CMD Active	0		ns	
T17b	Valid READ Data from CMD Active		54	ns	Applies for Standard Cycles Only
T18b	Valid READ Data from IOCHRDY Active		42	ns	Applies for Ready Cycles Only
T19b	READ Data Hold from CMD Inactive	0		ns	
T20b	READ CMD Inactive to Data Tristate		30	ns	
T21b	CMD to WRITE Data Active		62	ns	
T22b	WRITE Data Hold from CMD Inactive	15		ns	
T23b	WRITE CMD Inactive to Data Tristate		30	ns	
T24b	IOCHRDY Inactive to CMD Active	15		ns	Applies for Early IOCHRDY
T25b	BALE Inactive to CMD Active	55		ns	Applies for Early IOCHRDY
T26b	READ CMD Active to $\overline{\text{DIRx}}$ Active		34	ns	
T27b	READ CMD Inactive to $\overline{\text{DIRx}}$ Inactive		15	ns	

Table 11-5. ISA 8-Bit Memory Access

Parameter	Description	Min	Max	Units	Comments
T1c	BALE Active to Inactive	50		ns	
T2c	BALE Active from Command Inactive	35		ns	
T4c	AEN Valid to Command Active	100		ns	
T5c	AEN Valid from Command Inactive	30		ns	
T7c	SA to CMD Active	63		ns	
T8c	SA Valid Hold from CMD Inactive	42		ns	
T11c	CMD Active to Inactive	125		ns	
T12c	CMD Inactive to Active	60		ns	*Before* Memory Command
T13c	Active CMD to Valid IOCHRDY		18	ns	
T14c	IOCHRDY Inactive Pulse		12	µs	
T15c	CMD Active Hold from IOCHRDY Active	80		ns	Applies to Ready Cycles
T16c	DATA Driven from READ CMD Active	0		ns	
T18c	Valid READ Data from IOCHRDY Active		42	ns	Applies for Ready Cycles Only
T19c	READ Data Hold from CMD Inactive	0		ns	
T20c	READ CMD Inactive to Data Tristate		30	ns	
T21c	CMD to WRITE Data Active		52	ns	
T23c	WRITE CMD Inactive to Data Tristate		30	ns	
T26c	READ CMD Active to $\overline{\text{DIRx}}$ Active		34	ns	
T27c	READ CMD Inactive to $\overline{\text{DIRx}}$ Inactive		15	ns	

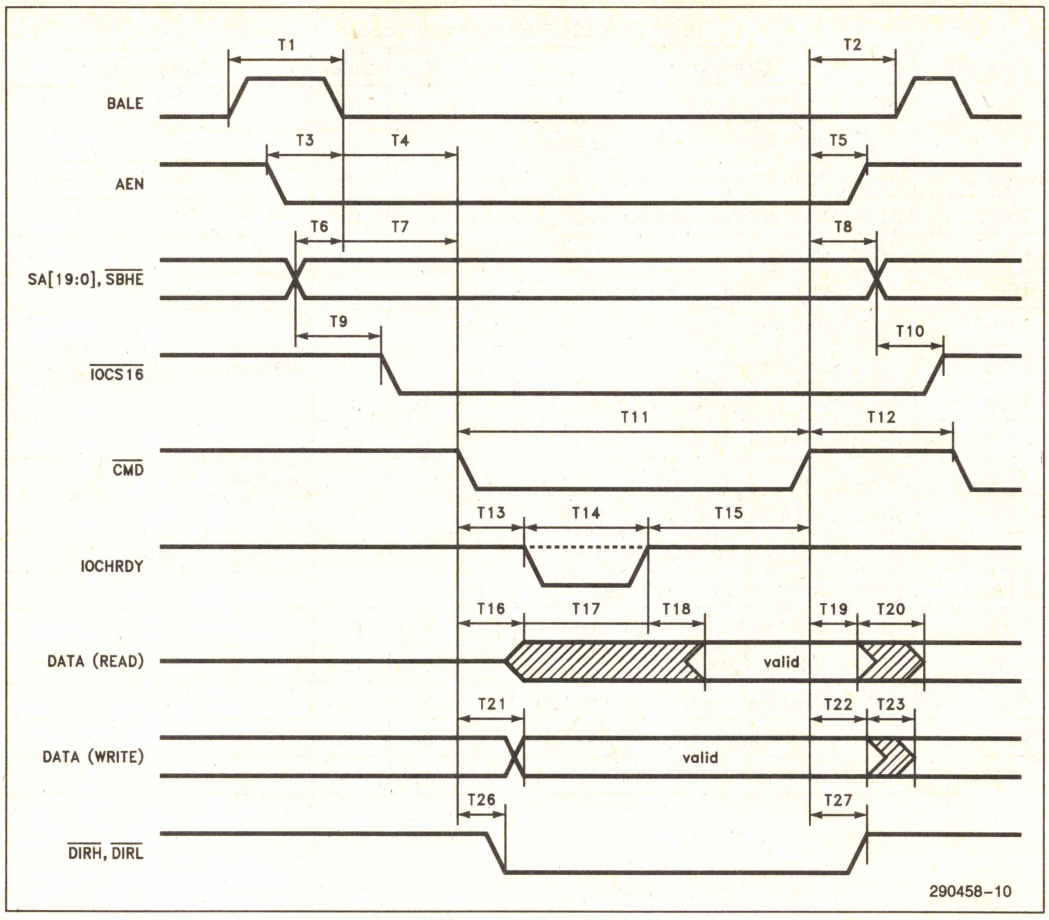


Figure 11-6. ISA-Compatible Cycle

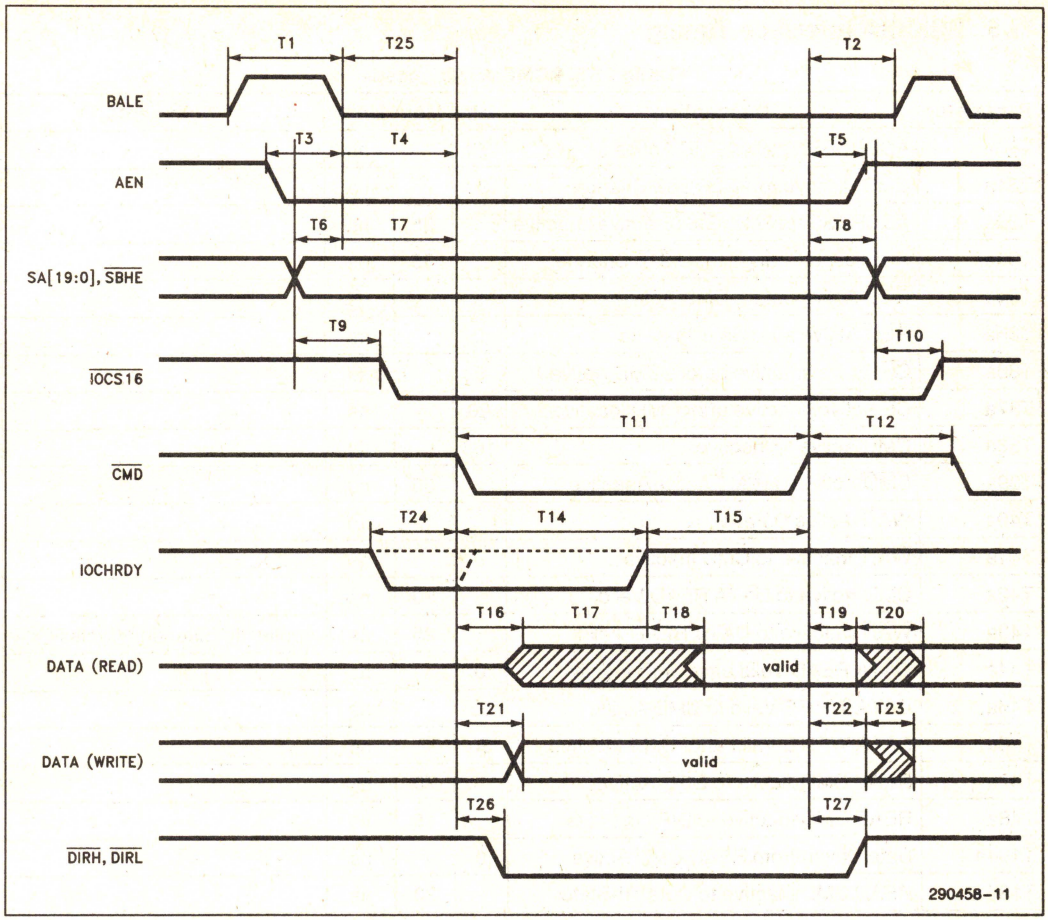


Figure 11-7. Early IOCHRDY Cycle

11.5 PCMCIA Interface Timing

Table 11-6. PCMCIA I/O Access

Parameter	Description	Min	Max	Units	Comments
T30a	ADDRESS Valid to CMD Active	70		ns	
T31a	CMD Inactive to ADDRESS Change	20		ns	
T32a	ADDRESS Valid to $\overline{IOIS16}$ Active/Inactive		35	ns	
T33a	ADDRESS Change to $\overline{IOIS16}$ Change		35	ns	
T34a	$\overline{REG}$ Active before CMD Active	5		ns	
T35a	$\overline{REG}$ Active after CMD Inactive	0		ns	
T36a	$\overline{CE}$ Active/Inactive before CMD Active	5		ns	
T37a	$\overline{CE}$ Active/Inactive after CMD Inactive	20		ns	
T38a	CMD Active to Inactive	165		ns	
T39a	$\overline{CMD}$ Active to $\overline{WAIT}$ Active/Inactive		35	ns	
T40a	$\overline{WAIT}$ Active Duration		12	μs	
T41a	$\overline{WAIT}$ Inactive to CMD Inactive	0		ns	
T42a	CMD Active to DATA READ Valid		90	ns	
T43a	$\overline{WAIT}$ Inactive to DATA READ Valid		25	ns	Applies to Extended Cycles Only
T44a	DATA READ Valid after CMD Inactive	0		ns	
T45a	DATA WRITE Valid to CMD Active	50		ns	
T46a	DATA WRITE Valid after CMD Inactive	30		ns	
T47a	READ CMD Active to $\overline{DIRx}$ Active		70	ns	
T48a	READ CMD Inactive to $\overline{DIRx}$ Inactive		15	ns	
T184a	Data Driven from READ CMD Active	0		ns	
T185a	READ CMD Inactive to Data Tri-State		30	ns	

Table 11-7. PCMCIA Memory Access

Parameter	Description	Min	Max	Units	Comments
T30b	ADDRESS Valid to CMD Active	30		ns	
T31b	CMD Inactive to ADDRESS Change	20		ns	
T34b	$\overline{REG}$ Inactive before CMD Active	30		ns	
T35b	$\overline{REG}$ Inactive after CMD Inactive	20		ns	
T36b	$\overline{CE}$ Active/Inactive before CMD Active	0		ns	
T37b	$\overline{CE}$ Active/Inactive after CMD Inactive	20		ns	
T38b	CMD Active to Inactive	100		ns	
T39b	$\overline{CMD}$ Active to $\overline{WAIT}$ Active/Inactive		35	ns	
T40b	$\overline{WAIT}$ Active Duration		12	µs	
T41b	$\overline{WAIT}$ Inactive to CMD Inactive	0		ns	
T42b	CMD Active to DATA READ Valid		140	ns	
T43b	$\overline{WAIT}$ Inactive to DATA READ Valid		−10	ns	
T44b	DATA READ Valid after CMD Inactive	0		ns	
T45b	CMD Active to DATA WRITE Valid	125		ns	
T46b	DATA WRITE Valid after CMD Inactive	25		ns	
T47b	READ CMD Active to $\overline{DIRx}$ Active		105	ns	
T48b	READ CMD Inactive to $\overline{DIRx}$ Inactive		85	ns	
T184b	Data Driven from READ CMD Active	5		ns	
T185b	READ CMD Inactive to Data Tri-State		100	ns	

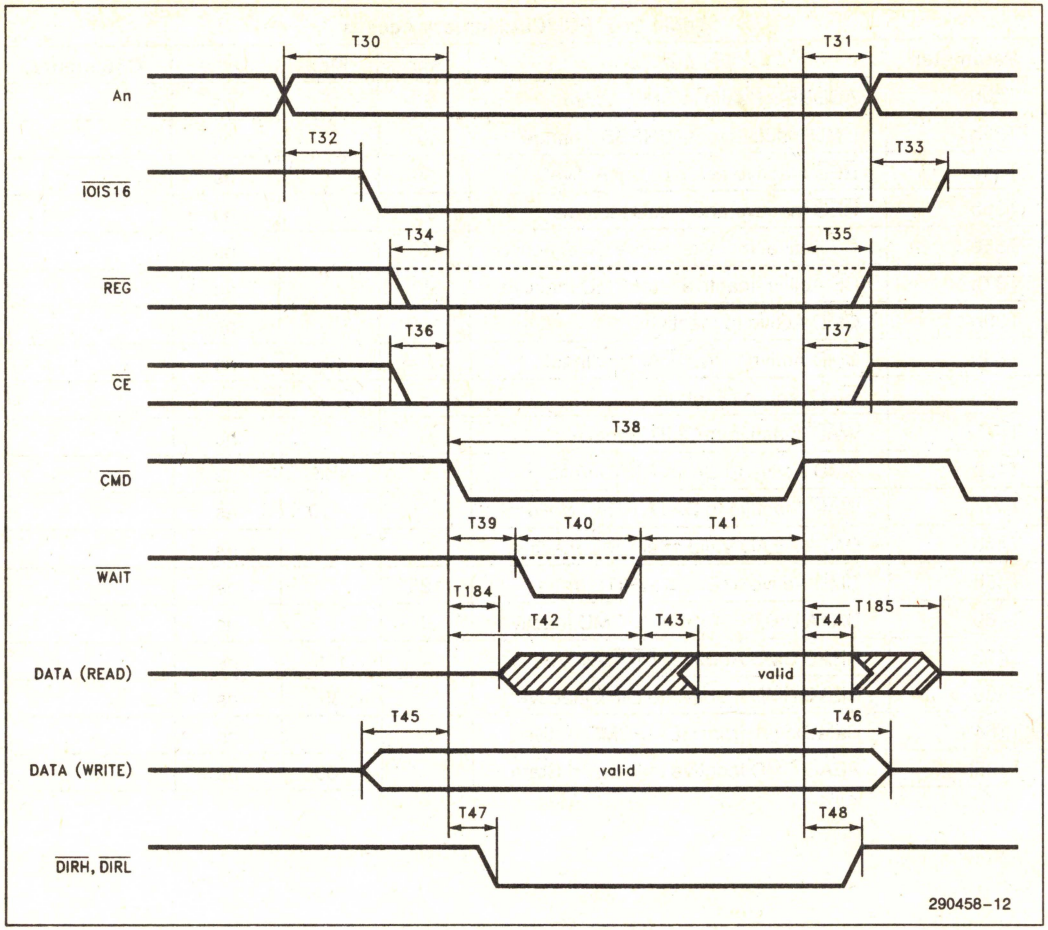


Figure 11-8. PCMCIA Cycle

11.6 Local Memory Timings

11.6.1 DRAM TIMINGS

The 82595 supports up to 80 ns DRAM producing:

Word transfer every 400 ns.

Byte transfer every 250 ns.

Refresh cycle—200 ns.

The 82595 supports 64K x 4 or 256K x 4 DRAM in fast page mode only. Write cycles are produced in *EARLY WRITE* mode. This eliminates the using of the DRAM $\overline{OE}$ signal (it must be connected to GND).

Table 11-8. DRAM—A.C. Characteristics

Symbol	Parameter	Timing		Units	Notes
		Min	Max		
T49	Access Time from $\overline{RAS}$		80	ns	
T50	Access Time from $\overline{CAS}$		30	ns	
T51	Access Time from Column Address		40	ns	
T52	$\overline{CAS}$ to Output Low Z	0		ns	
T53	Output Buffer Turn-Off Delay Time	0	40	ns	
T54	$\overline{RAS}$ Precharge Time	75		ns	
T55	$\overline{RAS}$ Pulse Width	80		ns	
T56	$\overline{RAS}$ Hold Time	30		ns	
T57	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	20		ns	
T58	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	30		ns	
T59	$\overline{CAS}$ Pulse Width	35		ns	
T60	$\overline{CAS}$ Hold Time	80		ns	
T61	Row Address Set-Up Time	0		ns	
T62	Row Address Hold Time	15		ns	
T63	Column Address Set-Up Time	0		ns	
T64	Column Address Hold Time	20		ns	
T65	Column Address Time Referenced to $\overline{RAS}$	65		ns	
T66	$\overline{RAS}$ to Column Address Delay Time	20		ns	
T67	Column Address to $\overline{RAS}$ Lead Time	40		ns	
T68	Write Command Set-Up Time	0		ns	
T69	Write Command Hold Time	15		ns	
T70	Write Command to $\overline{CAS}$ Lead Time	30		ns	
T71	D_{IN} Set-Up Time	0		ns	
T72	D_{IN} Hold Time	15		ns	
T73	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		ns	
T74	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	25		ns	
T75	Fast Page Mode Cycle Time	55		ns	
T76	Fast Page Mode $\overline{CAS}$ Precharge Time	15		ns	
T77	Random Read or Write Cycle Time	190		ns	
T78	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	100		ns	

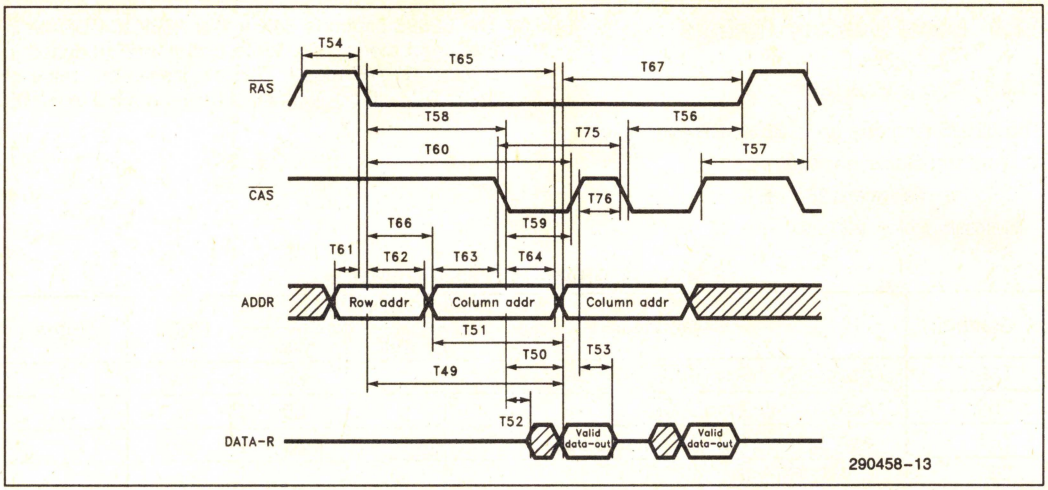


Figure 11-9. DRAM Timing Diagram: Fast Page Mode—Read Cycle

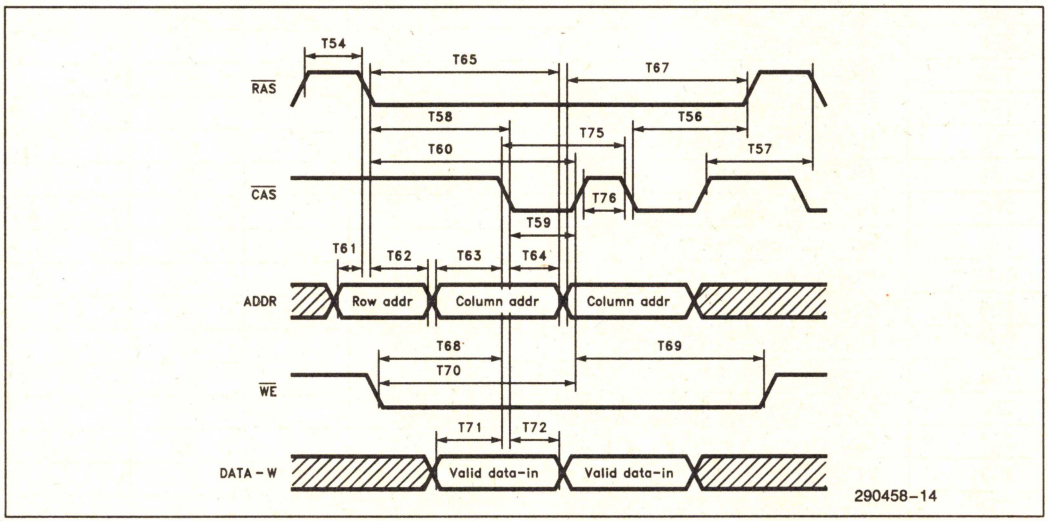


Figure 11-10. DRAM Timing Diagrams: Fast Page Mode—Write Cycle

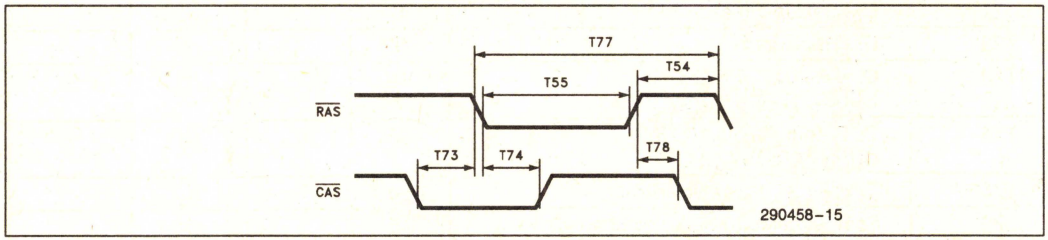


Figure 11-11. DRAM Timing Diagrams: $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

11.6.2 FLASH/EPROM TIMINGS

- The 82595 is designed to support a FLASH or EPROM up to 200 ns access time.
- The V_{PP} signal in FLASH implementation is connected always to 12V. Thus writing to the FLASH is controlled only by the $\overline{WE}$ signal.

Table 11-9. FLASH—A.C. Characteristics

Symbol	Parameter	Min	Max	Units	Notes
T79	Address Access Time		200	ns	
T80	Chip Enable Access Time		200	ns	
T81	Output Enable Access Time		100	ns	
T82	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$	0		ns	
T84	Address Set-Up Time	0			
T85	Address Hold Time	100		ns	
T86	Chip Enable Set-Up Time before Write	15		ns	
T87	Chip Enable Hold Time	0		ns	
T88	Data Set-Up Time	60		ns	
T89	Data Hold Time	15		ns	

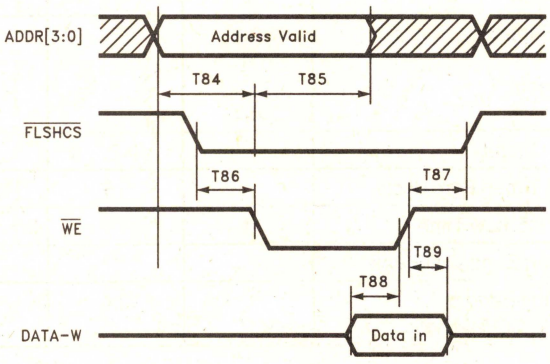


Figure 11-12. FLASH Timings—Write Cycle

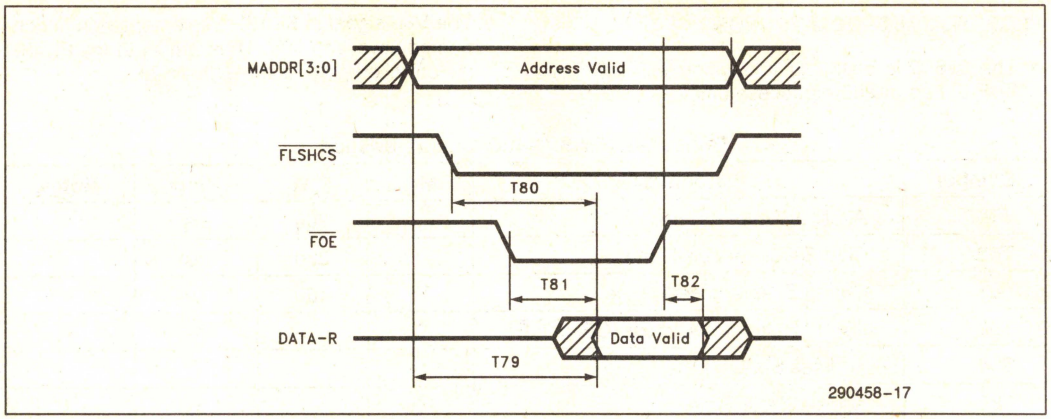
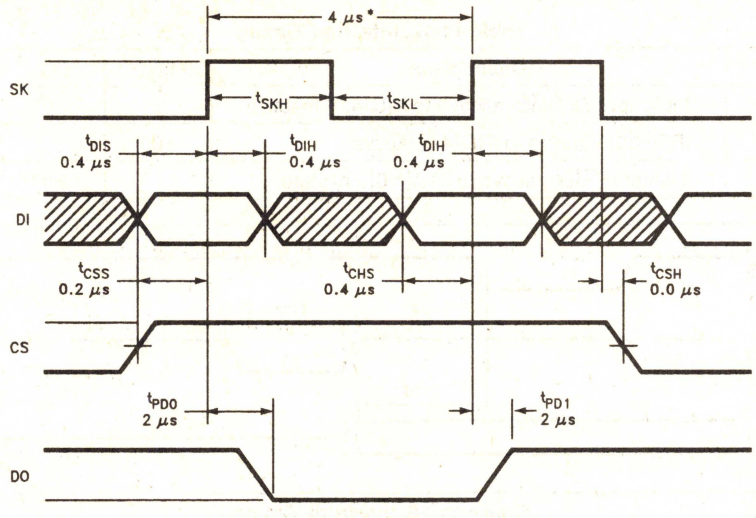


Figure 11-13. Flash Timings—Read Cycle

Table 11-10. EEPROM Timings

Symbol	Parameter	Min	Max	Unit	Notes
	SK Frequency		200	KHz	
t_{SKH}	SK High	3		μs	
t_{SKL}	SK Low	2		μs	
t_{CSS}	CSS Input	0.2		μs	
t_{CSH}		0		μs	
t_{DIS}	DI Input	0.4		μs	
t_{DIH}		0.4		μs	
t_{pd}	DO Output		2	μs	
$t_{E/W}$	Self Timed Pgm Cycle		15	ms	
t_{CS}	Min CS Low Time	1		μs	
t_{SV}	Rising Edge to CS Valid		1	μs	
t_{OH}, t_{IH}	Falling Edge of CS to DO Tri-State		0.4	μs	



NOTE:
*This is the minimum SK period.

Figure 11-14. EEPROM Timings

11.6.3 IA PROM TIMINGS

*The PROM used is a TTL 32 x 8 bit.

Table 11-11. IA PROM A.C. Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
T174	Address Access Time		60	ns	
T175	Chip Enable Access Time		40	ns	

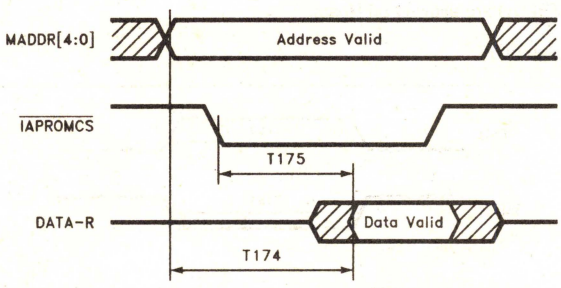


Figure 11-15. IA PROM Timings

11.7 Interrupt Timing

Table 11-12. Interrupt Timing

Parameter	Description	Min	Max	Notes
T177	Interrupt Ack $\overline{CMD}$ Inactive to IRQ[4:0] Inactive		500	
T178	IRQ[4:0] Inactive to IRQ[4:0] Active	100		
T179	Tri-state $\overline{CMD}$ Inactive to IRQ[4:0] Tri-State		500	

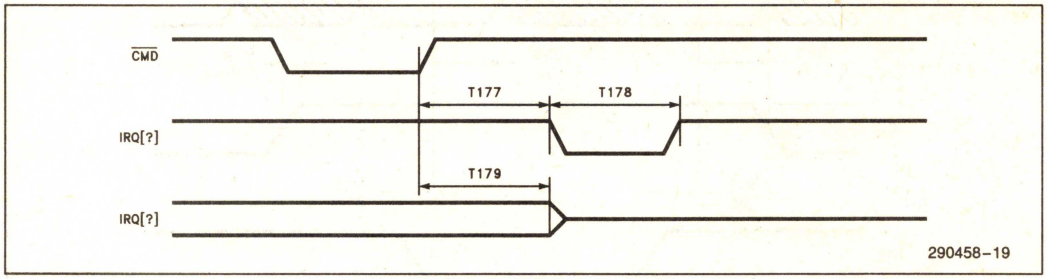


Figure 11-16. Interrupt Timing

11.8 RESET and $\overline{SMOUT}$ Timing

General Comments

- Both signals are asynchronous signals and have minimum pulse duration specification only.
- $\overline{SMOUT}$ during Hardware power down activation.

Table 11-13. RESET and $\overline{SMOUT}$ Timing

Parameter	Description	Min	Max	Units	Notes
T180	RESET Minimum Duration	32		ms	1
T181	$\overline{SMOUT}$ Minimum Duration	100		ns	2
T182	$\overline{SMOUT}$ Activation by Power Down Command	150		ns	3
T183	$\overline{SMOUT}$ Deactivation	25		ns	3

NOTES:
1. Noise spikes of maximum TBD ns are allowed on Reset.
2. $\overline{SMOUT}$ is input.
3. $\overline{SMOUT}$ is output after configuration.

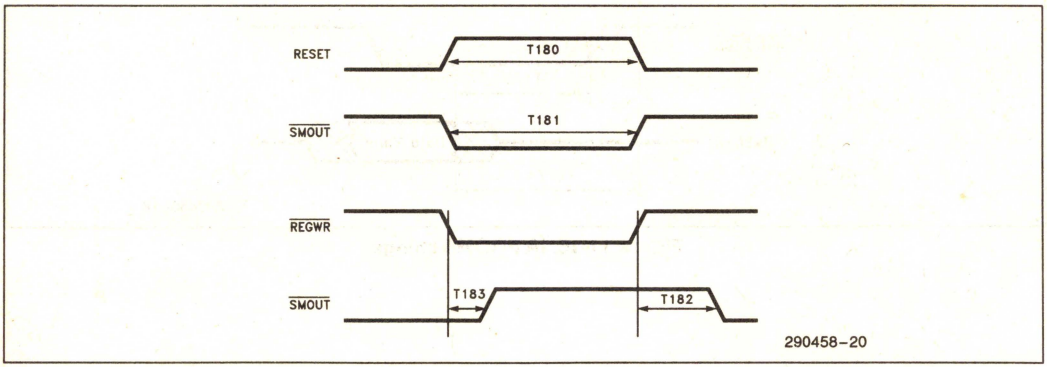


Figure 11-17. $\overline{SMOUT}$ Timing

11.9 JTAG Timing

Table 11-14. 82595 JTAG Timing

Symbol	Parameter	Min	Max	Unit	Notes
T1	TMS Set-Up Time	15		ns	
T2	TMS Hold Time	10		ns	
T3	TDI Set-Up Time	10		ns	
T4	TDI Hold Time	10		ns	
T5	Input Signals Set-Up Time	15		ns	
T6	Input Signals Hold Time	10		ns	
T7	Outputs Valid Delay		150	ns	
T8	TDO Valid Delay		40	ns	

NOTES:
TCK 20 MHz, 50% duty cycle.
$4.5V < V_{CC} < 5.45V$
Data sheet values for V_{OH}, V_{OL}, I_{OH}, I_{OL} used.
Measurements taken at 105°C (worst case temp.).

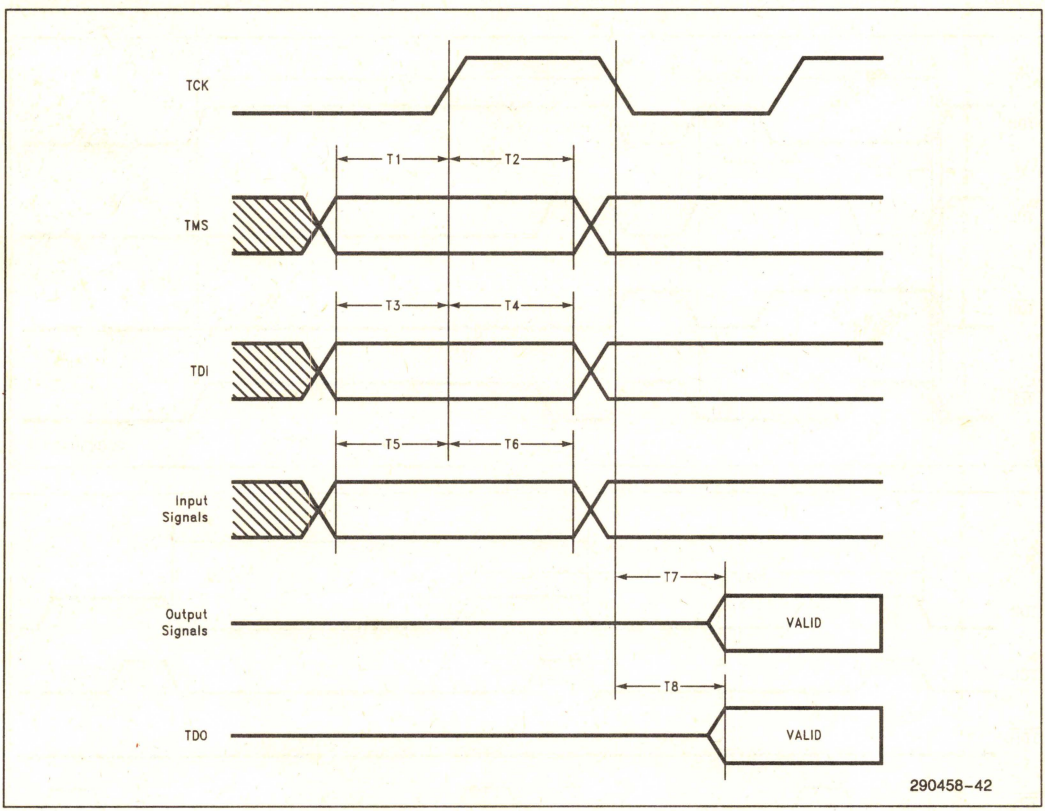
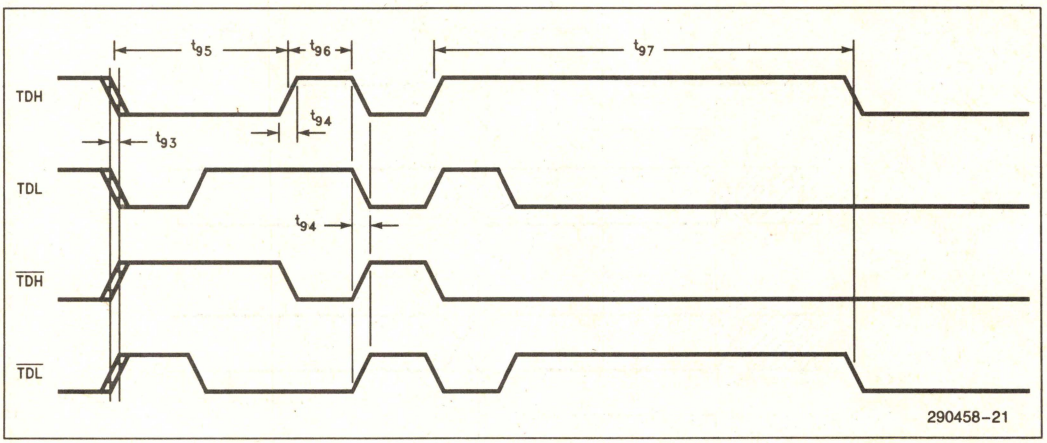


Figure 11-18. 82595 JTAG Timing

11.10 Serial Timings

Table 11-15. TPE Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{90}	Number of TxD Bit Loss at Start of Packet			2	bits
t_{91}	Internal Steady State Propagation Delay			400	ns
t_{92}	Internal Start UP Delay			600	ns
t_{93}	TDH and TDL Pairs Edge Skew (@ $V_{CC}/2$)		1.5	3	ns
t_{94}	TDH and TDL Pairs Rise/Fall Times (@ 0.5V to V_{CC} − 0.5V)		2	5	ns
t_{95}	TDH and TDL Pairs Bit Cell Center to Center	99	100	101	ns
t_{96}	TDH and TDL Pairs Bit Cell Center to Boundary	49	50	51	ns
t_{97}	TDH and TDL Pairs Return to Zero from Last TDH	250		400	ns
t_{98}	Link Test Pulse Width	98	100	100	ns
t_{99}	Last TD Activity to Link Test Pulse	8	13	24	ms
t_{100}	Link Test Pulse to Data Separation	190	200		ns



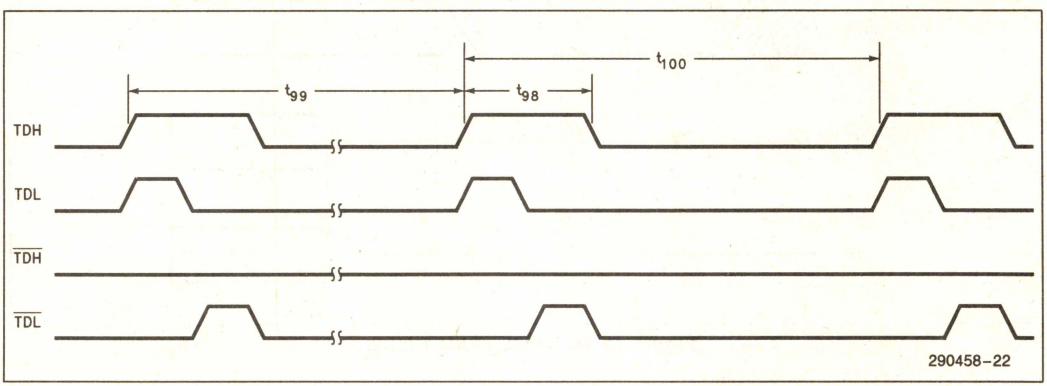


Figure 11-19. TPE Transmit Timings (Link Test Pulse)

Table 11-16. TPE Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{105}	RD to RxD Bit Loss at Start of Packet	4		19	bits
t_{106}	RD Invalid Bits Allowed at Start of Packet			1	bits
t_{107}	RD to Internal Steady State Propagation Delay			400	ns
t_{108}	RD to Internal Start Up Delay			2.4	μs
t_{109}	RD Pair Bit Cell Center Jitter			±13.5	ns
t_{110}	RD Pair Bit Cell Boundry Jitter			±13.5	ns
t_{111}	RD Pair Held High from Last Valid Position Transition	230		400	ns
t_{112}	Internal $\overline{CRS}$ Assertion Delay			700	ns
t_{113}	Internal $\overline{CRS}$ Deassertion Delay			450	ns

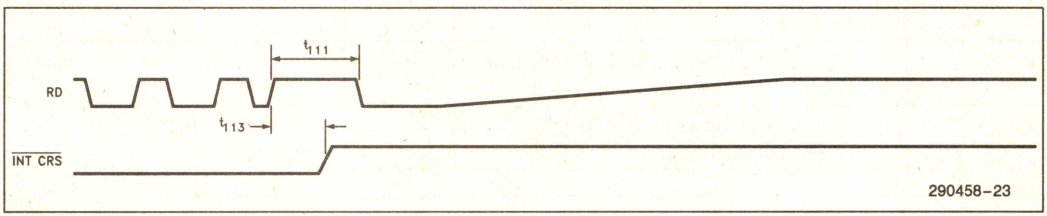


Figure 11-20. TPE Receive Timings (End of Frame)

Table 11-17. TPE Collision Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{115}	Onset of Collision (RD Pair and Internal $\overline{RTS}$ Active) to Internal CDT			9	bits
t_{116}	End of Collision (RD Pair or Internal $\overline{RTS}$ Inactive) to Internal CDT Deassert			9	bits

Table 11-18. TPE Link Integrity Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{120}	Last RD Activity to Link Fault (Link Loss Timer)	50	100	150	ms
t_{121}	Minimum Received Linkbeat Separation(1)	2	5	7	ms
t_{122}	Maximum Received Linkbeat Separation(2)	25	50	150	ms

NOTES:
1. Linkbeats closer in time to this value are considered noise, and rejected.
2. Linkbeats further apart in time than this value are not considered consecutive and are rejected.

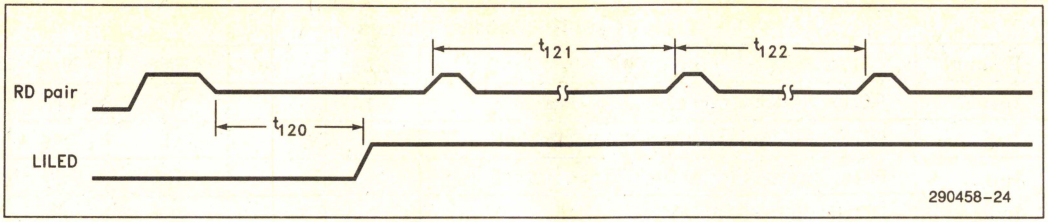


Figure 11-21. TPE Link Integrity Timings

Table 11-19. AUI Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{126}	TRMT Pair Rise/Fall Times		3	5	ns
t_{127}	Bit Cell Center to Bit Cell Center of TRMT Pair	99.5	50	100.5	ns
t_{128}	Bit Cell Center to Bit Cell Boundary of TRMT Pair	49.5	50	50.5	ns
t_{129}	TRMT Pair Held at Positive Differential at Start of Idle	200			ns
t_{130}	TRTM Pair Return to ≤40 mVp from Last Positive Transition			8.0	μs

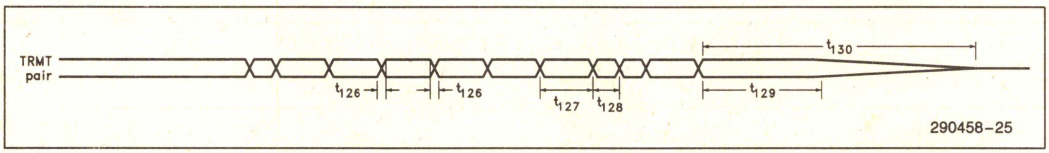


Figure 11-22. AUI Transmit Timings

Table 11-20. AUI Receive Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{135}	RCV Pair Rise/Fall Times			10	ns
t_{136}	RCV Pair Bit Cell Center Jitter in Preamble			±12	ns
t_{137}	RCV Pair Bit Cell Center/Boundary Jitter in Data			±18	ns
t_{138}	RCV Pair Idle Time after Transmission	8			μs
t_{139}	RCV Pair Return to Zero from Last Positive Transition	160			ns

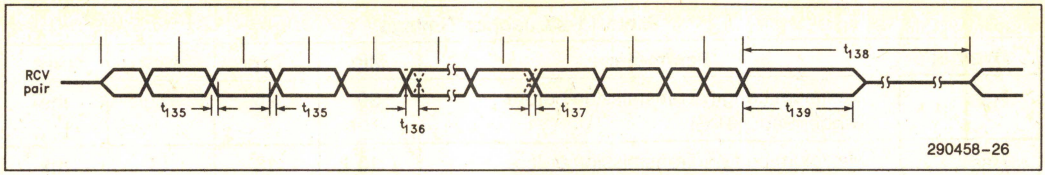


Figure 11-23. AUI Receive Timings

Table 11-21. AUI Collision Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{145}	CLSN Pair Cycle Time	80		118	ns
t_{146}	CLSN Pair Rise/Fall Times			10	ns
t_{147}	CLSN Pair Return to Zero from Last Positive Transition	160			ns
t_{148}	CLSN Pair High/Low Times	35		70	ns

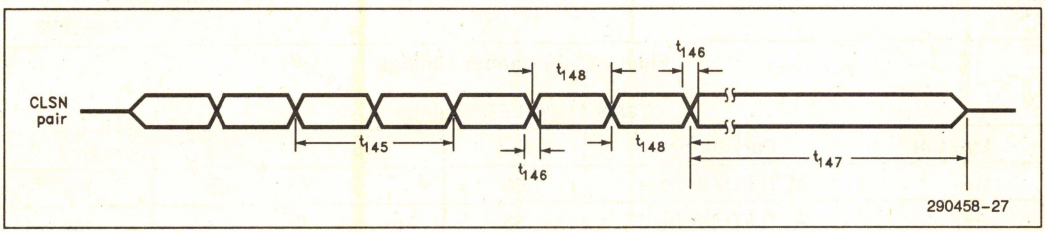


Figure 11-24. AUI Collision Timings

Table 11-22. AUI Noise Filter Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{152}	RCV Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns
t_{153}	CLSN Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns

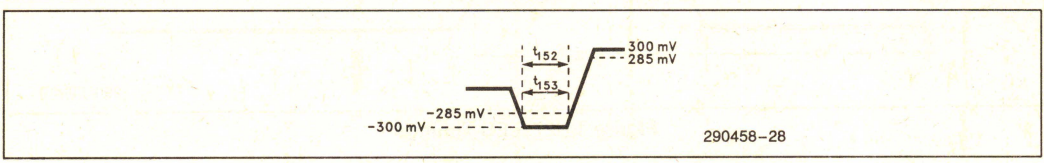


Figure 11-25. AUI Noise Filter Timings

Table 11-23. Jabber Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{165}	Maximum Length Transmission before Jabber Fault (TPE)	20	25	150	ms
t_{166}	Maximum Length Transmission before Jabber Fault (AUI)	10	13	18	ms
t_{167}	Minimum Idle Time to Clear Jabber Function	250	275	750	ms

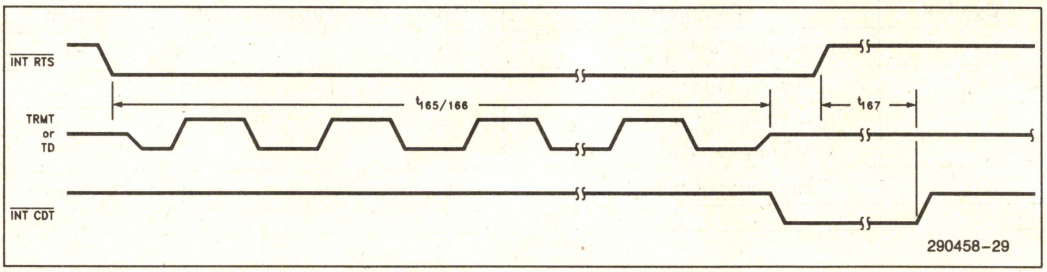


Figure 11-26. Jabber Timings

Table 11-24. LED Timings

Symbol	Parameter	Min	Typ	Max	Unit
t_{170}	ACTLED On Time	50		450	ms
t_{171}	ACTLED Off Time	50			ms
t_{172}	LILED On Time	50			ms
t_{173}	LILED Off Time	100			ms

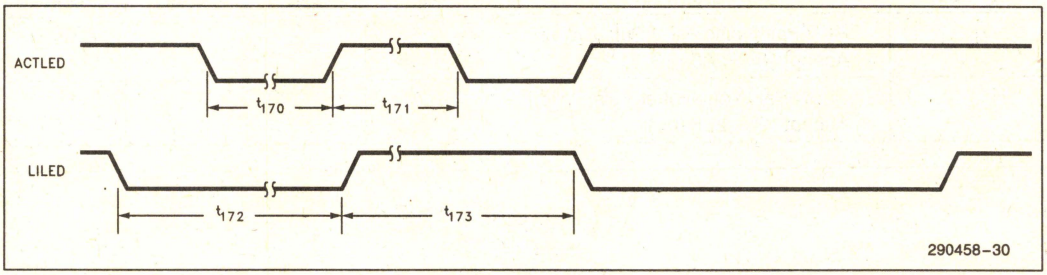


Figure 11-27. LED Timings

12.0 REVISION SUMMARY

The following list represents key differences between version -002 and version -003 of the 82595 Ethernet Controller Data Sheet.

Section 2.3 Pin type of FL/IADATA4-7 and EEPROMDO have been corrected.

Section 2.8 Power Down states using SMOUT# or software command have been clarified.

Section 4.1.3 The MC ALL bit has been deleted. The default value is 0.

Section 4.5 The EEPROM Register 0 contents have been changed and corrected.

Section 10.5 Figure 10-1, 10-5 have been changed for correct resistor values (R5–R8).

Section 11.1 Table 11-1. V_{IH} (jumpr) has been added; also, several chip signals have been added to note 11.

Section 11.3 The inductor value used in parallel with the load resistor is incorrect. The correct value is 27 μH ±5%.

Section 11.5 Figure 11-8. T184 and T185 timings have been added to the diagram. IOCS16# is incorrect in the diagram. The correct pin is IOIS16#.

Section 11.6.2 T83 has been deleted. Figure 11-14, EEPROM timings have been added.

Section 11.6.3 T176 has been deleted.

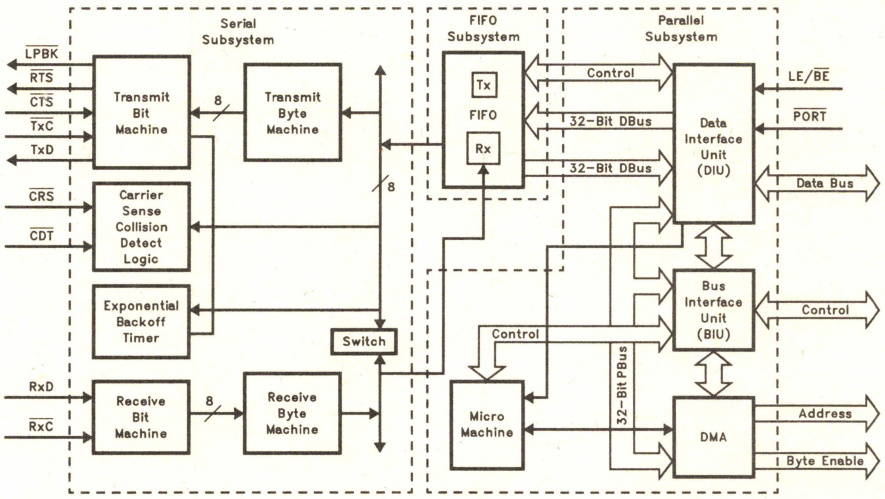
Section 11.9 JTAG timings have been added.

82596CA
HIGH-PERFORMANCE 32-BIT LOCAL AREA NETWORK COPROCESSOR

- **Performs Complete CSMA/CD Medium Access Control (MAC) Functions—Independently of CPU**
  - — IEEE 802.3 (EOC) Frame Delimiting
  - — HDLC Frame Delimiting
- **Supports Industry Standard LANs**
  - — IEEE TYPE 10BASE-T, IEEE TYPE 10BASE5 (Ethernet*), IEEE TYPE 10BASE2 (Cheapernet), IEEE TYPE 1BASE5 (StarLAN), and the Proposed Standard 10BASE-F
  - — Proprietary CSMA/CD Networks Up to 20 Mb/s
- **On-Chip Memory Management**
  - — Automatic Buffer Chaining
  - — Buffer Reclamation after Receipt of Bad Frames; Optional Save Bad Frames
  - — 32-Bit Segmented or Linear (Flat) Memory Addressing Formats
- **Network Management and Diagnostics**
  - — Monitor Mode
  - — 32-Bit Statistical Counters
- **82586 Software Compatible**
- **Self-Test Diagnostics**
- **Optimized CPU Interface**
  - — Optimized Bus Interface to Intel's i486™DX, i486™SX, i487™SX and 80960CA Processors
  - — 33 MHz, 25 MHz, 20 MHz and 16 MHz Clock Frequencies
  - — Supports Big Endian and Little Endian Byte Ordering
- **32-Bit Bus Master Interface**
  - — 106 MB/s Bus Bandwidth
  - — Burst Bus Transfers
  - — Bus Throttle Timers
  - — Transfers Data at 100% of Serial Bandwidth
  - — 128-Byte Receive FIFO, 64-Byte Transmit FIFO
- **Configurable Initialization Root for Data Structures**
- **High-Speed, 5V, CHMOS** IV Technology**
- **132-Pin Plastic Quad Flat Pack (PQFP) and PGA Package**

  (See Packaging Spec Order No. 240800-001, Package Type KU and A)

i486 is a trademark of Intel Corporation.
*Ethernet is a registered trademark of Xerox Corporation.
**CHMOS is a patented process of Intel Corporation.



290218-1

Figure 1. 82596CA Block Diagram

October 1993
Order Number: 290218-006

82596CA High-Performance 32-Bit Local Area Network Coprocessor

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INTRODUCTION

The 82596CA is an intelligent, high-performance 32-bit Local Area Network coprocessor. The 82596CA implements the CSMA/CD access method and can be configured to support all existing IEEE 802.3 standards—TYPEs 10BASE-T, 10BASE5, 10BASE2, 1BASE5, and 10BROAD36. It can also be used to implement the proposed standard TYPE 10BASE-F. The 82596CA performs high-level commands, command chaining, and interprocessor communications via shared memory, thus relieving the host CPU of many tasks associated with network control. All time-critical functions are performed independently of the CPU, this increases network performance and efficiency. The 82596CA bus interface is optimized for Intel's i486™SX, i486™DX, i487™SX, 80960CA, and 80960KB processors.

The 82596CA implements all IEEE 802.3 Medium Access Control and channel interface functions, these include framing, preamble generation and stripping, source address generation, destination address checking, short-frame detection, and automatic length-field handling. Data rates up to 20 Mb/s are supported.

The 82596CA provides a powerful host system interface. It manages memory structures automatically, with command chaining and bidirectional data chaining. An on-chip DMA controller manages four channels, this allows autonomous transfer of data blocks (buffers and frames) and relieves the CPU of byte transfer overhead. Buffers containing errored or collided frames can be automatically recovered without CPU intervention. The 82596CA provides an upgrade path for existing 82586 software drivers by providing an 82586-software-compatible mode that supports the current 82586 memory structure. The 82586CA also has a Flexible memory structure and a Simplified memory structure. The 82596CA can address up to 4 gigabytes of memory. The 82596CA supports Little Endian and Big Endian byte ordering.

The 82596CA bus interface can achieve a burst transfer rate of 106 MB/s at 33 MHz. The bus interface employs bus throttle timers to regulate 82596CA bus use. Two large, independent FIFOs—128 bytes for Receive and 64 bytes for Transmit—tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case bus latency. The high-performance bus is capable of back-to-back transmission and reception during the IEEE 802.3 9.6-μs Interframe Spacing (IFS) period.

The 82596CA provides a wide range of diagnostics and network management functions, these include internal and external loopback, exception condition tallies, channel activity indicators, optional capture of all frames regardless of destination address (promiscuous mode), optional capture of errored or collided frames, and time domain reflectometry for locating fault points on the network cable. The statistical counters, in 32-bit segmented and linear modes, are 32-bits each and include CRC errors, alignment errors, overrun errors, resource errors, short frames, and received collisions. The 82596CA also features a monitor mode for network analysis. In this mode the 82596CA can capture status bytes, and update statistical counters, of frames monitored on the link without transferring the contents of the frames to memory. This can be done concurrently while transmitting and receiving frames destined for that station.

The 82596CA can be used in both baseband and broadband networks. It can be configured for maximum network efficiency (minimum contention overhead) with networks of any length. Its highly flexible CSMA/CD unit supports address field lengths of zero through six bytes—configurable to either IEEE 802.3/Ethernet or HDLC frame delimitation. It also supports 16- or 32-bit cyclic redundancy checks. The CRC can be transferred directly to memory for receive operations, or dynamically inserted for transmit operations. The CSMA/CD unit can also be configured for full duplex operation for high throughput in point-to-point connections.

The 82596 C-step incorporates several new features not found in previous steppings. The following is a summary of the 82596 C-step's new features.

- The 82596 C-step fixes Errata found in the A1 and B steppings.
- The 82596 C-step has improved AC timings over both the A and B steppings.
- The 82596 C-step has a New Enhanced Big Endian Mode where in Linear Addressing Mode, true 32-bit Big Endian functionality is achieved. New Enhanced Big Endian Mode is enabled by setting bit 7 of the SYSBUS byte. This mode is software compatible with the big endian mode of the B-step with one exception—no 32-bit addresses need to be swapped by software in the C-step. In this new mode, the 82596 C-step treats 32-bit address pointers as true 32-bit entities and the SCB absolute address and statistical counters are still treated as two 16-bit big endian entities. Not setting this mode will configure the 82596 C-step to be 100% compatible to the A1-step big endian mode.
- The 82596 C-step is hardware and software compatible to both the A1 and B steppings allowing for easy "drop-in" to current designs. Pinout and control structures remain unchanged.

The 82596CA is fabricated with Intel's reliable, 5-V, CHMOS IV (process 648.8) technology. It is available in a 132-pin PQFP or PGA package.

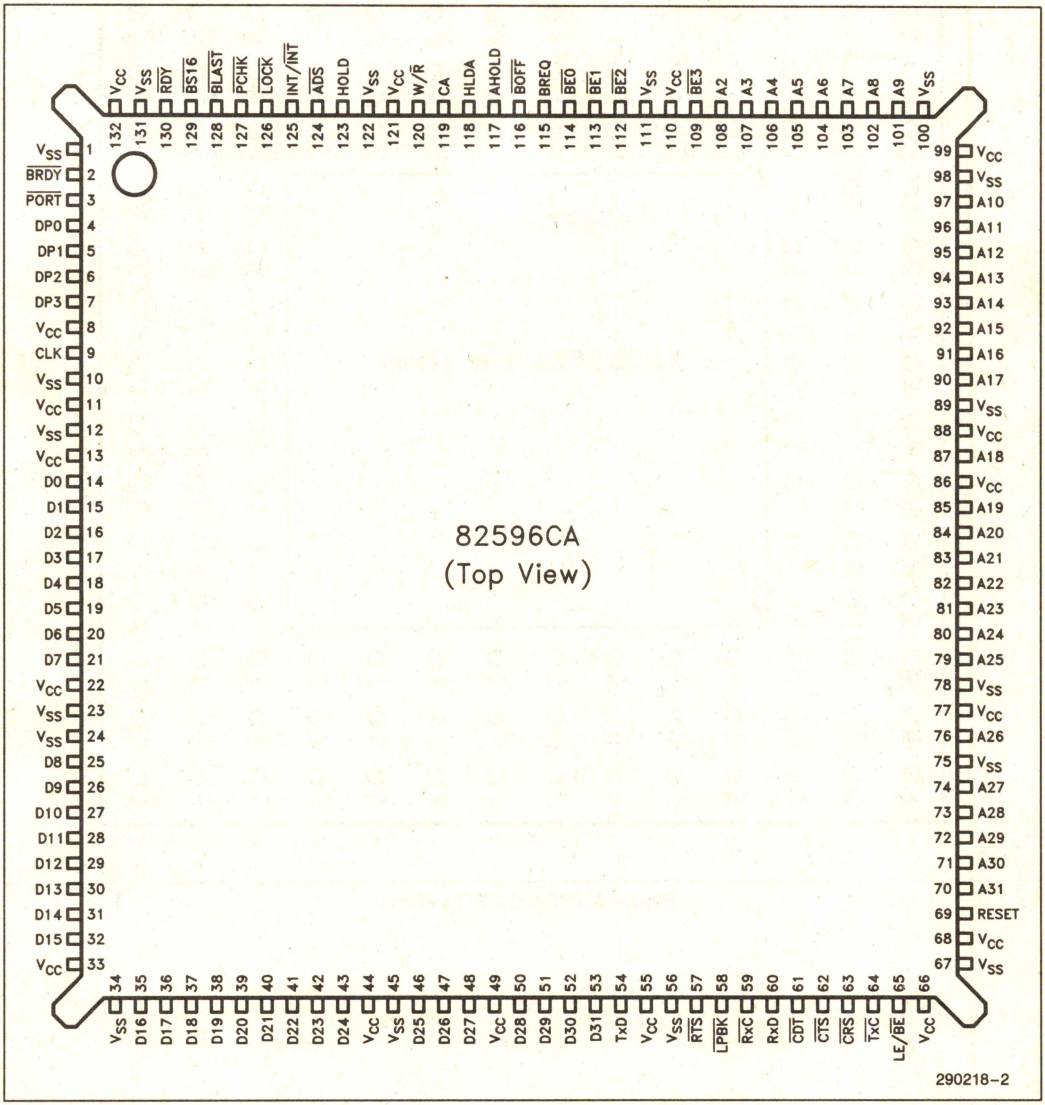


Figure 2. 82596CA PQFP Pin Configuration

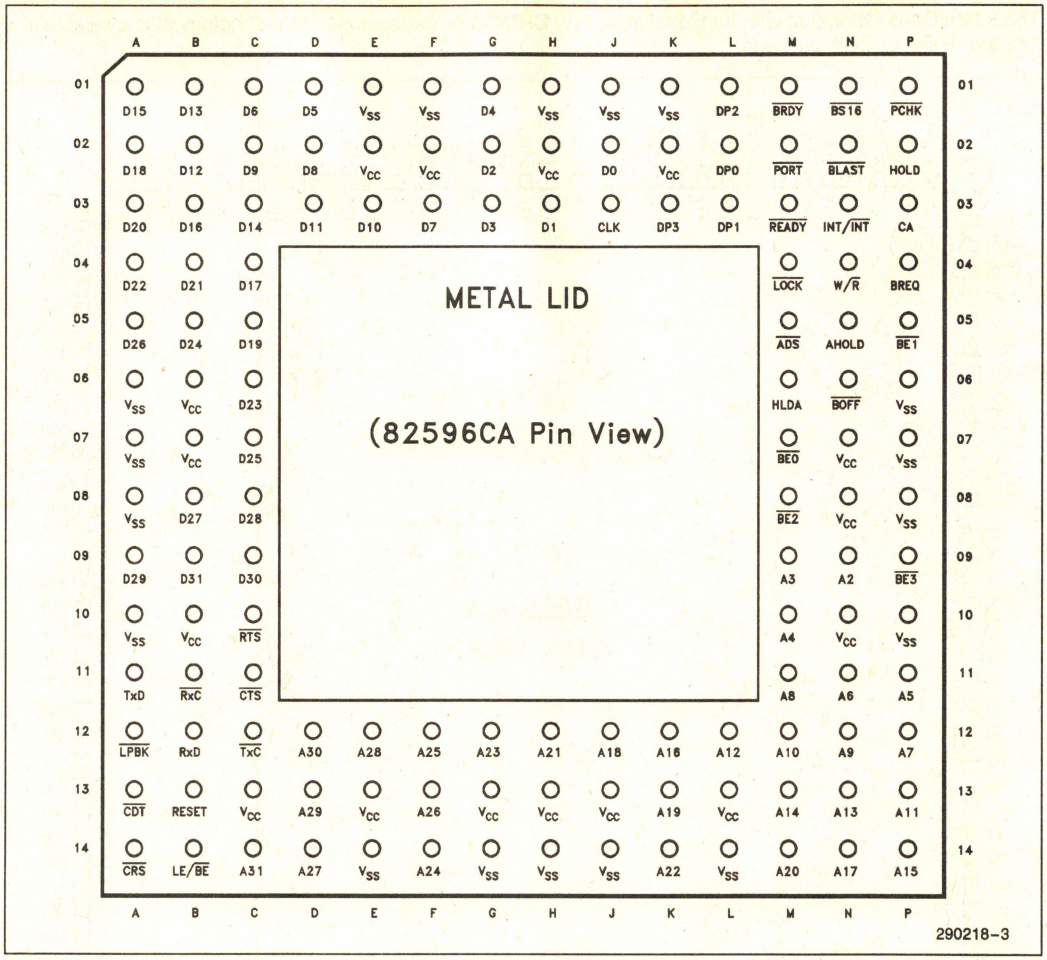


Figure 3. 82596CA PGA Pinout

82596CA PGA Cross Reference by Pin Name

Address		Data		Control		Serial Interface		V_{CC}	V_{SS}
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Pin No.	Pin No.
A2	N9	D0	J2	$\overline{ADS}$	M5	$\overline{CDT}$	A13	B6	A6
A3	M9	D1	H3	AHOLD	N5	$\overline{CRS}$	A14	B7	A7
A4	M10	D2	G2	$\overline{BE0}$	M7	$\overline{CTS}$	C11	B10	A8
A5	P11	D3	G3	$\overline{BE1}$	P5	$\overline{LPBK}$	A12	C13	A10
A6	N11	D4	G1	$\overline{BE2}$	M8	$\overline{RTS}$	C10	E2	E1
A7	P12	D5	D1	$\overline{BE3}$	P9	$\overline{RxC}$	B11	E13	E14
A8	M11	D6	C1	$\overline{BLAST}$	N2	$\overline{RxD}$	B12	F2	F1
A9	N12	D7	F3	$\overline{BOFF}$	N6	$\overline{TxC}$	C12	G13	G14
A10	M12	D8	D2	$\overline{BRDY}$	M1	TxD	A11	H2	H1
A11	P13	D9	C2	BREQ	P4			H13	H14
A12	L12	D10	E3	$\overline{BS16}$	N1			J13	J1
A13	N13	D11	D3	CA	P3			K2	J14
A14	M13	D12	B2	CLK	J3			L13	K1
A15	P14	D13	B1	DP0	L2			N7	L14
A16	K12	D14	C3	DP1	L3			N8	P6
A17	N14	D15	A1	DP2	L1			N10	P7
A18	J12	D16	B3	DP3	K3				P8
A19	K13	D17	C4	HLDA	M6				P10
A20	M14	D18	A2	HOLD	P2				
A21	H12	D19	C5	INT/$\overline{INT}$	N3				
A22	K14	D20	A3	LE/$\overline{BE}$	B14				
A23	G12	D21	B4	$\overline{LOCK}$	M4				
A24	F14	D22	A4	$\overline{PCHK}$	P1				
A25	F12	D23	C6	$\overline{PORT}$	M2				
A26	F13	D24	B5	$\overline{READY}$	M3				
A27	D14	D25	C7	RESET	B13				
A28	E12	D26	A5	W/$\overline{R}$	N4				
A29	D13	D27	B8						
A30	D12	D28	C8						
A31	C14	D29	A9						
		D30	C9						
		D31	B9						

PIN DESCRIPTIONS

<table>
<tr><th>Symbol</th><th>PQFP Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>CLK</td><td>9</td><td>I</td><td>CLOCK. The system clock input provides the fundamental timing for the 82596. It is a 1X CLK input used to generate the 82596 clock and requires TTL levels. All external timing parameters are specified in reference to the rising edge of CLK.</td></tr>
<tr><td>D0–D31</td><td>14–53</td><td>I/O</td><td>DATA BUS. The 32 Data Bus lines are bidirectional, tri-state lines that provide the general purpose data path between the 82596 and memory. With the 82596 the bus can be either 16 or 32 bits wide; this is determined by the $\overline{BS16}$ signal. The 82596 always drives all 32 data lines during Write operations, even with a 16-bit bus. D31– D0 are floated after a Reset or when the bus is not acquired.
These lines are inputs during a CPU Port access; in this mode the CPU writes the next address to the 82596 through the data lines. During $\overline{PORT}$ commands (Relocatable SCP, Self-Test, Reset and Dump) the address must be aligned to a 16-byte boundary. This frees the D_3–D_0 lines so they can be used to distinguish the commands. The following is a summary of the decoding data.
<table>
<tr><th>D0</th><th>D1</th><th>D2</th><th>D3</th><th>D31–D4</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0000</td><td>Reset</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>ADDR</td><td>Relocatable SCP</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>ADDR</td><td>Self-Test</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>ADDR</td><td>Dump Command</td></tr>
</table></td></tr>
<tr><td>DP0–DP3</td><td>4–7</td><td>I/O</td><td>DATA PARITY. These are tri-stated data parity pins. There is one parity line for each byte of the data bus. The 82596 drives them with even-parity information during write operations having the same timing as data writes. Likewise, even-parity information, with the same timing as read information, must be driven back to the 82596 over these pins to ensure that the correct parity check status is indicated by the 82596.</td></tr>
<tr><td>$\overline{PCHK}$</td><td>127</td><td>O</td><td>PARITY CHECK. This pin is driven high one clock after $\overline{RDY}$ to inform Read operations of the parity status of data sampled at the end of the previous clock cycle. When driven low it indicates that incorrect parity data has been sampled. It only checks the parity status of enabled bytes, which are indicated by the Byte Enable and Bus Size signals. $\overline{PCHK}$ is only valid for one clock time after data read is returned to the 82596; i.e., it is inactive (high) at all other times.</td></tr>
<tr><td>A31-A2</td><td>70–108</td><td>O</td><td>ADDRESS LINES. These 30 tri-stated Address lines output the address bits required for memory operation. These lines are floated after a Reset or when the bus is not acquired.</td></tr>
<tr><td>$\overline{BE3}$–$\overline{BE0}$</td><td>109–114</td><td>O</td><td>BYTE ENABLE. These tri-stated signals are used to indicate which bytes are involved with the current memory access. The number of Byte Enable signals asserted indicates the physical size of the data being transferred (1, 2, 3, or 4 bytes).
• $\overline{BE0}$ indicates D7–D0
• $\overline{BE1}$ indicates D15–D8
• $\overline{BE2}$ indicates D23–D16
• $\overline{BE3}$ indicates D31–D24
These lines are floated after a Reset or when the bus is not acquired.</td></tr>
<tr><td>W/$\overline{R}$</td><td>120</td><td>O</td><td>WRITE/READ. This dual function pin is used to distinguish Write and Read cycles. This line is floated after a Reset or when the bus is not acquired.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
$\overline{ADS}$	124	O	**ADDRESS STATUS.** The 82596 uses this tri-state pin to indicate to indicate that a valid bus cycle has begun and that A31–A2, $\overline{BE3}$–$\overline{BE0}$, and W/$\overline{R}$ are being driven. It is asserted during t1 bus states. This line is floated after a Reset or when the bus is not acquired.
$\overline{RDY}$	130	I	**READY.** Active low. This signal is the acknowledgment from addressed memory that the transfer cycle can be completed. When high, it causes wait states to be inserted. It is ignored at the end of the first clock of the bus cycle's data cycle. This active-low signal does not have an internal pull-up resistor. This signal must meet the setup and hold times to operate correctly.
$\overline{BRDY}$	2	I	**BURST READY.** Active low. Burst Ready, like $\overline{RDY}$, indicates that the external system has presented valid data on the data pins in response to a Read, or that the external system has accepted the 82596 data in response to a Write request. Also, like $\overline{RDY}$, this signal is ignored at the end of the first clock in a bus cycle. If the 82596 can still receive data from the previous cycle, ADS will not be asserted in the next clock cycle; however, Address and Byte Enable will change to reflect the next data item expected by the 82596. $\overline{BRDY}$ will be sampled during each succeeding clock and if active, the data on the pins will be strobed to the 82596 or to external memory (read/write). $\overline{BRDY}$ operates exactly like READY during the last data cycle of a burst sequence and during nonburstable cycles.
$\overline{BLAST}$	128	O	**BURST LAST.** A signal (active low) on this tri-state pin indicates that the burst cycle is finished and when $\overline{BRDY}$ is next returned it will be treated as a normal ready; i.e., another set of addresses will be driven with $\overline{ADS}$ or the bus will go idle. $\overline{BLAST}$ is not asserted if the bus is not acquired.
AHOLD	117	I	**ADDRESS HOLD.** This hold signal is active high, it allows another bus master to access the 82596 address bus. In a system where an 82596 and an i486 processor share the local bus, AHOLD allows the cache controller to make a cache invalidation cycle while the 82596 holds the address lines. In response to a signal on this pin, the 82596 immediately (i.e. during the next clock) stops driving the entire address bus (A31–A2); the rest of the bus can remain active. For example, data can be returned for a previously specified bus cycle during Address Hold. The 82596 will not begin another bus cycle while AHOLD is active.
$\overline{BOFF}$	116	I	**BACKOFF.** This signal is active low, it informs the 82596 that another bus master requires access to the bus before the 82596 bus cycle completes. The 82596 immediately (i.e. during the next clock) floats its bus. Any data returned to the 82596 while $\overline{BOFF}$ is asserted is ignored. $\overline{BOFF}$ has higher priority than $\overline{RDY}$ or $\overline{BRDY}$; if two such signals are returned in the same clock period, $\overline{BOFF}$ is given preference. The 82596 remains in Hold until $\overline{BOFF}$ goes high, then the 82596 resumes its bus cycle by driving out the address and status, and asserting $\overline{ADS}$.
$\overline{LOCK}$	126	O	**LOCK.** This tri-state pin is used to distinguish locked and unlocked bus cycles. $\overline{LOCK}$ generates a semaphore handshake to the CPU. $\overline{LOCK}$ can be active for several memory cycles, it goes active during the first locked memory cycle (t1) and goes inactive at the last locked cycle (t2). This line is floated after a Reset or when the bus is not acquired. $\overline{LOCK}$ can be disabled via the sysbus byte in software.

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
$\overline{BS16}$	129	I	**BUS SIZE.** This signal allows the 82596CA to work with either 16- or 32-bit bytes. Inserting $\overline{BS16}$ low causes the 82596 to perform two 16-bit memory accesses when transferring 32-bit data. In little endian mode the D15–D0 lines are driven when $\overline{BS16}$ is inserted, in Big Endian mode the D31–D16 lines are driven.
HOLD	123	O	**HOLD.** The HOLD signal is active high, the 82596 uses it to request local bus mastership. In normal operation HOLD goes inactive before HLDA. The 82596 can be forced off the bus by deasserting HLDA or if the bus throttle timers expire.
HLDA	118	I	**HOLD ACKNOWLEDGE.** The HLDA signal is active high, it indicates that bus mastership has been given to the 82596. HLDA is internally synchronized; after HOLD is detected low, the CPU drives HLDA low. **NOTE:** *Do not connect HLDA to V_{CC}—it will cause a deadlock.* A user wanting to give the 82596 permanent access to the bus should connect HLDA to HOLD. If HLDA goes inactive before HOLD, the 82596 will release the bus (by deasserting HOLD) within a maximum of within a specified number of bus cycles as specified in the 82596 User's Manual.
BREQ	115	I	**BUS REQUEST.** This signal, when configured to an externally activated mode, is used to trigger the bus throttle timers.
$\overline{PORT}$	3	I	**PORT.** When this signal is received, the 82596 latches the data on the data bus into an internal 32-bit register. When the CPU is asserting this signal it can write into the 82596 (via the data bus). This pin must be activated twice during all CPU Port access commands.
RESET	69	I	**RESET.** This active high, internally synchronized signal causes the 82596 to terminate current activity. The signal must be high for at least five system clock cycles. After five system clock cycles and four $\overline{TxC}$ clock cycles the 82596 will execute a Reset when it receives a high RESET signal. When RESET returns to low the 82596 waits for the first CA signal and then begins the initialization sequence.
LE/$\overline{BE}$	65	I	**LITTLE ENDIAN/BIG ENDIAN.** This dual-function pin is used to select byte ordering. When LE/$\overline{BE}$ is high, little endian byte ordering is used; when low, big endian byte ordering is used for data in frames (bytes) and for control (SCB, RFD, CBL, etc).
CA	119	I	**CHANNEL ATTENTION.** The CPU uses this pin to force the 82596 to begin executing memory resident Command blocks. The CA signal is internally synchronized. The signal must be high for at least one system clock. It is latched internally on the high to low edge and then detected by the 82596. The first CA after a Reset forces the 82596 into the initialization sequence beginning at location 00FFFFF6h or an SCP address written to the 82596 using CPU Port access. All subsequent CA signals cause the 82596 to begin executing new command sequences from the SCB.
INT/$\overline{INT}$	125	O	**INTERRUPT.** A high signal on this pin notifies the CPU that the 82596 is requesting an interrupt. This signal is an edge triggered interrupt signal, and can be configured to be active high or low.

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
V_{CC}	17 Pins		**POWER.** +5 V ±10%.
V_{SS}	17 Pins		**GROUND.** 0 V.
TxD	54	O	**TRANSMIT DATA.** This pin transmits data to the serial link. It is high when not transmitting.
$\overline{TxC}$	64	I	**TRANSMIT CLOCK.** This signal provides the fundamental timing for the serial subsystem. The clock is also used to transmit data synchronously on the TxD pin. For NRZ encoding, data is transferred to the TxD pin on the high to low clock transition. For Manchester encoding, the transmitted bit center is aligned with the low to high transition. Transmit clock must always be running for proper device operation.
$\overline{LPBK}$	58	O	**LOOPBACK.** This TTL-level control signal enables the loopback mode. In this mode serial data on the TxD input is routed through the 82C501 internal circuits and back to the RxD output without driving the transceiver cable. To enable this signal, both internal and external loopback need to be set with the Configure command.
RxD	60	I	**RECEIVE DATA.** This pin receives NRZ serial data only. It must be high when not receiving.
$\overline{RxC}$	59	I	**RECEIVE CLOCK.** This signal provides timing information to the internal shifting logic. For NRZ data the state of the RxD pin is sampled on the high to low transition of the clock.
$\overline{RTS}$	57	O	**REQUEST TO SEND.** When this signal is low the 82596 informs the external interface that it has data to transmit. It is forced high after a Reset or when transmission is stopped.
$\overline{CTS}$	62	I	**CLEAR TO SEND.** An active-low signal that enables the 82596 to send data. It is normally used as an interface handshake to $\overline{RTS}$. Asserting $\overline{CTS}$ high stops transmission. $\overline{CTS}$ is internally synchronized. If $\overline{CTS}$ goes inactive, meeting the setup time to the $\overline{TxC}$ negative edge, the transmission will stop and $\overline{RTS}$ will go inactive within, at most, two $\overline{TxC}$ cycles.
$\overline{CRS}$	63	I	**CARRIER SENSE.** This signal is active low, it is used to notify the 82596 that traffic is on the serial link. It is only used if the 82596 is configured for external Carrier Sense. In this configuration external circuitry is required for detecting traffic on the serial link. $\overline{CRS}$ is internally synchronized. To be accepted, the signal must remain active for at least two serial clock cycles (for CRSF = 0).
$\overline{CDT}$	61	I	**COLLISION DETECT.** This active-low signal informs the 82596 that a collision has occurred. It is only used if the 82596 is configured for external Collision Detect. External circuitry is required for collision detection. $\overline{CDT}$ is internally synchronized. To be accepted, the signal must remain active for at least two serial clock cycles (for CDTF = 0).

82596 AND HOST CPU INTERACTION

The 82596CA and the host CPU communicate through shared memory. Because of its on-chip DMA capability, the 82596 can make data block transfers (buffers and frames) independently of the CPU; this greatly reduces the CPU byte transfer overhead.

The 82596 is a multitasking coprocessor that comprises two independent logical units—the Command Unit (CU) and the Receive Unit (RU). The CU executes commands from shared memory. The RU handles all activities related to frame reception. The independence of the CU and RU enables the 82596 to engage in both activities simultaneously—the CU can fetch and execute commands from memory while the RU is storing received frames in memory. The CPU is only involved with this process after the CU has executed a sequence of commands or the RU has finished storing a sequence of frames.

The CPU and the 82596 use the hardware signals Interrupt (INT) and Channel Attention (CA) to initiate communication with the System Control Block (SCB), see Figure 4. The 82596 uses INT to alert the CPU of a change in the contents of the SCB, the CPU uses CA to alert the 82596.

The 82596 has a CPU Port Access state that allows the CPU to execute certain functions without accessing memory. The 82596 $\overline{\text{PORT}}$ pin and data bus pins are used to enable this feature. The CPU can directly activate four operations when the 82596 is in this state.

- Write an alternative System Configuration Pointer (SCP). This can be used when the 82596 cannot use the default SCP address space.
- Write a different Dump Command Pointer and execute Dump. This can be used for troubleshooting No Response problems.
- The CPU can reset the 82596 via software without disturbing the rest of the system.
- A self-test can be used for board testing; the 82596 will execute a self-test and write the results to memory.

82596 BUS INTERFACE

The 82596CA has bus interface timings and pin definitions that are compatible with Intel's 32-bit i486™SX and i486™DX microprocessors. This eliminates the need for additional bus interface logic. Operating at 33 MHz, the 82596's bus bandwidth can be as high as 106 MB/s. Since Ethernet only requires 1.25 MB/s, this leaves a considerable amount of bandwidth for the CPU. The 82596 also has a bus throttle to regulate its use of the bus. Two timers can be programmed through the SCB: one controls the maximum time the 82596 can remain on the bus, the other controls the time the 82596 must stay off the bus (see Figure 5). The bus throttle can be programmed to trigger internally with HLDA or externally with BREQ. These timers can restrict the 82596 HOLD activation time and improve bus utilization.

82596 MEMORY ADDRESSING

The 82596 has a 32-bit memory address range, which allows addressing up to four gigabytes of memory. The 82596 has three memory addressing modes (see Table 1).

- **82586 Mode.** The 82596 has a 24-bit memory address range. The System Control Block, Command List, Receive Descriptor List, and Buffer Descriptors must reside in one 64-KB memory segment. Transmit and Receive buffers can reside in a 24-bit address space.
- **32-Bit Segmented Mode.** The 82596 has a 32-bit memory address range. The System Control Block, Command List, Receive Descriptor List, and Buffer Descriptors must reside in one 64-KB memory segment. Transmit and Receive buffers can reside in a 32-bit address space.
- **Linear Mode.** The 82596 has a 32-bit memory address range. Any memory structure can reside anywhere within the 32-bit memory address range.

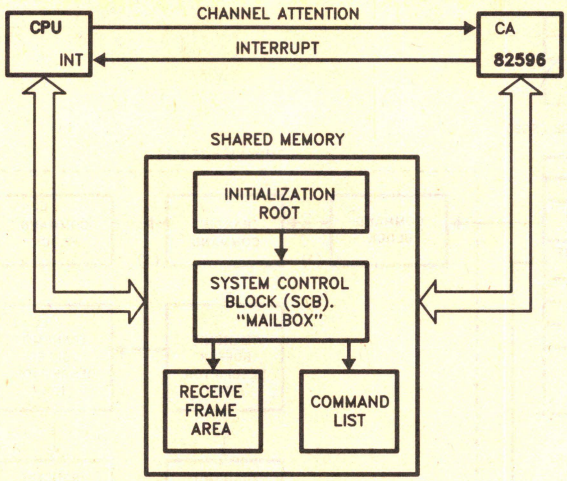


Figure 4. 82596 and Host CPU Intervention

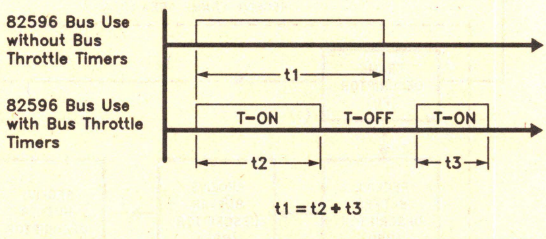


Figure 5. Bus Throttle Timers

Table 1. 82596 Memory Addressing Formats

Pointer or Offset	Operation Mode		
	82586	32-Bit Segmented	Linear
ISCP Address	24-Bit Linear	32-Bit Linear	32-Bit Linear
SCB Address	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Command Block Pointers	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Frame Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Tx Frame Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Buffer Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Tx Buffer Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Buffers	24-Bit Linear	32-Bit Linear	32-Bit Linear
Tx Buffers	24-Bit Linear	32-Bit Linear	32-Bit Linear

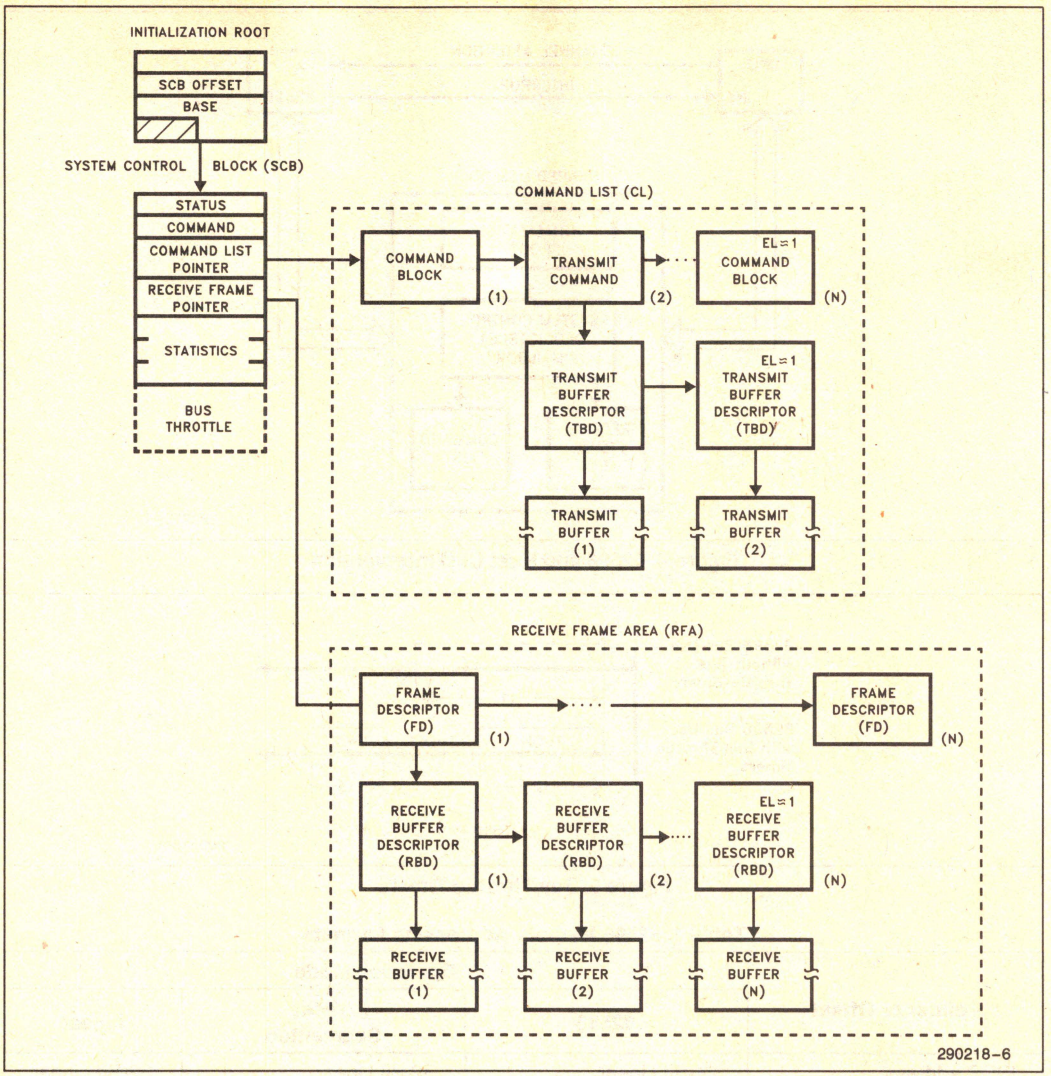


Figure 6. 82596 Shared Memory Structure

82596 SYSTEM MEMORY STRUCTURE

The Shared Memory structure consists of four parts: the Initialization Root, the System Control Block, the Command List, and the Receive Frame Area (see Figure 6).

The Initialization Root is in an established location known to the host CPU and the 82596 (00FFFFF6h). However, the CPU can establish the Initialization Root in another location by using the CPU Port access. This root is accessed during initialization, and points to the System Control Block.

The System Control Block serves as a bidirectional mail drop for the host CPU and the 82596 CU and RU. It is the central point through which the CPU and the 82596 exchange control and status information. The SCB has two areas. The first contains instructions from the CPU to the 82596. These include: control of the CU and RU (Start, Abort, Suspend, and Resume), a pointer to the list of CU commands, a pointer to the Receive Frame Area, a set of Interrupt Acknowledge bits, and the T-ON and T-OFF timers for the bus throttle. The second area contains status information the 82596 is sending to the CPU. Such as, the CU and RU states (Idle, Active

Ready, Suspended, No Receive Resources, etc.), interrupt bits (Command Completed, Frame Received, CU Not Ready, and RU Not Ready), and statistical counters.

The Command List functions as a program for the CU; individual commands are placed in memory units called Command Blocks (CBs). These CBs contain the parameters and status of specific high-level commands called Action Commands; e.g., Transmit or Configure.

Transmit causes the 82596 to transmit a frame. The Transmit CB contains the destination address, the length field, and a pointer to a list of linked buffers holding the frame that is to be constructed from several buffers scattered throughout memory. The Command Unit operates without CPU intervention; the DMA for each buffer, and the prefetching of references to new buffers, is performed in parallel. The CPU is notified only after a transmission is complete.

The Receive Frame Area is a list of Free Frame Descriptors (descriptors not yet used) and a list of user-prepared buffers. Frames arrive at the 82596 unsolicited; the 82596 must always be ready to receive and store them in the Free Frame Area. The Receive Unit fills the buffers when it receives frames, and reformats the Free Buffer List into received-frame structures. The frame structure is, for all practical purposes, identical to the format of the frame to be transmitted. The first Frame descriptor is referenced by the SCB. Unless the 82596 is configured to Save Bad Frames, the frame descriptor, and the associated buffer descriptor, which is wasted when a bad frame is received, are automatically reclaimed and returned to the Free Buffer List.

Receive buffer chaining (storing incoming frames in a linked buffer list) significantly improves memory utilization. Without buffer chaining, the user must allocate consecutive blocks of memory, each capable of containing a maximum frame (for Ethernet, 1518 bytes). Since an average frame is about 200 bytes, this is very inefficient. With buffer chaining, the user can allocate small buffers and the 82596 will only use those that are needed.

Figure 7 A–D illustrates how the 82596 uses the Receive Frame Area. Figure 7A shows an unused Receive Frame Area composed of Free Frame Descriptors and Free Receive Buffers prepared by the user. The SCB points to the first Frame Descriptor of the Frame Descriptor List. Figure 7B shows the same Receive Frame Area after receiving one frame. This first frame occupies two Receive Buffers and one Frame Descriptor—a valid received frame will only occupy one Frame Descriptor. After receiving this frame the 82596 sets the next Free Frame Descriptor RBD pointer to the next Free RBD. Figure 7C shows the RFA after receiving a second frame. In this example the second frame occupies only one Receive Buffer and one RFD. The 82596 again sets the RBD pointer. This process is repeated again in Figure 7D, showing the reception of another frame using one Receive Buffer; in this example there is an extra Frame Descriptor.

TRANSMIT AND RECEIVE MEMORY STRUCTURES

There are three memory structures for reception and transmission. The 82586 memory structure, the Flexible memory structure, and the Simplified memory structure. The 82586 mode is selected by configuring the 82596 during initialization. In this mode all the 82596 memory structures are compatible with the 82586 memory structures.

When the 82596 is not configured to the 82586 mode, the other two memory structures, Simplified and Flexible, are available for transmitting and receiving. These structures are selected by setting the S/F bit in the Transmit Command and/or the Receive Frame Descriptor (see Figures 29, 30, 41, and 42). It is recommended that any linked list of buffers be relegated to a single type—either simplified or flexible. The Simplified memory structure offers a simple structure for ease of programming (see Figure 8). All information about a frame is contained in one structure; for example, during reception the RFD and data field are contained in one structure.

The Flexible memory structure (see Figure 9) has a control field that allows the programmer to specify the amount of receive data the RFD will contain for receive operations and the amount of transmit data the Transmit Command Block will contain for transmit operations. For example, when the control field in the RFD is set to 20 bytes during a reception, the first 20 bytes of the data field are stored in the RFD (6 bytes of destination address, 6 bytes of source address, 2 bytes of length field, and 6 bytes of data) and the remainder of the data field is stored in the Receive Data Buffers. This is useful for capturing frame headers when header information is contained in the data field. The header information can then be automatically stored in the RFD partitioned from the Receive Data Buffer.

The control field can also be used for the Transmit Command when the Flexible memory structure is used. The quantity of data field bytes to be transmitted from the Transmit Command Block is specified by the variable control field.

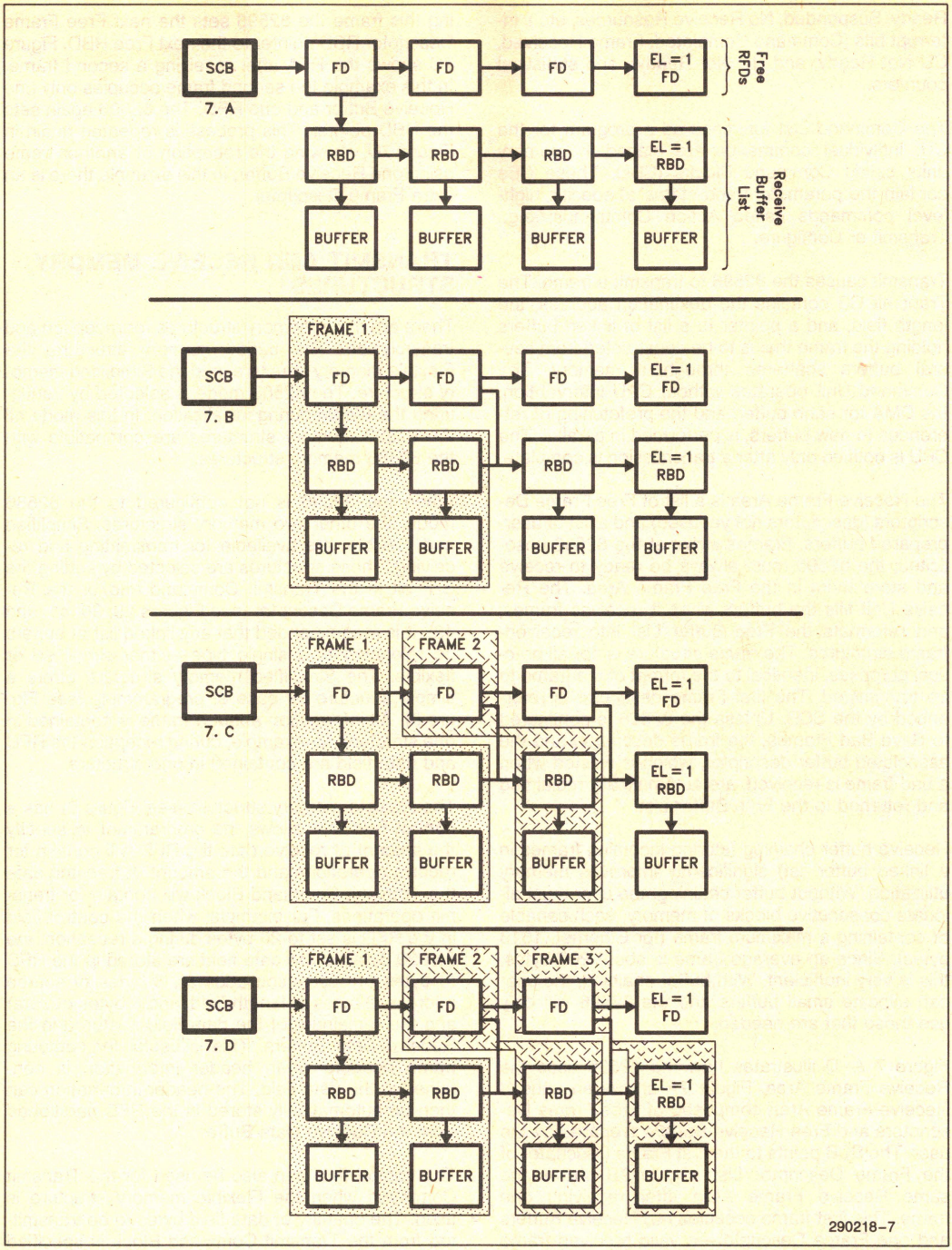


Figure 7. Frame Reception in the RFA

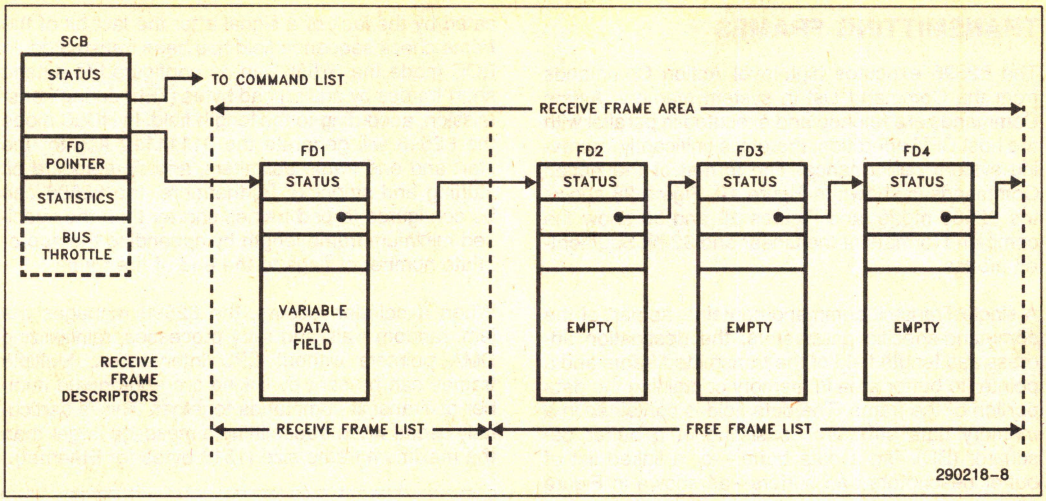


Figure 8. Simplified Memory Structure

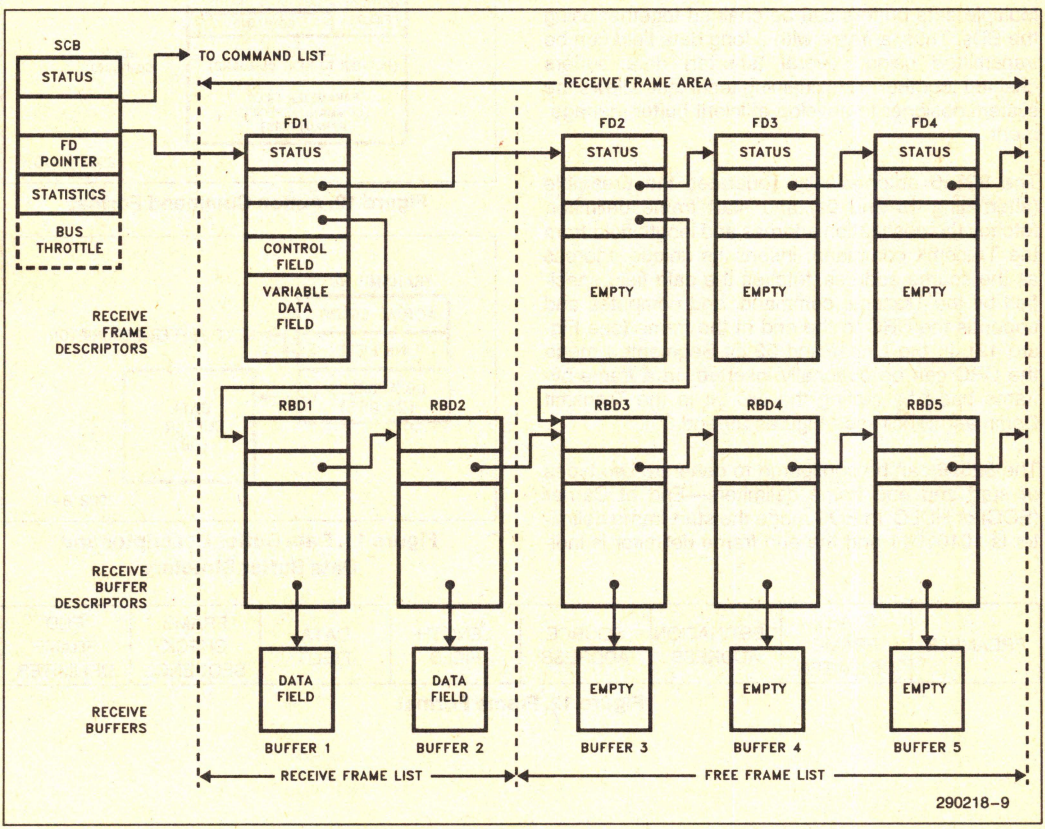


Figure 9. Flexible Memory Structure

TRANSMITTING FRAMES

The 82596 executes high-level Action Commands from the Command List in system memory. Action Commands are fetched and executed in parallel with the host CPU operation, thereby significantly improving system performance. The format of the Action Commands is shown in Figure 10. Figure 28 shows the 82586 mode, and Figures 29 and 30 show the command formats of the Linear and 32-bit Segmented modes.

A single Transmit command contains, as part of the command-specific parameters, the destination address and length field of the transmitted frame and a pointer to buffer area in memory containing the data portion of the frame. The data field is contained in a memory data structure consisting of a buffer descriptor (BD) and a data buffer—or a linked list of buffer descriptors and buffers—as shown in Figure 11.

Multiple data buffers can be chained together using the BDs. Thus, a frame with a long data field can be transmitted using several (shorter) data buffers chained together. This chaining technique allows the system designer to develop efficient buffer management.

The 82596 automatically generates the preamble (alternating 1s and 0s) and start frame delimiter, fetches the destination address and length field from the Transmit command, inserts its unique address as the source address, fetches the data field specified by the Transmit command, and computes and appends the CRC to the end of the frame (see Figure 12). In the Linear and 32-bit Segmented mode the CRC can be optionally inserted on a frame-by-frame basis by setting the NC bit in the Transmit Command Block (see Figures 29 and 30).

The 82596 can be configured to generate two types of start and end frame delimiters—End of Carrier (EOC) or HDLC. In EOC mode the start frame delimiter is 10101011 and the end frame delimiter is indicated by the lack of a signal after the last bit of the frame check sequence field has been transmitted. In EOC mode the 82596 can be configured to extend short frames by adding pad bytes (7Eh) during transmission, according to the length field. In HDLC mode the 82596 will generate the 01111110 flag for the start and end frame delimiters, and do standard bit stuffing and stripping. Furthermore, the 82596 can be configured to pad frames shorter than the specified minimum frame length by appending the appropriate number of flags to the end of the frame.

When a collision occurs, the 82596 manages the jam, random wait, and retry processes, reinitializing DMA pointers without CPU intervention. Multiple frames can be sent by linking the appropriate number of Transmit commands together. This is particularly useful when transmitting a message larger than the maximum frame size (1518 bytes for Ethernet).

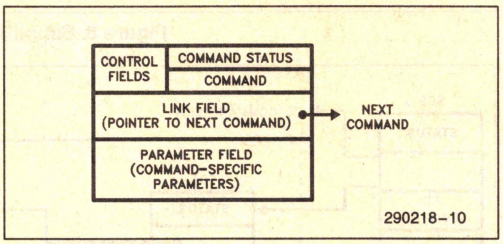


Figure 10. Action Command Format

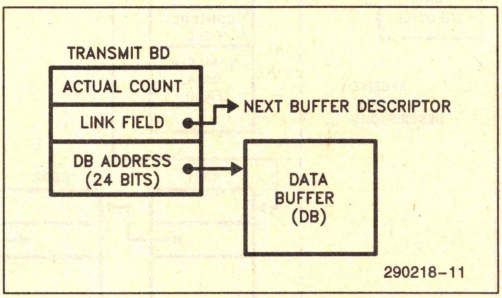


Figure 11. Data Buffer Descriptor and Data Buffer Structure

PREAMBLE	START FRAME DELIMITER	DESTINATION ADDRESS	SOURCE ADDRESS	LENGTH FIELD	DATA FIELD	FRAME CHECK SEQUENCE	END FRAME DELIMITER

Figure 12. Frame Format

RECEIVING FRAMES

To reduce CPU overhead, the 82596 is designed to receive frames without CPU supervision. The host CPU first sets aside an adequate receive buffer space and then enables the 82596 Receive Unit. Once enabled, the RU watches for arriving frames and automatically stores them in the Receive Frame Area (RFA). The RFA contains Receive Frame Descriptors, Receive Buffer Descriptors, and Data Buffers (see Figure 13). The individual Receive Frame Descriptors make up a Receive Descriptor List (RDL) used by the 82596 to store the destination and source addresses, the length field, and the status of each frame received (see Figure 14).

Once enabled, the 82596 checks each passing frame for an address match. The 82596 will recognize its own unique address, one or more multicast addresses, or the broadcast address. If a match is found the 82596 stores the destination and source addresses and the length field in the next available RFD. It then begins filling the next available Data Buffer on the FBL, which is pointed to by the current RFD, with the data portion of the incoming frame. As one Data Buffer is filled, the 82596 automatically fetches the next DB on the FBL until the entire frame is received. This buffer chaining technique is particularly memory efficient because it allows the system designer to set aside buffers to fit frames much shorter than the maximum allowable frame length. If AL-LOC = 1, or if the flexible memory structure is used, the addresses and length field can be placed in the Receive Buffer.

Once the entire frame is received without error, the 82596 does the following housekeeping tasks.

- The actual count field of the last Buffer Descriptor used to hold the frame just received is updated with the number of bytes stored in the associated Data Buffer.
- The next available Receive Frame Descriptor is fetched.
- The address of the next available Buffer Descriptor is written to the next available Receive Frame Descriptor.
- A frame received interrupt status bit is posted in the SCB.
- An interrupt is sent to the CPU.

If a frame error occurs, for example a CRC error, the 82596 automatically reinitializes its DMA pointers and reclaims any data buffers containing the bad frame. The 82596 will continue to receive frames without CPU help as long as Receive Frame Descriptors and Data Buffers are available.

82596 NETWORK MANAGEMENT AND DIAGNOSTICS

The behavior of data communication networks is normally very complex because of their distributed and asynchronous nature. It is particularly difficult to pinpoint a failure when it occurs. The 82596 has extensive diagnostic and network management functions that help improve reliability and testability. The 82596 reports on the following events after each frame is transmitted.

- Transmission successful.
- Transmission unsuccessful. Lost Carrier Sense.
- Transmission unsuccessful. Lost Clear to Send.
- Transmission unsuccessful. A DMA underrun occurred because the system bus did not keep up with the transmission.
- Transmission unsuccessful. The number of collisions exceeded the maximum allowed.
- Number of Collisions. The number of collisions experienced during transmission of the frame.
- Heartbeat Indicator. This indicates the presence of a heartbeat during the last Interframe Spacing (IFS) after transmission.

When configured to Save Bad Frames the 82596 checks each incoming frame and reports the following errors.

- CRC error. Incorrect CRC in a properly aligned frame.
- Alignment error. Incorrect CRC in a misaligned frame.
- Frame too short. The frame is shorter than the value configured for minimum frame length.
- Overrun. Part of the frame was not placed in memory because the system bus did not keep up with incoming data.
- Out of buffer. Part of the frame was discarded because of insufficient memory storage space.
- Receive collision. A collision was detected during reception and the destination address of the incoming frame matches the 82596 individual address. Collisions in the preamble are not counted.
- Length error. A frame not matching the frame length parameter was detected.

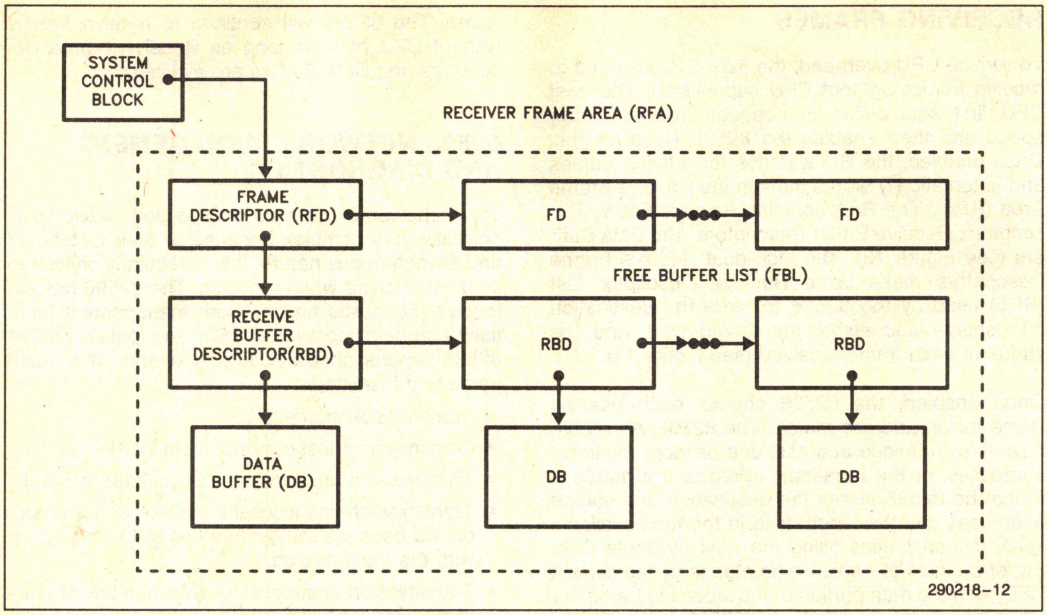


Figure 13. Receive Frame Area Diagram

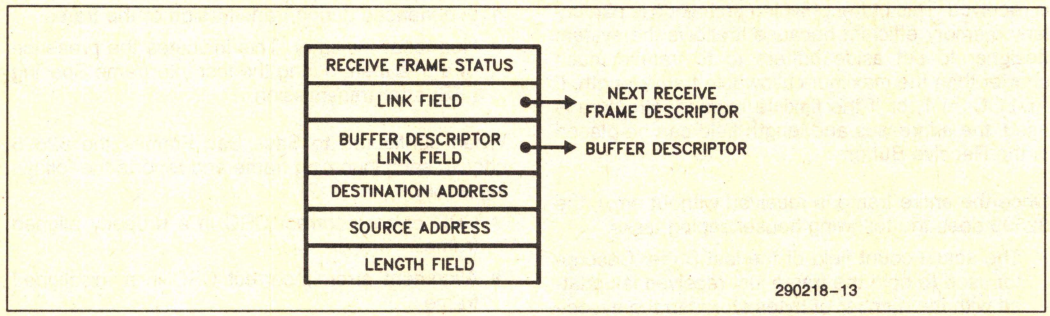


Figure 14. Receive Frame Descriptor

NETWORK PLANNING AND MAINTENANCE

To properly plan, operate, and maintain a communication network, the network management entity must accumulate information on network behavior. The 82596 provides a rich set of network-wide diagnostics that can serve as the basis for a network management entity.

Information on network activity is provided in the status of each frame transmitted. The 82596 reports the following activity indicators after each frame.

- Number of collisions. The number of collisions the 82596 experienced while attempting to transmit the frame.
- Deferred transmission. During the first transmission attempt the 82596 had to defer to traffic on the link.

The 82596 updates its 32-bit statistical counters after each received frame that both passes address filtering and is longer than the Minimum Frame Length configuration parameter. The 82596 reports the following statistics.

- CRC errors. The number of well-aligned frames that experienced a CRC error.
- Alignment errors. The number of misaligned frames that experienced a CRC error.
- No resources. The number of frames that were discarded because of insufficient resources for reception.
- Overrun errors. The number of frames that were not completely stored in memory because the system bus did not keep up with incoming data.
- Receive Collision counter. The number of collisions detected during receive. Collisions occurring before the minimum frame length will be counted as short frames. Collisions in the preamble will not be counted at all.
- Short Frame counter. The number of frames that were discarded because they were shorter than the configured minimum frame length.

Once again, these counters are not updated until the 82596 decodes a destination address match.

The 82596 can be configured to Promiscuous mode. In this mode it captures all frames transmitted on the network without checking the Destination Address. This is useful when implementing a monitoring station to capture all frames for analysis.

A useful method of capturing frame headers is to use the Simplified memory mode, configure the 82596 to Save Bad Frames, and configure the 82596 to Promiscuous mode with space in the RFD allocated for specific number of receive data bytes. The 82596 will receive all frames and put them in the RFD. Frames that exceed the available space in the RFD will be truncated, the status will be updated, and the 82596 will retrieve the next RFD. This allows the user to capture the initial data bytes of each frame (for instance, the header) and discard the remainder of the frame.

The 82596 also has a monitor mode for network analysis. During normal operation the receive function enables the 82596 to receive frames that pass address filtering. These frames must have the Start of Frame Delimiter (SFD) field and must be longer than the absolute minimum frame length of 5 bytes (6 bytes in case of Multicast address filtering). Contents and status of the received frames are transferred to memory. The monitor function enables the 82596 to simply evaluate the incoming frames. The 82596 can monitor the frames that pass or do not pass the address filtering. It can also monitor frames which do not have the SFD fields. The 82596 can be configured to only keep statistical information about monitor frames. Three options are available in the Monitor mode. These options are selected by the two monitor mode configuration bits available in the configuration command.

When the first option is selected, the 82596 receives good frames that pass address filtering and transfers them to memory while monitoring frames that do not pass address filtering or are shorter than the minimum frame size (these frames are not transferred to memory). When this option is used the 82596 updates six counters: CRC errors, alignment errors, no resource errors, overrun errors, short frames and total good frames received.

When the second option is selected, the receive function is completely disabled. The 82596 monitors only those frames that pass address filterings and meet the minimum frame length requirement. When this option is used the 82596 updates six counters: CRC errors, alignment errors, total frames (good and bad), short frames, collisions detected and total good frames.

When the third option is selected, the receive function is completely disabled. The 82596 monitors all frames, including frames that do not have a Start Frame Delimiter. When this option is used the 82596 updates six counters: CRC errors, alignment errors, total frames (good and bad), short frames, collisions detected and total good frames.

STATION DIAGNOSTICS AND SELF-TEST

The 82596 provides a large set of diagnostic and network management functions. These include internal and external loopback and time domain reflectometry for locating fault points in the network cable. The 82596 ensures software reliability by dumping the contents of the 82596 internal registers into system memory. The 82596 has a self-test mode that enables it to run an internal self-test and place the results in system memory.

82586 SOFTWARE COMPATIBILITY

The 82596 has a software-compatible state in which all its memory structures are compatible with the 82586 memory structure. This includes all the Action Commands, the Receive Frame Area (including the RFD, Buffer Descriptors, and Data Buffers), the System Control Block, and the initialization procedures. There are two minor differences between the 82596 in the 82586-Compatible memory structure and the 82586.

- When the internal and external loopback bits in the Configure command are set to 11 the 82596 is in external loopback and the $\overline{\text{LPBK}}$ pin is activated; in the 82586 this situation would produce internal loopback.
- During a Dump command both the 82596 and 82586 dump the same number of bytes; however, the data format is different.

INITIALIZING THE 82596

A Reset command is issued to the 82596 to prepare it for normal operation. The 82596 is initialized through two data structures that are addressed by two pointers, the System Configuration Pointer (SCP) and the Intermediate System Configuration Pointer (ISCP). The initialization procedure begins when a Channel Attention signal is asserted after RESET. The 82596 uses the address of the double word that contains the SCP as a default—00FFFFF4h. Before the CA signal is asserted this default address can be changed to any other available address by asserting the $\overline{\text{PORT}}$ pin and providing the desired address over the $D_{31}-D_4$ pins of the address bus. Pins D_3-D_0 must be 0010; i.e., any alternative address must be aligned to 16-byte boundaries. All addresses sent to the 82596 must be word aligned, which means that all pointers and memory structures must start on an even address (A_0 = zero).

SYSTEM CONFIGURATION POINTER (SCP)

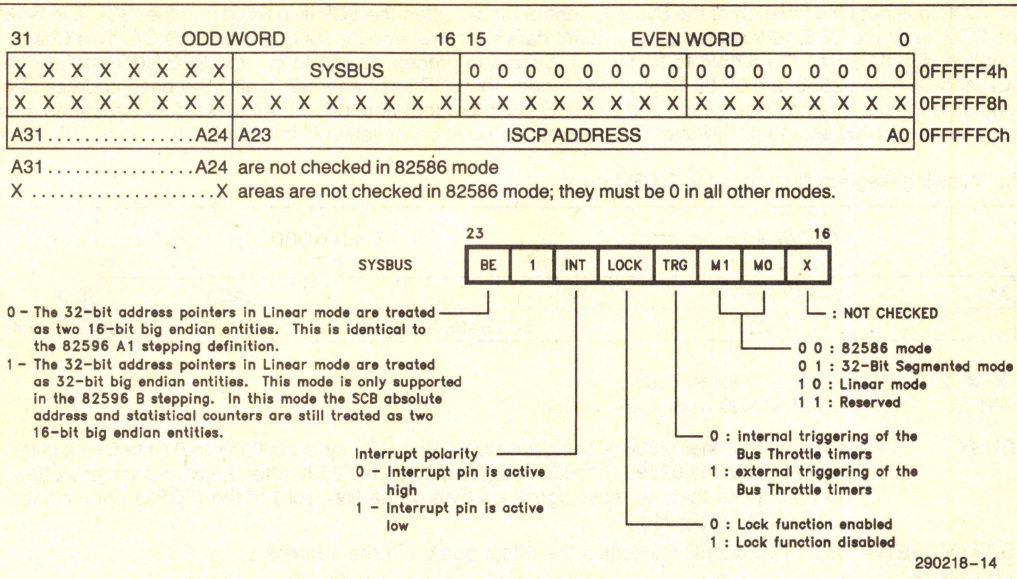
The SCP contains the sysbus byte and the location of the next structure of the initialization process, the ISCP. The following parameters are selected in the SYSBUS.

- The 82596 operation mode.
- The Bus Throttle timer triggering method.
- Lock enabled.
- Interrupt polarity.
- Big Endian 32-bit entity mode.

Byte ordering is determined by the LE/$\overline{\text{BE}}$ pin. LE/$\overline{\text{BE}}$ = 1 selects Little Endian byte ordering and LE/$\overline{\text{BE}}$ = 0 selects Big Endian byte ordering.

NOTE:
In the following, X indicates a bit not checked 82586 mode. This bit must be set to 0 in all other modes.

The following diagram illustrates the format of the SCP.



ISCP ADDRESS— The physical address of the ISCP. In the 82586 mode, bits A31–A24 are considered to be zero.

Figure 15. The System Configuration Pointer

Writing the Sysbus

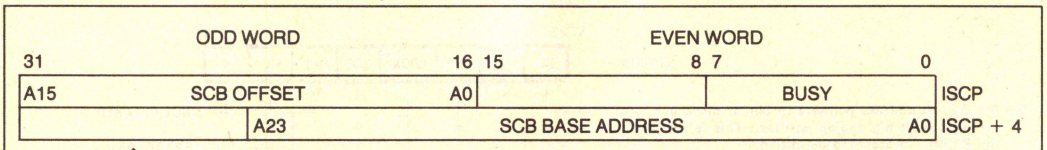
When writing the sysbus byte it is important to pay attention to the byte order.

- When a Little Endian processor is used, the sysbus byte is located at byte address 00FFFFF6h (or address $n+2$ if an alternative SCP address n was programmed).
- When a processor using Big Endian byte ordering is used, the sysbus, alternative SCP, and ISCP addresses will be different.
  - The sysbus byte is located at 00FFFFF5h.
  - If an alternative SCP address is programmed, the sysbus byte should be at byte address $n+1$.

INTERMEDIATE SYSTEM CONFIGURATION POINTER (ISCP)

The ISCP indicates the location of the System Control Block. Often the SCP is in ROM and the ISCP is in RAM. The CPU loads the SCB address (or an equivalent data structure) into the ISCP and asserts CA. This Channel Attention signal causes the 82596 to begin its initialization procedure and to get the SCB address from the ISCP and SCP. In 82586 and 32-bit Segmented modes the SCP base address is also the base address of all Command Blocks, Frame Descriptors, and Buffer Descriptors (but not buffers). All these data structures must reside in one 64-KB segment; however, in Linear mode no such limitation is imposed.

The following diagram illustrates the ISCP format.

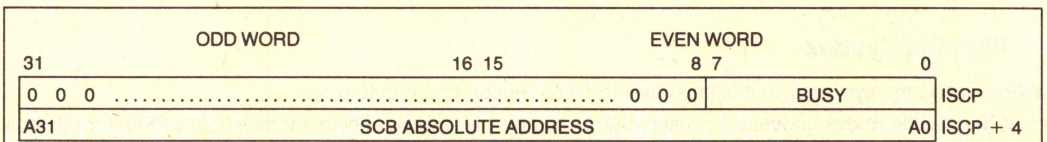


BUSY — Indicates that the 82596 is being initialized. The CPU sets the ISCP to 01h before it gives the first CA to the 82596. The ISCP is cleared by the 82596 after the SCB base and offset are read. Note that the most significant byte of the first word of the ISCP is not modified when BUSY is cleared.

SCB OFFSET— This 16-bit quantity specifies the offset portion of the address of the SCB.

SCB BASE — Specifies the base portion of the address of the SCB. The base of SCB is also the base of all 82596 Command Blocks, Frame Descriptors and Buffer Descriptors. In the 82586 mode, bits A31–A24 are considered to be zero.

Figure 16. The Intermediate System Configuration Pointer—82586 and 32-Bit Segmented Modes



BUSY — Indicates that the 82596 is being initialized. The ISCP is set to 01h by the CPU before its first CA to the 82596. It is cleared by the 82596 after the SCB address is read.

SCB ADDRESS— This 32-bit quantity specifies the physical address of the SCB.

Figure 17. The Intermediate System Configuration Pointer—Linear Mode.

INITIALIZATION PROCESS

The CPU sets up the SCP, ISCP, and the SCB structures, and, if desired, an alternative SCP address. It also sets BUSY to 01h. The 82596 is initialized when a Channel Attention signal follows a Reset signal, causing the 82596 to access the System Configuration Pointer. The sysbus byte, the operational mode, the bus throttle timer triggering method, the interrupt polarity, and the state of $\overline{LOCK}$ are read. After reset the Bus Throttle timers are essentially disabled—the T-ON value is infinite, the T-OFF value is zero. After the SCP is read, the 82596 reads the ISCP and saves the SCB address. In 82586 and 32-bit Segmented modes this address is represented as a base address plus the offset (this base address is also the base address of all the control blocks). In Linear mode the base address is also an absolute address. The 82596 clears BUSY, sets CX and CNR to equal 1 in the SCB, clears the SCB command word, sends an interrupt to the CPU, and awaits another Channel Attention signal. RESET configures the 82596 to its default state before CA is asserted.

CONTROLLING THE 82596CA

The host CPU controls the 82596 with the commands, data structures, and methods described in this section. The CPU and the 82596 communicate through shared memory structures. The 82596 contains two independent units: the Command Unit and the Receive Unit. The Command Unit executes commands from the CPU, and the Receive Unit handles frame reception. These two units are controlled and monitored by the CPU through a shared memory structure called the System Control Block (SCB). The CPU and the 82596 use the CA and INT signals to communicate with the SCB.

82596 CPU ACCESS INTERFACE ($\overline{PORT}$)

The 82596 has a CPU access interface that allows the host CPU to do four things.

- Write an alternative System Configuration Pointer address.
- Write an alternative Dump area pointer and perform Dump.
- Execute a software reset.
- Execute a self-test.

The following events initiate the CPU access state.

- Presence of an address on the $D_{31}-D_4$ data bus pins.
- The D_3-D_0 pins are used to select one of the four functions.
- The $\overline{PORT}$ input pin is asserted, as in a regular write cycle.

NOTE.
The SCP Dump and Self-Test addresses must be 16-byte aligned.

The 82596 requires two 16-bit write cycles for a port command. The first write holds the internal machines and reads the first 16 bits; the second activates the $\overline{PORT}$ command and reads the second 16 bits.

The $\overline{PORT}$ Reset is useful when only the 82596 needs to be reset. The CPU must wait for 10-system and 5-serial clocks before issuing another CA to the 82596; this new CA begins a new initialization process.

The Dump function is useful for troubleshooting No Response problems. If the chip is in a No Response state, the $\overline{PORT}$ Dump operation can be executed and a $\overline{PORT}$ Reset can be used to reinitialize the 82596 without disturbing the rest of the system.

The Self-Test function can be used for board testing; the 82596 will execute a self-test and write the results to memory.

Table 2. $\overline{PORT}$ Function Selection

	D31 ..... D4						D0
Function	**Addresses and Results**			**D3**	**D2**	**D1**	**D0**
Reset	A31	Don't Care	A4	0	0	0	0
Self-Test	A31	Self-Test Results Address	A4	0	0	0	1
SCP	A31	Alternative SCP Address	A4	0	0	1	0
Dump	A31	Dump Area Pointer	A4	0	0	1	1

MEMORY ADDRESSING FORMATS

The 82596 accesses memory by 32-bit addresses. There are two types of 32-bit addresses: linear and segmented. The type of address used depends on the 82596 operating mode and the type of memory structure it is addressing. The 82596 has three operating modes.

- 82586 Mode
  - A Linear address is a single 24-bit entity. Address pins $A_{31}-A_{24}$ are always zero.
  - A Segmented address uses a 24-bit base and a 16-bit offset.
- 32-bit Segmented Mode
  - A Linear address is a single 32-bit entity.
  - A Segmented address uses a 32-bit base and a 16-bit offset.

NOTE:
In the previous two memory addressing modes, each command header (CB, TBD, RFD, RBD, and SCB) must wholly reside within one segment. If the 82596 encounters a memory structure that does not follow this restriction, the 82596 will fetch the next contiguous location in memory (beyond the segment).

- Linear Mode
  - A Linear address is a single 32-bit entity.
  - There are no Segmented addresses.

Linear addresses are primarily used to address transmit and receive data buffers. In the 82586 and 32-bit Segmented modes, segmented addresses (base plus offset) are used for all Command Blocks, Buffer Descriptors, Frame Descriptors, and System Control Blocks. When using Segmented addresses, only the offset portion of the entity being addressed is specified in the block. The base for all offsets is the same—that of the SCB. See Table 1.

LITTLE ENDIAN AND BIG ENDIAN BYTE ORDERING

The 82596 supports both Little Endian and Big Endian byte ordering for its memory structures.

The 82596 A1 stepping supports Big Endian byte ordering for word and byte entities. Dword entities are not supported with 82596 A1 Big Endian byte ordering. This results in slightly different 82596A1 memory structures for Big Endian operation. These structures are defined in the *32-Bit LAN Components User's Manual.*

The 82596 B stepping supports Big Endian byte ordering for Linear mode only. All 82596 B 32-bit address pointers are treated as 32-bit Big Endian entities, however, the SCB absolute address and statistical counters are treated as two 16-bit Big Endian entities. This 32-bit Big Endian entity support is configured through bit 7 in the SYSBUS byte.

The 82596 C-step has a New Enhanced Big Endian Mode where in Linear Addressing mode, true 32-bit Big Endian functionality is achieved. New Enhanced Big Endian Mode is enabled exactly the same as the B-step, by setting bit 7 of the SYSBUS byte. This mode is software compatible with the big endian mode of the B-step with one exception—no 32-bit addresses need to be swapped by software in the C-step. In this new mode, the 82596 C-step treats 32-bit address pointers as true 32-bit entities and the SCB absolute address and statistical counters are still treated as two 16-bit big endian entities. Not setting this mode will configure the 82596 C-step to be 100% compatible to the A1-step big endian mode.

NOTE:
All 82596 memory entities must be word or dword aligned, except the transmit buffers can be byte aligned for the 82596 B or C-steppings.

An example of a dword entity is a frame descriptor command/status dword, whereas the raw data of the frame are byte entities. Both 32- and 16-bit buses are supported. When a 16-bit bus is used with Big Endian memory organization, data lines $D_{15}-D_0$ are used. The 82596 has an internal crossover that handles these swap operations.

COMMAND UNIT (CU)

The Command Unit is the logical unit that executes Action Commands from a list of commands very similar to a CPU program. A Command Block is associated with each Action Command. The CU is modeled as a logical machine that takes, at any given time, one of the following states.

- **Idle.** The CU is not executing a command and is not associated with a CB on the list. This is the initial state.
- **Suspended.** The CU is not executing a command; however, it is associated with a CB on the list.
- **Active.** The CU is executing an Action Command and pointing to its CB.

The CPU can affect CU operation in two ways: by issuing a CU Control Command or by setting bits in the Command word of the Action Command.

When programming the 82596 CU, it is important to consider the asynchronous way the 82596 processes commands. If a command is issued to the 82596 CU, it may be busy processing other commands. In order to avoid asynchronous race conditions, the following guidelines are recommended to the 82596 programmer:

- If the CU is already in the Active state, and another command needs to be executed, it is unwise to immediately issue another CU Start command. If a new command (or list of commands) needs to be started, first issue a CU Suspend command, wait for the CU to become Suspended, then issue the new CU Start. This will insure that all commands are processed correctly.
- In general, it is a good idea to make sure any CU command has been accepted and executed before issuing a new control command to the CU.

RECEIVE UNIT (RU)

The Receive Unit is the logical unit that receives frames and stores them in memory. The RU is modeled as a logical machine that takes, at any given time, one of the following states.

- **Idle.** The RU has no memory resources and is discarding incoming frames. This is the initial state.
- **No Resources.** The RU has no memory resources and is discarding incoming frames. This state differs from Idle in that the RU accumulates statistics on the number of discarded frames.
- **Suspended.** The RU has memory available for storing frames, but is discarding them. The suspend state can only be reached if the CPU forces this through the SCB or sets the suspend bit in the RFD.
- **Ready.** The RU has memory available and is storing incoming frames.

The CPU can affect RU operation in three ways: by issuing an RU Control Command, by setting bits in the Frame Descriptor Command word of the frame being received, or by setting the EL bit of the current buffer's Buffer Descriptor.

When programming the 82596 RU, it is important to consider the asynchronous way the 82596 processes receive frames. If an RU Start is issued to the 82596 RU, it may be busy processing other incoming packets. In order to avoid asynchronous race conditions, the following guidelines are recommended to the 82596 programmer:

- If the RU is already in the Ready state, and a new RFA is required to be started, it is unwise to immediately issue another RU Start command. If the new RFA needs to be started, first issue an RU Suspend command, wait for the RU to become Suspended, then issue the new RU Start. This will insure that all incoming frames are received correctly.
- In general, it is a good idea to make sure any RU command has been accepted and executed before issuing a new control command to the RU.

SYSTEM CONTROL BLOCK (SCB)

The SCB is a memory block that plays a major role in communications between the CPU and the 82596. Such communications include the following.

- Commands issued by the CPU
- Status reported by the 82596

Control commands are sent to the 82596 by writing them into the SCB and then asserting CA. The 82596 examines the command, performs the required action, and then clears the SCB command word. Control commands perform the following types of tasks.

- Operation of the Command Unit (CU). The SCB controls the CU by specifying the address of the Command Block List (CBL) and by starting, suspending, resuming, or aborting execution of CBL commands.
- Operation of the Bus Throttle. The SCB controls the Bus Throttle timers by providing them with new values and sending the Load and Start timer commands. The timers can be operated in both the 32-bit Segmented and Linear modes.
- Reception of frames by the Receive Unit (RU). The SCB controls the RU by specifying the address of the Receive Frame Area and by starting, suspending, resuming, or aborting frame reception.
- Acknowledgment of events that cause interrupts.
- Resetting the chip.

The 82596 sends status reports to the CPU via the System Control Block. The SCB contains four types of status reports.

- The cause of the current interrupts. These interrupts are caused by one or more of the following 82596 events.
  - The Command Unit completes an Action Command that has its I bit set.
  - The Receive Unit receives a frame.
  - The Command Unit becomes inactive.
  - The Receive Unit becomes not ready.
- The status of the Command Unit.
- The status of the Receive Unit.
- Status reports from the 82596 regarding reception of corrupted frames.

Events can be cleared only by CPU acknowledgment. If some events are not acknowledged by the ACK field the Interrupt signal (INT) will be reissued after Channel Attention (CA) is processed. Furthermore, if a new event occurs while an interrupt is set, the interrupt is temporarily cleared to trigger edge-triggered interrupt controllers.

The CPU uses the Channel Attention line to cause the 82596 to examine the SCB. This signal is trailing-edge triggered—the 82596 latches CA on the trailing edge. The latch is cleared by the 82596 before the SCB control command is read.

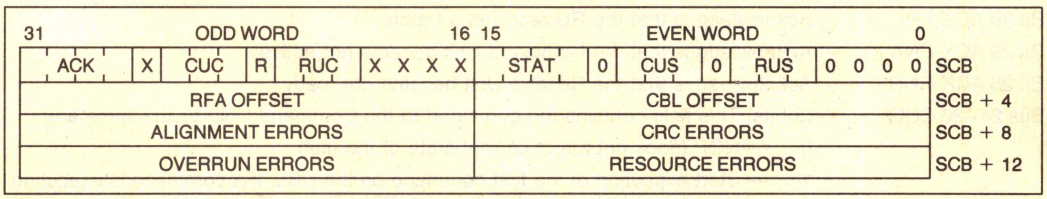
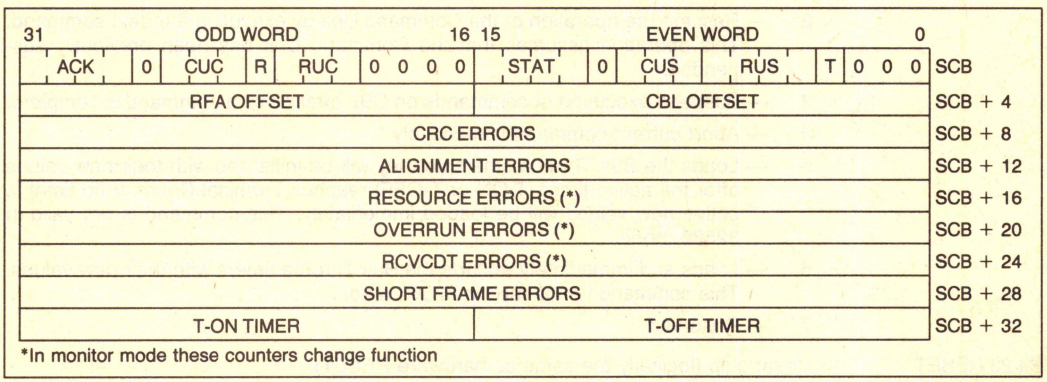
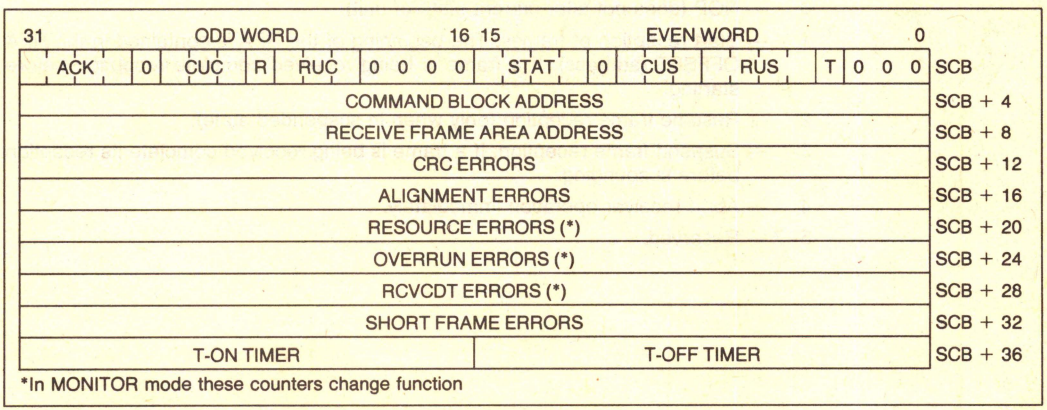


Figure 18. SCB—82586 Mode



*In monitor mode these counters change function

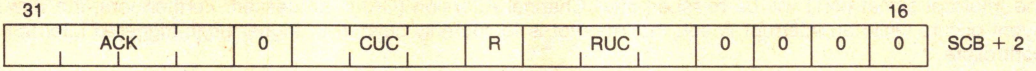
Figure 19. SCB—32-Bit Segmented Mode



*In MONITOR mode these counters change function

Figure 20. SCB—Linear Mode

Command Word



These bits specify the action to be performed as a result of a CA. This word is set by the CPU and cleared by the 82596. Defined bits are:

Bit 31 ACK-CX — Acknowledges that the CU completed an Action Command.

Bit 30 ACK-FR — Acknowledges that the RU received a frame.

Bit 29 ACK-CNA — Acknowledges that the Command Unit became not active.

Bit 28 ACK-RNR — Acknowledges that the Receive Unit became not ready.

Bits 24–26 CUC — (3 bits) This field contains the command to the Command Unit. Valid values are:

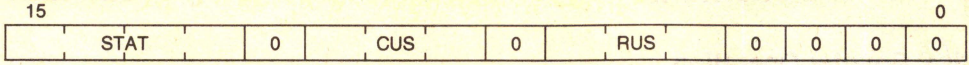
- 0 — NOP (does not affect current state of the unit).
- 1 — Start execution of the first command on the CBL. If a command is executing, complete it before starting the new CBL. The beginning of the CBL is in CBL OFFSET (address).
- 2 — Resume the operation of the Command Unit by executing the next command. This operation assumes that the Command Unit has been previously suspended.
- 3 — Suspend execution of commands on CBL after current command is complete.
- 4 — Abort current command immediately.
- 5 — Loads the Bus Throttle timers so they will be initialized with their new values after the active timer (T-ON or T-OFF) reaches Terminal Count. If no timer is active new values will be loaded immediately. This command is not valid in 82586 mode.
- 6 — Loads and immediately restarts the Bus Throttle timers with their new values. This command is not valid in 82586 mode.
- 7 — Reserved.

Bit 23 RESET — Reset chip (logically the same as hardware RESET).

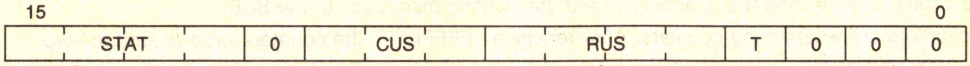
Bits 20–22 RUC — (3 bits) This field contains the command to the Receive Unit. Valid values are:

- 0 — NOP (does not alter current state of unit).
- 1 — Start reception of frames. The beginning of the RFA is contained in the RFA OFFSET (address). If a frame is being received complete reception before starting.
- 2 — Resume frame reception (only when in suspended state).
- 3 — Suspend frame reception. If a frame is being received complete its reception before suspending.
- 4 — Abort receiver operation immediately.
- 5–7 — Reserved.

Status Word



82586 mode



32-Bit Segmented and Linear mode.

Indicates the status of the 82596. This word is modified only by the 82596. Defined bits are:

Bit 15 CX — The CU finished executing a command with its I (interrupt) bit set.

Bit 14 FR — The RU finished receiving a frame.

Bit 13 CNA — The Command Unit left the Active state.

Bit 12 RNR — The Receive Unit left the Ready state.

Bits 8–10 CUS — (3 bits) This field contains the status of the command unit. Valid values are:

- 0 — Idle
- 1 — Suspended
- 2 — Active
- 3–7 — Not used

Bits 4–7 RUS — This field contains the status of the receive unit. Valid values are:

- 0h (0000) — Idle
- 1h (0001) — Suspended
- 2h (0010) — No Resources. This bit indicates both no resources due to lack of RFDs in the RDL and no resources due to lack of RBDs in the FBL.
- 4h (0100) — Ready
- Ah (1010) — No resources due to no more RBDs (not in the 82586 mode).
- Ch (1100) — No more RBDs (not in 82586 mode)
- No other combinations are allowed

Bit 3 T — Bus Throttle timers loaded (not in 82586 mode).

SCB OFFSET ADDRESSES

CBL Offset (Address)

In 82586 and 32-bit Segmented modes this 16-bit quantity indicates the offset portion of the address for the first Command Block on the CBL. In Linear mode it is a 32-bit linear address for the first Command Block on the CBL. It is accessed only if CUC equals Start.

RFA Offset (Address)

In 82586 and 32-bit Segmented modes this 16-bit quantity indicates the offset portion of the address for the Receive Frame Area. In Linear mode it is a 32-bit linear address for the Receive Frame Area. It is accessed only if RUC equals Start.

SCB STATISTICAL COUNTERS

Statistical Counter Operation

- The CPU is responsible for clearing all error counters before initializing the 82596. The 82596 updates these counters by reading them, adding 1, and then writing them back to the SCB.
- The counters are wraparound counters. After reaching FFFFFFFFh the counters wrap around to zero.
- The 82596 updates the required counters for each frame. It is possible for more than one counter to be updated; multiple errors will result in all affected counters being updated.
- The 82596 executes the read-counter/increment/write-counter operation without relinquishing the bus (locked operation). This is to ensure that no logical contention exists between the 82596 and the CPU due to both attempting to write to the counters simultaneously. In the dual-port memory configuration the CPU should not execute any write operation to a counter if $\overline{\text{LOCK}}$ is asserted.
- The counters are 32-bits wide and their behavior is fully compatible with the IEEE 802.3 standard. The 82596 supports all relevant statistics (mandatory, optional, and desired) through the status of the transmit and receive header and directly through SCB statistics.

CRCERRS

This 32-bit quantity contains the number of aligned frames discarded because of a CRC error. This counter is updated, if needed, regardless of the RU state.

ALNERRS

This 32-bit quantity contains the number of frames that both are misaligned (i.e., where $\overline{\text{CRS}}$ deasserts on a nonoctet boundary) and contain a CRC error. The counter is updated, if needed, regardless of the RU state.

SHRTFRM

This 32-bit quantity contains the number of received frames shorter than the minimum frame length.

The last three counters change function in monitor mode.

RSCERRS

This 32-bit quantity contains the number of good frames discarded because there were no resources to contain them. Frames intended for a host whose RU is in the No Receive Resources state, fall into this category. This counter is updated only if the RU is in the No Resources state. When in Monitor mode this counter counts the total number of frames—good and bad.

OVRNERRS

This 32-bit quantity contains the number of frames known to be lost because the local system bus was not available. If the traffic problem lasts longer than the duration of one frame, the frames that follow the first are lost without an indicator, and they are not counted. This counter is updated, if needed, regardless of the RU state.

This 32-bit counter contains the number of collisions detected during frame reception. This counter will only be updated if at least 64 bytes of data are received before the collision occurs. If a collision occurs before 64 bytes of data are received, the frame is counted as a short frame. If the collision occurs in the preamble, no counters are incremented.

ACTION COMMANDS AND OPERATING MODES

This section lists all the Action Commands of the Command Unit Command Block List (CBL). Each command contains the Command field, the Status and Control fields, the link to the next Action Command, and any command-specific parameters. There are three basic types of action commands: 82596 Configuration and Setup, Transmission, and Diagnostics. The following is a list of the actual commands.

- NOP
- Individual Address Setup
- Configure
- MC Setup
- Transmit
- TDR
- Dump
- Diagnose

The 82596 has three addressing modes. In the 82586 mode all the Action Commands look exactly like those of the 82586.

- **82586 Mode.** The 82596 software and memory structure is compatible with the 82586.
- **32-Bit Segmented Mode.** The 82596 can access the entire system memory and use the two new memory structures—Simplified and Flexible—while still using the segmented approach. This does not require any significant changes to existing software.
- **Linear Mode.** The 82596 operates in a flat, linear, 4 gigabyte memory space without segmentation. It can also use the two new memory structures.

In the 32-bit Segmented mode there are some differences between the 82596 and 82586 action commands, mainly in programming and activating new 82596 features. Those bits marked "don't care" in the compatible mode are not checked; however, we strongly recommend that those bits all be zeroes; this will allow future enchancements and extensions.

In the Linear mode all of the address offsets become 32-bit address pointers. All new 82596 features are accessible in this mode, and all bits previously marked "don't care" must be zeroes.

The Action Commands, and all other 82596 memory structures, must begin on even byte boundaries, i.e., they must be word aligned.

NOP

This command results in no action by the 82596 except for those performed in the normal command processing. It is used to manipulate the CBL manipulation. The format of the NOP command is shown in Figure 21.

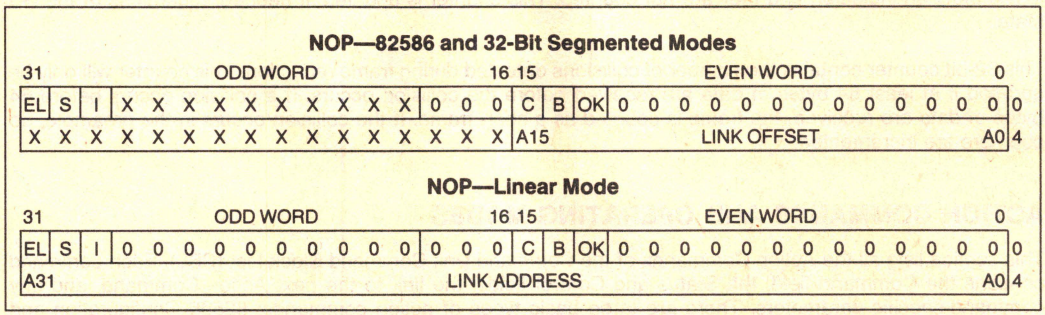


Figure 21

where:

LINK POINTER — In the 82586 or 32-bit Segmented modes this is a 16-bit offset to the next Command Block. In the Linear mode this is the 32-bit address of the next Command Block.

EL — If set, this bit indicates that this command block is the last on the CBL.

S — If set to one, suspend the CU upon completion of this CB.

I — If set to one, the 82596 will generate an interrupt after execution of the command is complete. If I is not set to one, the CX bit will not be set.

CMD (bits 16–18) — The NOP command. Value: 0h.

Bits 19–28 — Reserved (zero in the 32-bit Segmented and Linear modes).

C — This bit indicates the execution status of the command. The CPU initially resets it to zero when the Command Block is placed on the CBL. Following a command Completion, the 82596 will set it to one.

B — This bit indicates that the 82596 is currently executing the NOP command. It is initially reset to zero by the CPU. The 82596 sets it to one when execution begins and to zero when execution is completed. This bit is also set when the 82596 prefetches the command.

NOTE:

The C and B bits are modified in one operation.

OK — Indicates that the command was executed without error. If set to one no error occurred (command executed OK). If zero an error occured.

Individual Address Setup

This command is used to load the 82596 with the Individual Address. This address is used by the 82596 for inserting the Source Address during transmission and recognizing the Destination Address during reception. After RESET, and prior to Individual Address Setup Command execution, the 82596 assumes the Broadcast Address is the Individual Address in all aspects, i.e.:

- This will be the Individual Address Match reference.
- This will be the Source Address of a transmitted frame (for AL-LOC = 0 mode only).

The format of the Individual Address Setup command is shown in Figure 22.

IA Setup—82586 and 32-Bit Segmented Modes

31 ODD WORD 16	15 EVEN WORD 0	
EL S I X X X X X X X X X X 0 0 1 C B OK A 0 0 0 0 0 0 0 0 0 0 0 0		0
INDIVIDUAL ADDRESS 1st byte	A15 LINK OFFSET A0	4
6th byte 5th byte	4th byte 3rd byte	8

IA Setup—Linear Mode

31 ODD WORD 16	15 EVEN WORD 0	
EL S I 0 0 0 0 0 0 0 0 0 0 0 0 1 C B OK A 0 0 0 0 0 0 0 0 0 0 0 0		0
A31 LINK ADDRESS A0		4
4th byte 3rd byte	INDIVIDUAL ADDRESS 1st byte	8
	6th byte 5th byte	C

Figure 22

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted, and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (zero in the 32-bit Segmented and Linear modes).

CMD (bits 16–18) — The Address Setup command. Value: 1h.

INDIVIDUAL ADDRESS — The individual address of the node, 0 to 6 bytes long.

The least significant bit of the Individual Address must be zero for Ethernet (see the Command Structure). However, no enforcement of 0 is provided by the 82596. Thus, an Individual Address with 1 as its least significant bit is a valid Individual Address in all aspects.

The default address length is 6 bytes long, as in 802.3. If a different length is used the IA Setup command should be executed after the Configure command.

Configure

The Configure command loads the 82596 with its operating parameters. It allows changing some of the parameters by specifying a byte count less than the maximum number of configuration bytes (11 in the 82586 mode, 14 in the 32-Bit Segmented and Linear modes). The 82596 configuration depends on its mode of operation. When configuring the 12th byte (Byte 11 undefined) in 82586 mode this byte should be all ones.

- In the 82586 mode the maximum number of configuration bytes is 12. Any number larger than 12 will be reduced to 12 and any number less than 4 will be increased to 4.
- The additional features of the serial side are disabled in the 82586 mode.
- In both the 32-Bit Segmented and Linear modes there are four additional configuration bytes, which hold parameters for additional 82596 features. If these parameters are not accessed, the 82596 will follow their default values.
- For more detailed information refer to the 32-Bit LAN Components User's Manual.

The format of the Configure command is shown in Figure 23, 24 and 25.

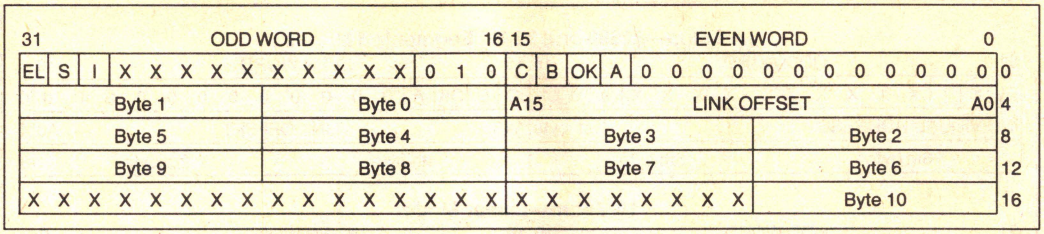


Figure 23. CONFIGURE—82586 Mode

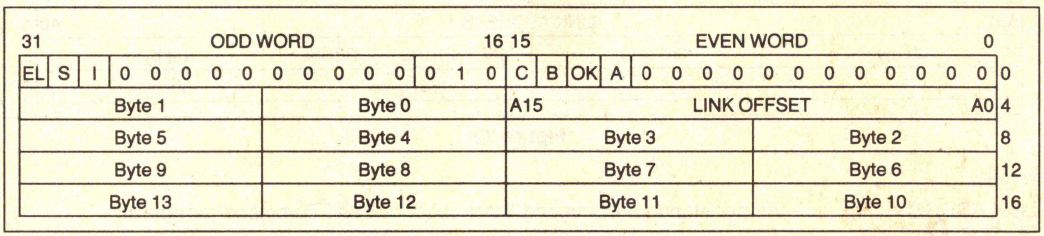


Figure 24. CONFIGURE—32-Bit Segmented Mode

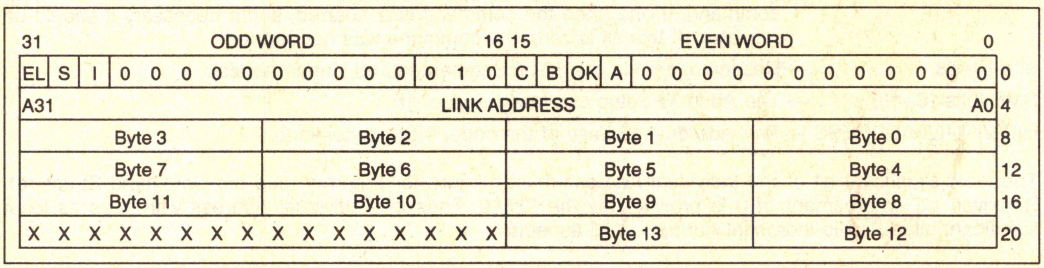


Figure 25. CONFIGURE—Linear Mode

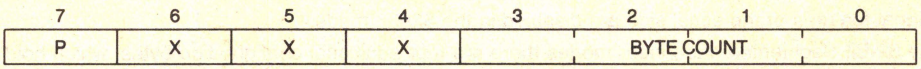
LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to a CU Abort control command. If 1, then the command was aborted and if necessary it should be repeated. If this bit is 0, the command was not aborted.

Bits 19–28 — Reserved (zero in the 32-Bit Segmented and Linear Modes)

CMD (bits 16–18) — The CONFIGURE command. Value: 2h.

The interpretation of the fields follows:

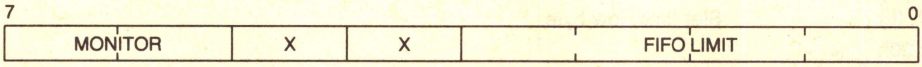


BYTE 0

BYTE CNT (Bits 0–3) — Byte Count. Number of bytes, including this one, that hold parameters to be configured.

PREFETCHED (Bit 7) — Enable the 82596 to write the prefetched bit in all prefetch RBDs.

NOTE:
The P bit is valid only in the new memory structure modes. In 82586 mode this bit is disabled (i.e., no prefetched mark).

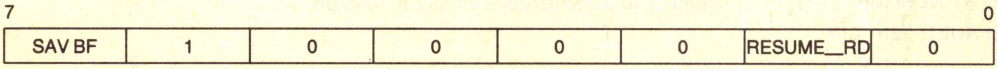


BYTE 1

FIFO Limit (Bits 0–3) — FIFO limit.

MONITOR# (Bits 6–7) — Receive monitor options. If the Byte Count of the configure command is less than 12 bytes then these Monitor bits are ignored.

DEFAULT: C8h

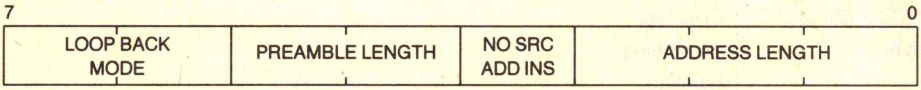


BYTE 2

SAV BF (Bit 7) — 0—Received bad frames are not saved in the memory.
1—Received bad frames are saved in the memory.

DEFAULT: 40h

RESUME_RD (Bit 1) — 0 — The 82596 does not reread the next CB on the list when a CU Resume Control Command is issued.
1 — The 82596 will reread the next CB on the list when a CU Resume Control Command is issued. This is available only on the 82596B stepping.



BYTE 3

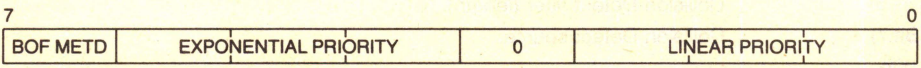
ADR LEN (Bits 0–2) — Address length (any kind).

NO SCR ADD INS (Bit 3) — No Source Address Insertion.
In the 82586 this bit is called AL LOC.

PREAM LEN (Bits 4–5) — Preamble length.

LP BCK MODE (Bits 6–7) — Loopback mode.

DEFAULT: 26h



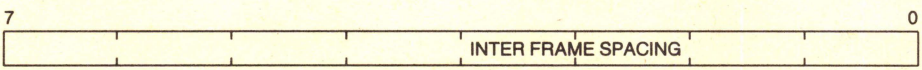
BYTE 4

LIN PRIO (Bits 0–2) — Linear Priority.

EXP PRIO (Bits 4–6) — Exponential Priority.

BOF METD (Bit 7) — Exponential Backoff method.

DEFAULT: 00h



BYTE 5

INTERFRAME SPACING — Interframe spacing.

DEFAULT: 60h

7							0
SLOT TIME - LOW							

BYTE 6

SLOT TIME (L) — Slot time, low byte.

DEFAULT: 00h

7							0
MAXIMUM RETRY NUMBER				0	SLOT TIME - HIGH		

BYTE 7

SLOT TIME (H) (Bits 0–2) — Slot time, high part.

RETRY NUM (Bits 4–7) — Number of transmission retries on collision.

DEFAULT: F2h

7							0
PAD	BIT STUFF	CRC16/ CRC32	NO CRC INSER	TONO CRS	MAN/ NRZ	BC DIS	PRM MODE

BYTE 8

PRM (Bit 0) — Promiscuous mode.

BC DIS (Bit 1) — Broadcast disable.

MANCH/NRZ (Bit 2) — Manchester or NRZ encoding. See specific timing requirements for TXC in Manchester mode.

TONO CRS (Bit 3) — Transmit on no CRS.

NOCRC INS (Bit 4) — No CRC insertion.

CRC-16/CRC-32 (Bit 5) — CRC type.

BIT STF (Bit 6) — Bit stuffing.

PAD (Bit 7) — Padding.

DEFAULT: 00h

7				0
CDT SRC	COLLISION DETECT FILTER	CRS SRC	CARRIER SENSE FILTER	

BYTE 9

CRSF (Bits 0–2) — Carrier Sense filter (length).

CRS SRC (Bit 3) — Carrier Sense source.

CDTF (Bits 4–6) — Collision Detect filter (length).

CDT SRC (Bit 7) — Collision Detect source.

DEFAULT: 00h

7							0
MINIMUM FRAME LENGTH							

BYTE 10

MIN FRAME LEN — Minimum frame length.

DEFAULT: 40h

7							0
MONITOR		MC_ALL	CDBSAC	AUTOTX	CRCINM	LNGFLD	PRECRS

BYTE 11

PRECRS (Bit 0) — Preamble until Carrier Sense

LNGFLD (Bit 1) — Length field. Enables padding at the End-of-Carrier framing (802.3).

CRCINM (Bit 2) — Rx CRC appended to the frame in memory.

AUTOTX (Bit 3) — Auto retransmit when a collision occurs during the preamble.

CDBSAC (Bit 4) — Collision Detect by source address recognition.

MC_ALL (Bit 5) — Enable to receive all MC frames.

MONITOR (Bits 6–7) — Receive monitor options.

DEFAULT: FFH

7							0
0	FDX	0	0	0	0	0	0

BYTE 12

FDX (Bit 6) — Enables Full Duplex operation.

DEFAULT: 00h

7							0
DIS_BOF	MULT_IA	1	1	1	1	1	1

BYTE 13

MULT_IA (Bit 6) — Multiple individual address.

DIS_BOF (Bit 7) — Disable the backoff algorithm.

DEFAULT: 3Fh

A reset (hardware or software) configures the 82596 according to the following defaults.

Table 4. Configuration Defaults

	Parameter	Default Value	Units/Meaning
	ADDRESS LENGTH	**6	Bytes
	A/L FIELD LOCATION	0	Located in FD
*	AUTO RETRANSMIT	1	Auto Retransmit Enable
	BITSTUFFING/EOC	0	EOC
	BROADCAST DISABLE	0	Broadcast Reception Enabled
*	CDBSAC	1	Disabled
	CDT FILTER	0	Bit Times
	CDT SRC	0	External Collision Detection
*	CRC IN MEMORY	1	CRC Not Transferred to Memory
	CRC-16/CRC-32	**0	CRC-32
	CRS FILTER	0	0 Bit Times
	CRS SRC	0	External CRS
*	DISBOF	0	Backoff Enabled
	EXT LOOPBACK	0	Disabled
	EXPONENTIAL PRIORITY	**0	802.3 Algorithm
	EXPONENTIAL BACKOFF METHOD	**0	802.3 Algorithm
*	FULL DUPLEX (FDX)	0	CSMA/CD Protocol (No FDX)
	FIFO THRESHOLD	8	TX: 32 Bytes, RX: 64 Bytes
	INT LOOPBACK	0	Disabled
	INTERFRAME SPACING	**96	Bit Times
	LINEAR PRIORITY	**0	802.3 Algorithm
*	LENGTH FIELD	1	Padding Disabled
	MIN FRAME LENGTH	**64	Bytes
*	MC ALL	1	Disabled
*	MONITOR	11	Disabled
	MANCHESTER/NRZ	0	NRZ
*	MULTI IA	0	Disabled
	NUMBER OF RETRIES	**15	Maximum Number of Retries
	NO CRC INSERTION	0	CRC Appended to Frame
	PREFETCH BIT IN RBD	0	Disabled (Valid Only in New Modes)
	PREAMBLE LENGTH	**7	Bytes
*	Preamble Until CRS	1	Disabled
	PROMISCUOUS MODE	0	Address Filter On
	PADDING	0	No Padding
	SLOT TIME	**512	Bit Times
	SAVE BAD FRAME	0	Discards Bad Frames
	TRANSMIT ON NO CRS	0	Disabled

NOTES:
1. This configuration setup is compatible with the IEEE 802.3 specification.
2. The Asterisk "*" signifies a new configuration parameter not available in the 82586.
3. The default value of the Auto retransmit configuration parameter is enabled(1).
4. Double Asterisk "**" signifies IEEE 802.3 requirements.

Multicast-Setup

This command is used to load the 82596 with the Multicast-IDs that should be accepted. As noted previously, the filtering done on the Multicast-IDs is not perfect and some unwanted frames may be accepted. This command resets the current filter and reloads it with the specified Multicast-IDs. The format of the Multicast-addresses setup command is:

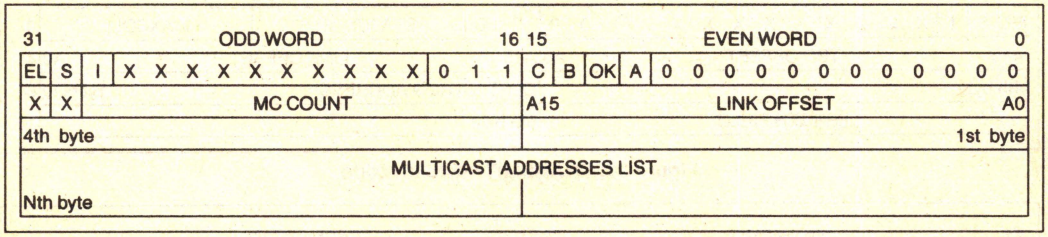


Figure 26. MC Setup—82586 and 32-Bit Segmented Modes

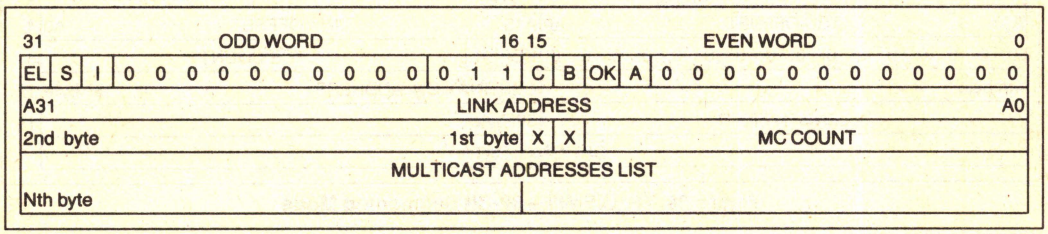


Figure 27. MC Setup—Linear Mode

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to a CU Abort control command. If one, then the command was aborted and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (0 in both the 32-Bit Segmented and Linear Modes).

CMD (bits 16–18) — The MC SETUP command value: 3h.

MC-CNT — This 14-bit field indicates the number of bytes in the MC LIST field. The MC CNT must be a multiple of the ADDR LEN; otherwise, the 82596 reduces the MC CNT to the nearest ADDR LEN multiple. MC CNT = 0 implies resetting the Hash table which is equivalent to disabling the Multicast filtering mechanism.

MC LIST — A list of Multicast Addresses to be accepted by the 82596. The least significant bit of each MC address must be 1.

NOTE:

The list is sequential; i.e., the most significant byte of an address is immediately followed by the least significant byte of the next address.

— When the 82596 is configured to recognize multiple Individual Address (Multi-IA), the MC-Setup command is also used to set up the Hash table for the individual address.

The least significant bit in the first byte of each IA address must be 0.

Transmit

This command is used to transmit a frame of user data onto the serial link. The format of a Transmit command is as follows.

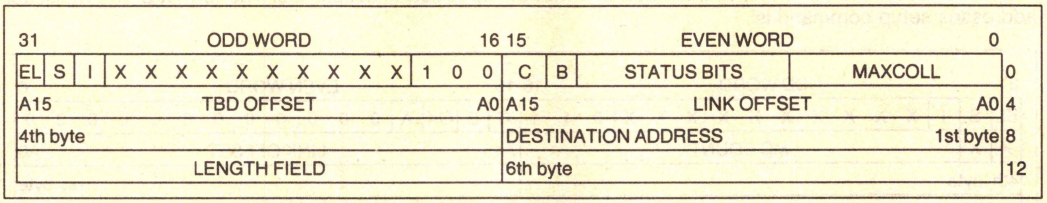


Figure 28. TRANSMIT—82586 Mode

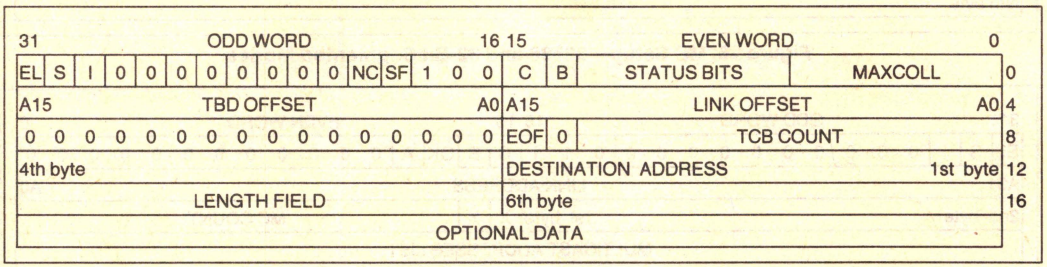


Figure 29. TRANSMIT—32-Bit Segmented Mode

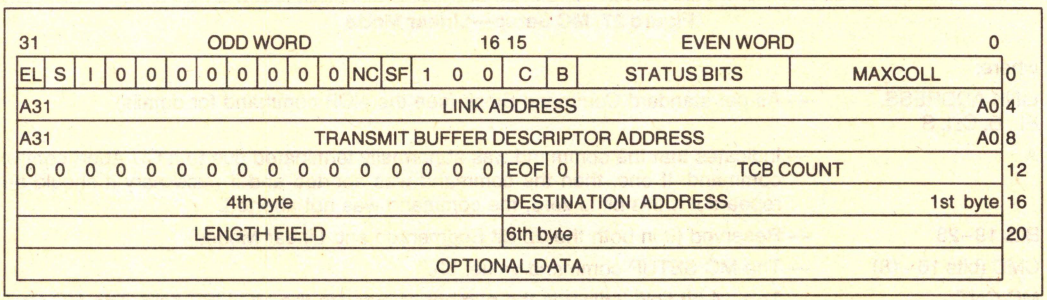
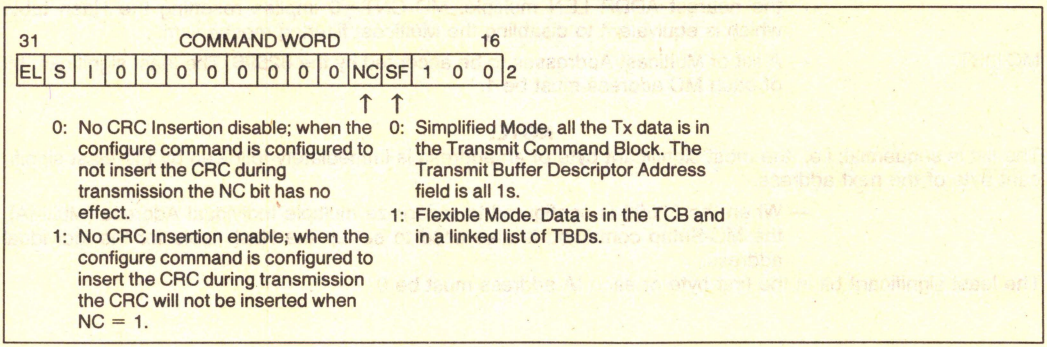


Figure 30. TRANSMIT—Linear Mode



where:

EL, B, C, I, S	— As per standard Command Block (see the NOP command for details).
OK (Bit 13)	— Error free completion.
A (Bit 12)	— Indicates that the command was abnormally terminated due to CU Abort control command. If 1, then the command was aborted, and if necessary it should be repeated. If this bit is 0, the command was not aborted.
Bits 19–28	— Reserved (0 in the 32-bit Segmented and Linear modes).
CMD (Bits 16–18)	— The transmit command: 4h.
Status Bit 11	— Late collision. A late collision (a collision after the slot time is elapsed) is detected.
Status Bit 10	— No Carrier Sense signal during transmission. Carrier Sense signal is monitored from the end of Preamble transmission until the end of the Frame Check Sequence for TONOCRS = 1 (Transmit On No Carrier Sense mode) it indicates that transmission has been executed despite a lack of CRS. For TONOCRS = 0 (Ethernet mode), this bit also indicates unsuccessful transmission (transmission stopped when lack of Carrier Sense has been detected).
Status Bit 9	— Transmission unsuccessful (stopped) due to Loss of $\overline{\text{CTS}}$.
Status Bit 8	— Transmission unsuccessful (stopped) due to DMA Underrun; i.e., the system did not supply data for transmission.
Status Bit 7	— Transmission Deferred, i.e., transmission was not immediate due to previous link activity.
Status Bit 6	— Heartbeat Indicator, Indicates that after a previously performed transmission, and before the most recently performed transmission, (Interframe Spacing) the CDT signal was monitored as active. This indicates that the Ethernet Transceiver Collision Detect logic is performing properly. The Heartbeat is monitored during the Interframe Spacing period.
Status Bit 5	— Transmission attempt was stopped because the number of collisions exceeded the maximum allowable number of retries.
Status Bit 4	— 0 (Reserved).
MAX-COL (Bits 3–0)	— The number of Collisions experienced during this frame. Max Col = 0 plus S5 = 1 indicates 16 collisions.
LINK OFFSET	— As per standard Command Block (see the NOP Command for details)
TBD POINTER	— In the 82586 and 32-bit Segmented modes this is the offset of the first Tx Buffer Descriptor containing the data to be transmitted. In the Linear mode this is the 32-bit address of the first Tx Buffer Descriptor on the list. If the TBD POINTER is all 1s it indicates that no TBD is used.
DEST ADDRESS	— Contains the Destination Address of the frame. The least significant bit (MC) indicates the address type. MC = 0: Individual Address. MC = 1: Multicast or Broadcast Address. If the Destination Address bits are all 1s this is a Broadcast Address.
LENGTH FIELD	— The contents of this 2-byte field are user defined. In 802.3 it contains the length of the data field. It is placed in memory in the same order it is transmitted; i.e., most significant byte first, least significant byte second.
TCB COUNT	— This 14-bit counter indicates the number of bytes that will be transmitted from the Transmit Command Block, starting from the third byte after the TCB COUNT field (address $n+12$ in the 32-bit Segmented mode, $N+16$ in the Linear mode). The TCB COUNT field can be any number of bytes (including an odd byte), this allows the user to transmit a frame with a header having an odd number of bytes. The TCB COUNT field is not used in the 82586 mode.
EOF Bit	— Indicates that the whole frame is kept in the Transmit Command Block. In the Simplified memory model it must be always asserted.

The interpretation of what is transmitted depends on the No Source Address insertion configuration bit and the memory model being used.

NOTES:

1. The Destination Address and the Length Field are sequential. The Length Field immediately follows the most significant byte of the Destination Address.
2. In case the 82596 is configured with No Source Address insertion bit equal to 0, the 82596 inserts its configured Source Address in the transmitted frame.
   - In the 82586 mode, or when the Simplified memory model is used, the Destination and Length fields of the transmitted frame are taken from the Transmit Command Block.
   - If the FLEXIBLE memory model is used, the Destination and Length fields of the transmitted frame can be found either in the TCB or TBD, depending on the TCB COUNT.
3. If the 82596 is configured with the Address/Length Field Location equal to 1, the 82596 does not insert its configured Source Address in the transmitted frame. The first (2 × Address Length) + 2 bytes of the transmitted frame are interpreted as Destination Address, Source Address, and Length fields respectively. The location of the first transmitted byte depends on the operational mode of the 82596:
   - In the 82586 mode, it is always the first byte of the first Tx Buffer.
   - In both the 32-bit Segmented and Linear modes it depends on the SF bit and TCB COUNT:
     - — In the Simplified memory mode the first transmitted byte is always the third byte after the TCB COUNT field.
     - — In the Flexible mode, if the TCB COUNT is greater than 0 then it is the third byte after the TCB COUNT field. If TCB COUNT equals 0 then it is first byte of the first Tx Buffer.
   - Transmit frames shorter than six bytes are invalid. The transmission will be aborted (only in 82586 mode) because of a DMA Underrun.
4. Frames which are aborted during transmission are jammed. Such an interruption of transmission can be caused by any reason indicated by any of the status bits 8, 9, 10 and 12.

Jamming Rules

1. Jamming will not start before completion of preamble transmission.
2. Collisions detected during transmission of the last 11 bits will not result in jamming.

The format of a Transmit Buffer Descriptor is:

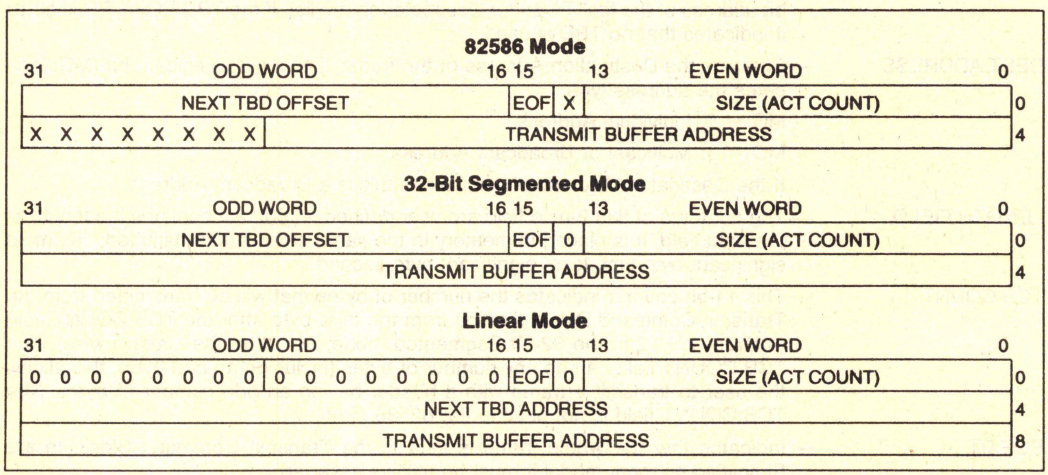


Figure 31

where:

EOF — This bit indicates that this TBD is the last one associated with the frame being transmitted. It is set by the CPU before transmit.

SIZE (ACT COUNT) — This 14-bit quantity specifies the number of bytes that hold information for the current buffer. It is set by the CPU before transmission.

NEXT TBD ADDRESS — In the 82586 and 32-bit Segmented modes, it is the offset of the next TBD on the list. In the Linear mode this is the 32-bit address of the next TBD on the list. It is meaningless if EOF = 1.

BUFFER ADDRESS — The starting address of the memory area that contains the data to be sent. In the 82586 mode, this is a 24-bit address (A31–A24 are considered to be zero). In the 32-bit Segmented and Linear modes this is a 32-bit address. This buffer can be byte aligned for the 82596 B step.

TDR

This operation activates Time Domain Reflectomet, which is a mechanism to detect open or short circuits on the link and their distance from the diagnosing station. The TDR command has no parameters. The TDR transmit sequence was changed, compared to the 82586, to form a regular transmission. The TDR command is designed to be used statically. Make sure that both the CU and RU are idle before attempting a TDR command. The TDR bit stream is as follows.

— Preamble

— Source address

— Another Source address (the TDR frame is transmitted back to the sending station, so DEST ADR = SRC ADR).

— Data field containing 7Eh patterns.

— Jam Pattern, which is the inverse CRC of the transmitted frame.

Maximum length of the TDR frame is 2048 bits. If the 82596 senses collision while transmitting the TDR frame it transmits the jam pattern and stops the transmission. The 82596 then triggers an internal timer (STC); the timer is reset at the beginning of transmission and reset if CRS is returned. The timer measures the time elapsed from the start of transmission until an echo is returned. The echo is indicated by Collision Detect going active or a drop in the Carrier Sense signal. The following table lists the possible cases that the 82596 is able to analyze.

Conditions of TDR as Interpreted by the 82596

Transceiver Type / Condition	Ethernet	Non Ethernet
Carrier Sense was inactive for 2048-bit-time periods	Short or Open on the Transceiver Cable	NA
Carrier Sense signal dropped	Short on the Ethernet cable	NA
Collision Detect went active	Open on the Ethernet cable	Open on the Serial Link
The Carrier Sense Signal did not drop or the Collision Detect did not go active within 2048-bit time period	No Problem	No Problem

An Ethernet transceiver is defined as one that returns transmitted data on the receive pair and activates the Carrier Sense Signal while transmitting. A Non-Ethernet Transceiver is defined as one that does not do so.

The format of the Time Domain Reflectometer command is:

82586 and 32-Bit Segmented Modes

31															16	15															0
ODD WORD																EVEN WORD															
EL	S	I	X	X	X	X	X	X	X	X	X	1	0	1		C	B	OK	0	0	0	0	0	0	0	0	0	0	0	0	0
LNK OK	XVR PRB	ET OPN	ET SRT	X	TIME (11 bits)											A15	LINK OFFSET														A0

Linear Mode

31															16	15															0
ODD WORD																EVEN WORD															
EL	S	I	0	0	0	0	0	0	0	0	0	1	0	1		C	B	OK	0	0	0	0	0	0	0	0	0	0	0	0	0
A31	LINK ADDRESS																														A0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LNK OK	XVR PRB	ET OPN	ET SRT	X	TIME (11 bits)										

Figure 32. TDR

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details).

A — Indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted, and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (0 in the 32-bit Segmented and Linear Modes).

CMD (Bits 16–18) — The TDR command. Value: 5h.

TIME — An 11-bit field that specifies the number of TxC cycles that elapsed before an echo was observed. No echo is indicated by a reception consisting of "1s" only. Because the network contains various elements such as transceiver links, transceivers, Ethernet, repeaters etc., the TIME is not exactly proportional to the problems distance.

LNK OK (Bit 15) — No link problem identified. TIME = 7FFh.

XCVR PRB (Bit 14) — Indicates a Transceiver problem. Carrier Sense was inactive for 2048-bit time period. LNK OK = 0. TIME = 7FFh.

ET OPN (Bit 13) — The transmission line is not properly terminated. Collision Detect went active and LNK OK = 0.

ET SRT (Bit 12) — There is a short circuit on the transmission line. Carrier Sense Signal dropped and LNK OK = 0.

DUMP

This command causes the contents of various 82596 registers to be placed in a memory area specified by the user. It is supplied as a 82596 self-diagnostic tool, and to provide registers of interest to the user. The format of the DUMP command is:

82586 and 32-Bit Segmented Modes

31			ODD WORD									16	15					EVEN WORD											0
EL	S	I	X	X	X	X	X	X	X	X	X	X	1	1	0	C	B	OK	0	0	0	0	0	0	0	0	0	0	0	0
A15			BUFFER OFFSET									A0	A15					LINK OFFSET											A0	

Linear Mode

31			ODD WORD									16	15					EVEN WORD											0
EL	S	I	X	X	X	X	X	X	X	X	X	X	1	1	0	C	B	OK	0	0	0	0	0	0	0	0	0	0	0	0
A31			LINK ADDRESS																										A0	
A31			BUFFER ADDRESS																										A0	

Figure 33. Dump

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details).

OK — Indicates error free completion.

Bits 19–28 — Reserved (0 in the 32-bit Segmented and Linear Modes).

CMD (Bits 16–18) — The Dump command. Value: 6h.

BUFFER POINTER — In the 82586 and 32-bit Segmented modes this is the 16-bit-offset portion of the dump area address. In the Linear mode this is the 32-bit linear address of the dump area.

Dump Area Information Format

- The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586. The compatible data will be marked with an asterisk.
- In 82586 mode the dump area is 170 bytes.
- The DUMP area format of the 32-bit Segmented and Linear modes is described in Figure 35.
- The size of the dump area of the 32-bit Segmented and Linear modes is 304 bytes.
- When the Dump is executed by the Port command an extra word will be appended to the Dump Area. The extra word is a copy of the Dump Area status word (containing the C, B, and OK Bits). The C and OK Bits are set when the 82596 has completed the Port Dump command.

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
DMA CONTROL REGISTER	00
CONFIGURE BYTES* 3, 2	02
CONFIGURE BYTES* 5, 4	04
CONFIGURE BYTES* 7, 6	06
CONFIGURE BYTES* 9, 8	08
CONFIGURE BYTES* 10	0A
I.A. BYTES 1, 0*	0C
I.A. BYTES 3, 2*	0E
I.A. BYTES 5, 4*	10
LAST T.X. STATUS*	12
T.X. CRC BYTES 1, 0*	14
T.X. CRC BYTES 3, 2*	16
R.X. CRC BYTES 1, 0*	18
R.X. CRC BYTES 3, 2*	1A
R.X. TEMP MEMORY 1, 0*	1C
R.X. TEMP MEMORY 3, 2*	1E
R.X. TEMP MEMORY 5, 4*	20
LAST RECEIVED STATUS*	22
HASH REGISTER BYTES 1, 0*	24
HASH REGISTER BYTES 3, 2*	26
HASH REGISTER BYTES 5, 4*	28
HASH REGISTER BYTES 7, 6*	2A
SLOT TIME COUNTER*	2C
WAIT TIME COUNTER*	2E
MICRO MACHINE** . REGISTER FILE . . 60 BYTES	30 6A
MICRO MACHINE LFSR**	6C
MICRO MACHINE** . FLAG ARRAY . . 14 BYTES	6E 7A
QUEUE MEMORY** . CU PORT 8 BYTES	7C . 82
MICRO MACHINE ALU**	84
RESERVED**	86
M.M. TEMP A ROTATE R**	88
M.M. TEMP A**	8A
T.X. DMA BYTE COUNT**	8C
M.M. INPUT PORT ADDRESS**	8E
T.X. DMA ADDRESS	90
M.M. OUTPUT PORT**	92
R.X. DMA BYTE COUNT**	94
M.M. OUTPUT PORT ADDRESS REGISTER**	96
R. DMA ADDRESS**	98
RESERVED**	9A
BUS THROTTLE TIMERS	9C
DIU CONTROL REGISTER**	9E
RESERVED**	A0
DMA CONTROL REGISTER**	A2
BIU CONTROL REGISTER**	A4
M.M. DISPATCHER REG.**	A6
M.M. STATUS REGISTER**	A8

*The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586.

**These bytes are not user defined, results may vary from Dump command to Dump command.

Figure 34. Dump Area Format—82586 Mode

31	0	
CONFIGURE BYTES 5, 4, 3, 2		00
CONFIGURE BYTES 9, 8, 7, 6		04
CONFIGURE BYTES 13, 12, 11, 10		08
I.A. BYTES 1, 0	X X X X X X X X	0C
I.A. BYTES 5, 2		10
TX CRC BYTES 0, 1	LAST T.X. STATUS	14
RX CRC BYTES 0, 1	TX CRC BYTES 3, 2	18
RX TEMP MEMORY 1, 0	RX CRC BYTES 3, 2	1C
R.X. TEMP MEMORY 5, 2		20
HASH REGISTERS 1, 0	LAST R.X. STATUS	24
HASH REGISTER BYTES 5, 2		28
SLOT TIME COUNTER	HASH REGISTERS 7, 6	2C
RECEIVE FRAME LENGTH	WAIT-TIME COUNTER	30
MICRO MACHINE**		34
REGISTER FILE		.
128 BYTES		B0
MICRO MACHINE LFSR**		B4
MICRO MACHINE**		B8
FLAG ARRAY		.
28 BYTES		D0
M.M. INPUT PORT**		D4
16 BYTES		.
		E0
MICRO MACHINE ALU**		E4
RESERVED**		E8
M.M. TEMP A ROTATE R.**		EC
M.M. TEMP A**		F0
T.X. DMA BYTE COUNT**		F4
M.M. INPUT PORT ADDRESS REGISTER**		F8
T.X. DMA ADDRESS**		FC
M.M. OUTPUT PORT REGISTER**		100
R.X. DMA BYTE COUNT**		104
M.M. OUTPUT PORT ADDRESS REGISTER**		108
R.X. DMA ADDRESS REGISTER**		10C
RESERVED**		110
BUS THROTTLE TIMERS		114
DIU CONTROL REGISTER**		118
RESERVED**		11C
DMA CONTROL REGISTER**		120
BIU CONTROL REGISTER**		124
M.M. DISPATCHER REG.**		128
M.M. STATUS REGISTER**		12C

The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586.
**These bytes are not user defined, results may vary from Dump command to Dump command.

Figure 35. Dump Area Format—Linear and 32-Bit Segmented Mode

Diagnose

The Diagnose Command triggers an internal self-test procedure that checks internal 82596 hardware, which includes:

- Exponential Backoff Random Number Generator (Linear Feedback Shift Register).
- Exponential Backoff Timeout Counter.
- Slot Time Period Counter.
- Collision Number Counter.
- Exponential Backoff Shift Register.
- Exponential Backoff Mask Logic.
- Timer Trigger Logic.

This procedure checks the operation of the Backoff block, which resides in the serial side and is not easily controlled. The Diagnose command is performed in two phases.

The format of the 82596 Diagnose command is:

82586 and 32-Bit Segmented Modes

31														16 15																0
ODD WORD																				EVEN WORD										
EL	S	I	X	X	X	X	X	X	X	X	X	X	1	1	1	C	B	OK	0	F	0	0	0	0	0	0	0	0	0	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A15					LINK OFFSET									A0

Linear Mode

31														16 15																0
ODD WORD																				EVEN WORD										
EL	S	I	0	0	0	0	0	0	0	0	0	0	1	1	1	C	B	OK	0	F	0	0	0	0	0	0	0	0	0	0
A31																					LINK ADDRESS										A0

Figure 36. Diagnose

where:

LINK ADDRESS, EL, B, C, I, S	— As per standard Command Block (see the NOP command for details).
Bits 19–28	— Reserved (0 in the 32-bit Segmented and Linear Modes).
CMD (bits 16–18)	— The Diagnose command. Value: 7h.
OK (bit 13)	— Indicates error free completion.
F (bit 11)	— Indicates that the self-test procedure has failed.

RECEIVE FRAME DESCRIPTOR

Each received frame is described by one Receive Frame Descriptor (see Figure 37). Two new memory structures are available for the received frames. The structures are available only in the Linear and 32-bit Segmented modes.

Simplified Memory Structure

The first is the Simplified memory structure, the data section of the received frame is part of the RFD and is located immediately after the Length Field. Receive Buffer Descriptors are not used with the Simplified structure, it is primarily used to make programming easier. If the length of the data area described in the Size Field is smaller than the incoming frame, the following happens.

1. The received frame is truncated.
2. The No Resource error counter is updated.
3. If the 82596 is configured to Save Bad Frames the RFD is not reused; otherwise, the same RFD is used to hold the next received frame, and the only action taken regarding the truncated frame is to update the counter.
4. The 82596 continues to receive the next frame in the next RFD.

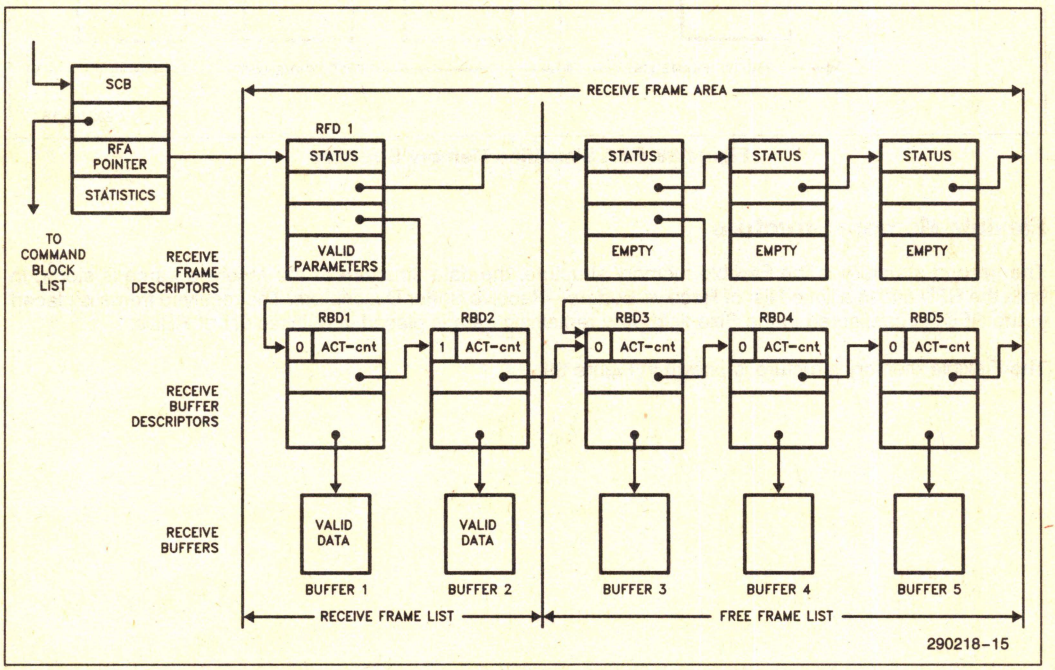


Figure 37. The Receive Frame Area

Note that this sequence is very useful for monitoring. If the 82596 is configured to Save Bad Frames, to receive in Promiscuous mode, and to use the Simplified memory structure, any programmed length of received data can be saved in memory.

The Simplified memory structure is shown in Figure 38.

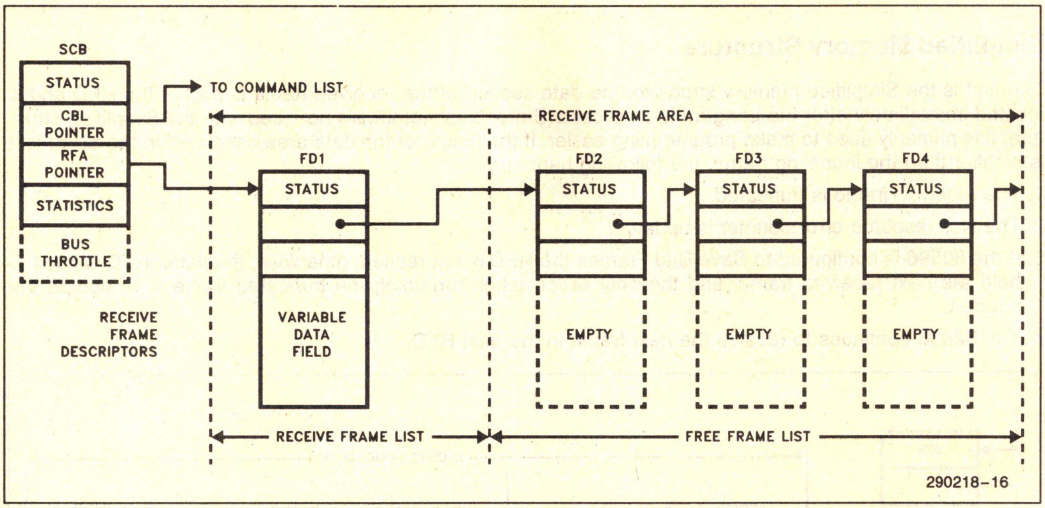


Figure 38. RFA Simplified Memory Structure

Flexible Memory Structure

The second structure is the Flexible memory structure, the data structure of the received frame is stored in both the RFD and in a linked list of Receive Buffers—Receive Buffer Descriptors. The received frame is placed in the RFD as configured in the Size field. Any remaining data is placed in a linked list of RBDs.

The Flexible memory structure is shown in Figure 39.

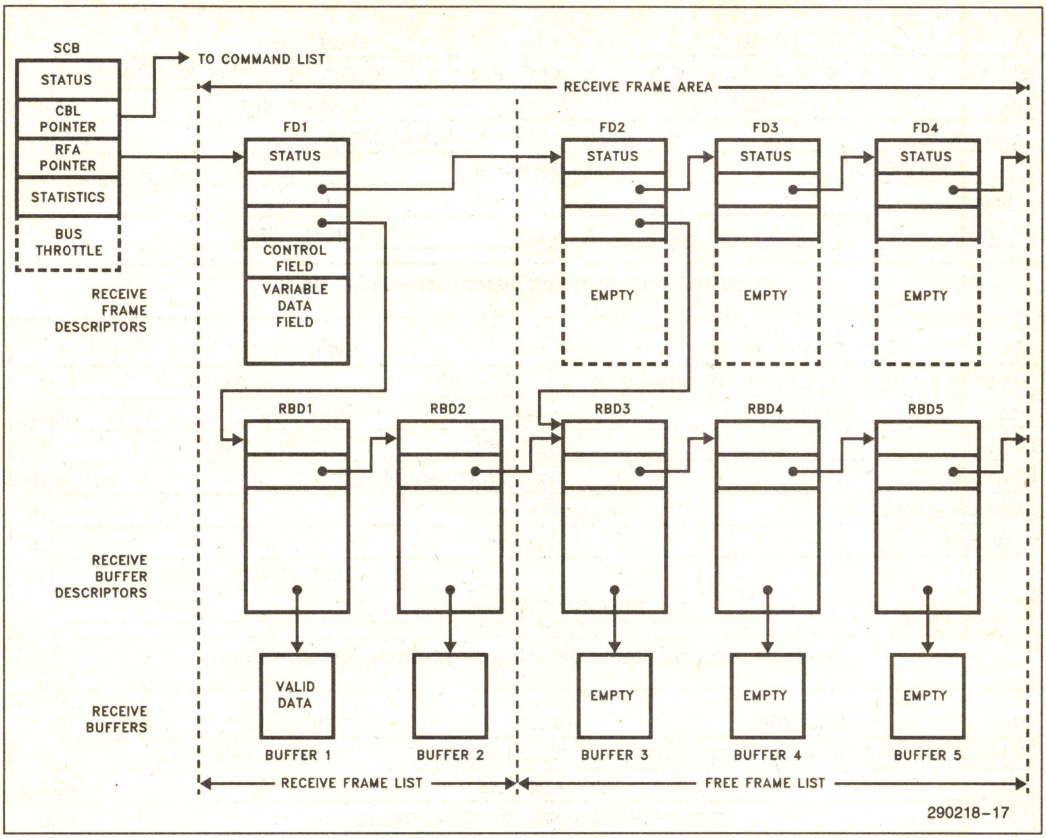


Figure 39. RFA Flexible Memory Structure

Buffers on the receive side can be different lengths. The 82596 will not place more bytes into a buffer than indicated in the associated RBD. The 82596 will fetch the next RBD before it is needed. The 82596 will attempt to receive frames as long as the FBL is not exhausted. If there are no more buffers, the 82596 Receive Unit will enter the No Resources state. Before starting the RU, the CPU must place the FBL pointer in the RBD pointer field of the first RFD. All remaining RBD pointer fields for subsequent RFDs should be "1s." If the Receive Frame Descriptor and the associated Receive Buffers are not reused (e.g., the frame is properly received or the 82596 is configured to Save Bad Frames), the 82596 writes the address of the next free RBD to the RBD pointer field of the next RFD.

Receive Buffer Descriptor (RBD)

The RBDs are used to store received data in a flexible set of linked buffers. The portion of the frame's data field that is outside the RFD is placed in a set of buffers chained by a sequence of RBDs. The RFD points to the first RBD, and the last RBD is flagged with an EOF bit set to 1. Each buffer in the linked list of buffers related to a particular frame can be any size up to 2^{14} bytes but must be word aligned (begin on an even numbered byte). This ensures optimum use of the memory resources while maintaining low overhead. All buffers in a frame are filled with the received data except for the last, in which the actual count can be smaller than the allocated buffer space.

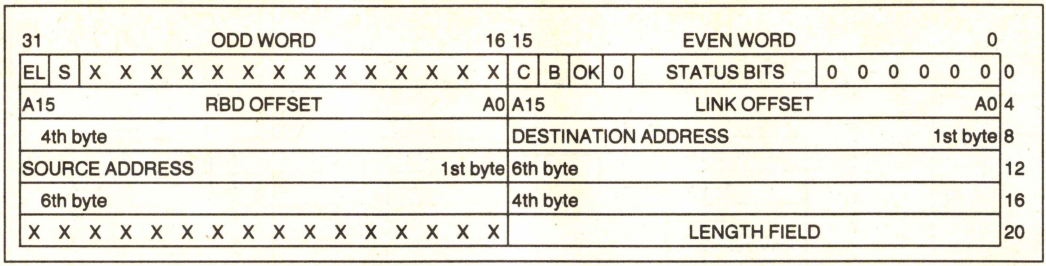


Figure 40. Receive Frame Descriptor—82586 Mode

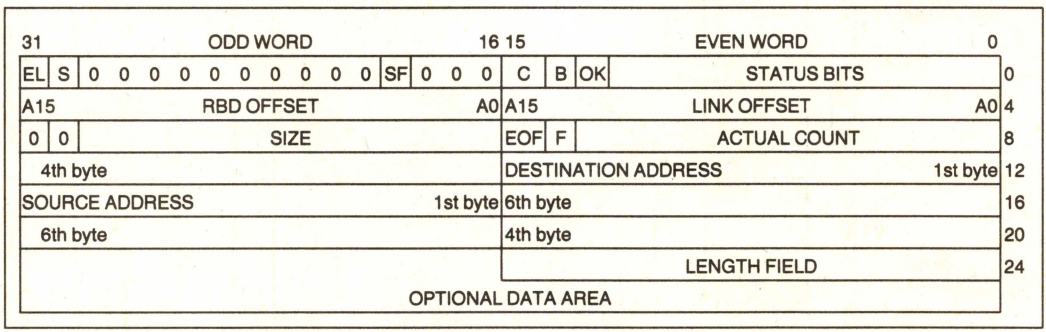


Figure 41. Receive Frame Descriptor—32-Bit Segmented Mode

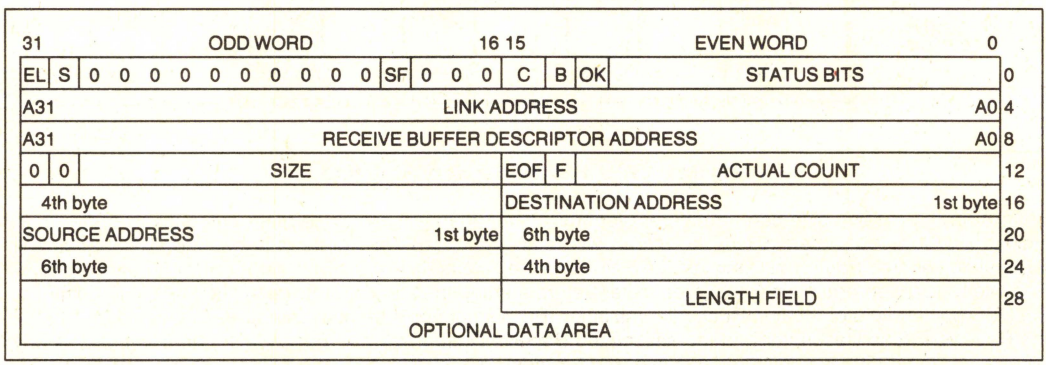


Figure 42. Receive Frame Descriptor—Linear Mode

where:

EL — When set, this bit indicates that this RFD is the last one on the RDL.

S — When set, this bit suspends the RU after receiving the frame.

SF — This bit selects between the Simplified or the Flexible mode.

0 — Simplified mode, all the RX data is in the RFD. RBD ADDRESS field is all "1s."

1 — Flexible mode. Data is in the RFD and in a linked list of Receive Buffer Descriptors.

C — This bit indicates the completion of frame reception. It is set by the 82596.

B — This bit indicates that the 82596 is currently receiving this frame, or that the 82596 is ready to receive the frame. It is initially set to 0 by the CPU. The 82596 sets it to 1 when reception set up begins, and to 0 upon completion. The C and B bits are set during the same operation.

OK (bit 13) — Frame received successfully, without errors. RFDs with bit 13 equal to 0 are possible only if the save bad frames, configuration option is selected. Otherwise all frames with errors will be discarded, although statistics will be collected on them.

STATUS — The results of the Receive operation. Defined bits are,

Bit 12: Length error if configured to check length

Bit 11: CRC error in an aligned frame

Bit 10: Alignment error (CRC error in misaligned frame)

Bit 9: Ran out of buffer space—no resources

Bit 8: DMA Overrun failure to acquire the system bus.

Bit 7: Frame too short.

Bit 6: No EOP flag (for Bit stuffing only)

Bit 5: When the SF bit equals zero, and the 82596 is configured to save bad frames, this bit signals that the receive frame was truncated. Otherwise it is zero.

Bits 2–4: Zeros

Bit 1: When it is zero, the destination address of the received frame matches the IA address. When it is a 1, the destination address of the received frame did not match the individual address. For example, a multicast address or broadcast address will set this bit to a 1.

Bit 0: Receive collision. A collision is detected during reception and the collision occurred after the destination address was received.

LINK ADDRESS — A 16-bit offset (32-bit address in the Linear mode) to the next Receive Frame Descriptor. The Link Address of the last frame can be used to form a cyclical list.

RBD POINTER — The offset (address in the Linear mode) of the first RBD containing the received frame data. An RBD pointer of all ones indicates no RBD.

EOF
F
SIZE
ACT COUNT — These fields are for the Simplified and Flexible memory models. They are exactly the same as the respective fields in the Receive Buffer Descriptor. See the next section for detailed explanation of their functions.

MC — Multicast bit.

DESTINATION ADDRESS — The contents of the destination address of the receive frame. The field is 0 to 6 bytes long.

SOURCE ADDRESS — The contents of the Source Address field of the received frame. It is 0 to 6 bytes long.

LENGTH FIELD — The contents of this 2-byte field are user defined. In 802.3 it contains the length of the data field. It is placed in memory in the same order it is received, i.e., most significant byte first, least significant byte second.

NOTES

1. The Destination address, Source address and Length fields are packed, i.e., one field immediately follows the next.
2. The affect of Address/Length Location (No Source Address Insertion) configuration parameter while receiving is as follows:

— 82586 Mode: The Destination address, Source address and Length field are not used, they are placed in the RX data buffers.

— 32-Bit Segmented and Linear Modes: when the Simplified memory model is used, the Destination address, Source address and Length fields reside in their respective fields in the RFD. When the Flexible memory strucrture is used the Destination address, Source address, and Length field locations depend on the SIZE field of the RFD. They can be placed in the RFD, in the RX data buffers, or partially in the RFD and the rest in the RX data buffers, depending on the SIZE field value.

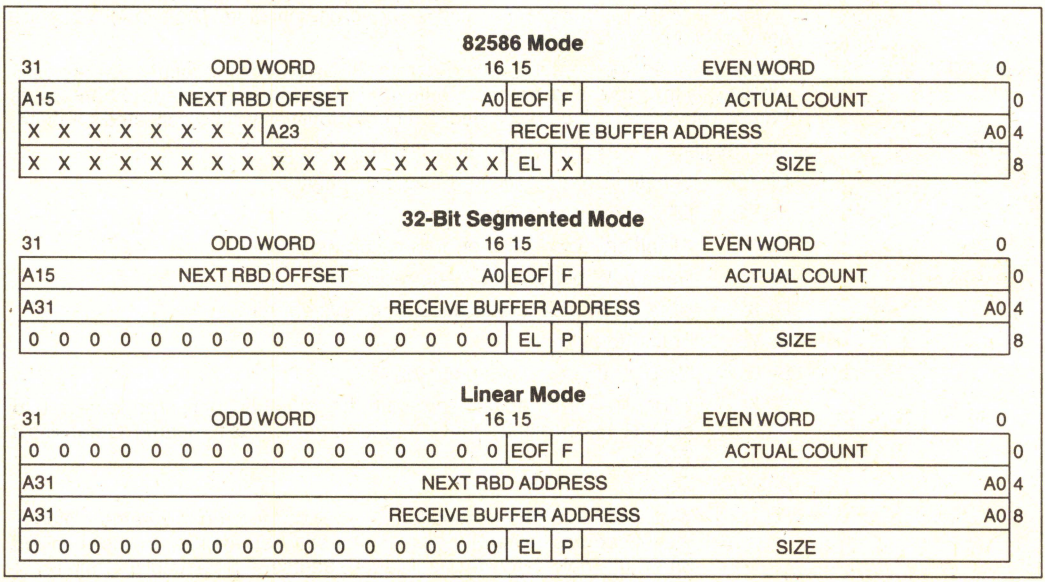


Figure 43. Receive Buffer Descriptor

where:

EOF — Indicates that this is the last buffer related to the frame. It is cleared by the CPU before starting the RU, and is written by the 82596 at the end of reception of the frame.

F — Indicates that this buffer has already been used. The Actual Count has no meaning unless the F bit equals one. This bit is cleared by the CPU before starting the RU, and is set by the 82596 after the associated buffer has been. This bit has the same meaning as the Complete bit in the RFD and CB.

ACT COUNT — This 14-bit quantity indicates the number of meaningful bytes in the buffer. It is cleared by the CPU before starting the RU, and is written by the 82596 after the associated buffer has already been used. In general, after the buffer is full, the Actual Count value equals the size field of the same buffer. For the last buffer of the frame, Actual Count can be less than the buffer size.

NEXT BD ADDRESS — The offset (absolute address in the Linear mode) of the next RBD on the list. It is meaningless if EL = 1.

BUFFER ADDRESS — The starting address of the memory area that contains the received data. In the 82586 mode, this is a 24-bit address (with pins A24–A31 = 0). In the 32-bit Segmented and Linear modes this is a 32-bit address.

EL — Indicates that the buffer associated with this RBD is last in the FBL.

P — This bit indicates that the 82596 has already prefetched the RBDs and any change in the RBD data will be ignored. This bit is valid only in the new 82596 memory modes, and if this feature has been enabled during configure command. The 82596 Prefetches the RBDs in locked cycles; after prefetching the RBD the 82596 performs a write cycle where the P bit is set to one and the rest of the data remains unchanged. The CPU is responsible for resetting it in all RBDs. The 82596 will not check this bit before setting it.

SIZE — This 14-bit quantity indicates the size, in bytes, of the associated buffer. This quantity must be an even number.

PGA PACKAGE THERMAL SPECIFICATION

Parameter	Thermal Resistance
θ_{JC}	3°C/W
θ_{JA}	24°C/W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

ELECTRICAL AND TIMING CHARACTERISTICS

Absolute Maximum Ratings

- Storage Temperature ..... −65°C to +150°C
- Case Temperature under Bias −65°C to +110°C
- Supply Voltage with Respect to V_{SS} ..... −0.5V to +6.5V
- Voltage on Other Pins .... −0.5V to V_{CC} + 0.5V

DC Characteristics

T_C = 0°C–85°C, V_{CC} = 5V ±10% LE/$\overline{BE}$ have MOS levels (see V_{MIL}, V_{MIH}).
All other signals have TTL levels (see V_{IL}, V_{IH}, V_{OL}, V_{OH}).

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage (TTL)	−0.3	+0.8	V	
V_{IH}	Input High Voltage (TTL)	2.0	V_{CC} + 0.3	V	
V_{MIL}	Input Low Voltage (MOS)	−0.3	+0.8	V	
V_{MIH}	Input High Voltage (MOS)	3.7	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage (TTL)		0.45	V	I_{OL} = 4.0 mA
V_{CIL}	$\overline{RXC}$, $\overline{TXC}$ Input Low Voltage	−0.5	0.6	V	
V_{CIH}	$\overline{RXC}$, $\overline{TXC}$ Input High Voltage	3.3	V_{CC}+0.5	V	
V_{OH}	Output High Voltage (TTL)	2.4		V	I_{OH} = 0.9 mA–1 mA
I_{LI}	Input Leakage Current		±15	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±15	μA	$0.45 < V_{OUT} < V_{CC}$
C_{IN}	Capacitance of Input Buffer		10	pF	FC = 1 MHz
C_{OUT}	Capacitance of Input/Output Buffer		12	pF	FC = 1 MHz
C_{CLK}	CLK Capacitance		20	pF	FC = 1 MHz
I_{CC}	Power Supply		200	mA	At 25 MHz I_{CC} Typical = 100 mA
I_{CC}	Power Supply		300	mA	At 33 MHz I_{CC} Typical = 150 mA

AC Characteristics

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C–+85°C, V_{CC} = 5V ±10%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	16 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	16 MHz	1X CLK Input
T1	CLK Period	62.5	80	
T1a	CLK Period Stability		0.1%	Adjacent CLK Δ
T2	CLK High	20		2.0V
T3	CLK Low	20		0.8V
T4	CLK Rise Time		8	0.8V to 2.0V
T5	CLK Fall Time		8	2.0V to 0.8V
T6	$\overline{BEn}$, $\overline{LOCK}$, and A2–A31 Valid Delay	3	23	
T6a	$\overline{BLAST}$, $\overline{PCHK}$ Valid Delay	3	32	
T7	$\overline{BEn}$, $\overline{LOCK}$, $\overline{BLAST}$, A2–A31 Float Delay	3	39	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	23	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	3	39	
T10	D0–D31, DPn Write Data Valid Delay	3	27	
T11	D0–D31, DPn Write Data Float Delay	3	39	
T12	HOLD Valid Delay	2	30	
T13	CA and BREQ Setup Time	11		1, 2
T14	CA and BREQ Hold Time	6		1, 2
T15	$\overline{BS16}$ Setup Time	12		2
T16	$\overline{BS16}$ Hold Time	5		2
T17	$\overline{BRDY}$, $\overline{RDY}$ Setup Time	12		2
T18	$\overline{BRDY}$, $\overline{RDY}$ Hold Time	5		2
T19	D0–D31, DPn READ Setup Time	10		2
T20	D0–D31, DPn READ Hold Time	6		2
T21	AHOLD and HLDA Setup Time	15		1, 2
T22	AHOLD Hold Time	5		1, 2
T22a	HLDA Hold Time	5		1, 2
T23	RESET Setup Time	14		1, 2
T24	RESET Hold Time	5		1, 2
T25	INT/$\overline{INT}$ Valid Delay	1	23	
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	2 T1		1, 2, 3
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	10		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	6		2
T29	$\overline{PORT}$ Setup Time	11		2
T30	$\overline{PORT}$ Hold Time	5		2
T31	$\overline{BOFF}$ Setup Time	12		2
T32	$\overline{BOFF}$ Hold Time	5		2

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C–+85°C, V_{CC} = 5V ±10%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	20 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	20 MHz	1X CLK Input
T1	CLK Period	50	80	
T1a	CLK Period Stability		0.1%	Adjacent CLK Δ
T2	CLK High	16		2.0V
T3	CLK Low	16		0.8V
T4	CLK Rise Time		6	0.8V to 2.0V
T5	CLK Fall Time		6	2.0V to 0.8V
T6	$\overline{BEn}$, $\overline{LOCK}$, and A2–A31 Valid Delay	3	20	
T6a	$\overline{BLAST}$, $\overline{PCHK}$ Valid Delay	3	25	
T7	$\overline{BEn}$, $\overline{LOCK}$, $\overline{BLAST}$, A2–A31 Float Delay	3	34	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	20	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	3	34	
T10	D0–D31, DPn Write Data Valid Delay	3	23	
T11	D0–D31, DPn Write Data Float Delay	3	34	
T12	HOLD Valid Delay	2	25	
T13	CA and BREQ Setup Time	10		1, 2
T14	CA and BREQ Hold Time	6		1, 2
T15	$\overline{BS16}$ Setup Time	12		2
T16	$\overline{BS16}$ Hold Time	4		2
T17	$\overline{BRDY}$, $\overline{RDY}$ Setup Time	12		2
T18	$\overline{BRDY}$, $\overline{RDY}$ Hold Time	4		2
T19	D0–D31, DPn READ Setup Time	6		2
T20	D0–D31, DPn READ Hold Time	5		2
T21	AHOLD and HLDA Setup Time	15		1, 2
T22	AHOLD Hold Time	4		1, 2
T22a	HLDA Hold Time	5		1, 2
T23	RESET Setup Time	12		1, 2
T24	RESET Hold Time	4		1, 2
T25	INT/$\overline{INT}$ Valid Delay	1	23	
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	2 T1		1, 2, 3
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	6		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	5		2
T29	$\overline{PORT}$ Setup Time	10		2
T30	$\overline{PORT}$ Hold Time	5		2
T31	$\overline{BOFF}$ Setup Time	12		2
T32	$\overline{BOFF}$ Hold Time	4		2

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C–+85°C, V_{CC} = 5V ±10%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	25 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	25 MHz	1X CLK Input
T1	CLK Period	40	80	
T1a	CLK Period Stability		0.1%	Adjacent CLK Δ
T2	CLK High	14		2.0V
T3	CLK Low	14		0.8V
T4	CLK Rise Time		4	0.8V to 2.0V
T5	CLK Fall Time		4	2.0V to 0.8V
T6	$\overline{BE}n$ Valid Delay	3	17	
T6a	$\overline{BLAST}$ Valid Delay	3	20	
T6b	$\overline{LOCK}$ Valid Delay	3	18	
T6c	A2–A31 Valid Delay	3	18	
T6d	$\overline{PCHK}$ Valid Delay	3	24	
T7	$\overline{BE}n$, $\overline{LOCK}$, $\overline{BLAST}$, A2–A31 Float Delay	3	30	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	19	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	3	30	
T10	D0–D31, DPn Write Data Valid Delay	3	20	
T11	D0–D31, DPn Write Data Float Delay	3	30	
T12	HOLD Valid Delay	3	19	
T13	CA and BREQ Setup Time	7		1, 2
T14	CA and BREQ Hold Time	3		1, 2
T15	$\overline{BS16}$ Setup Time	8		2
T16	$\overline{BS16}$ Hold Time	3		2
T17	$\overline{BRDY}$ Setup Time	9		2
T17a	$\overline{RDY}$ Setup Time	8		2
T18	$\overline{BRDY}$, $\overline{RDY}$ Hold Time	3		2
T19	D0–D31, DPn READ Setup Time	6		2
T20	D0–D31, DPn READ Hold Time	4.5		2
T21	AHOLD and HLDA Setup Time	10		1, 2
T22	AHOLD Hold Time	3		1, 2
T22a	HLDA Hold Time	3		1, 2
T23	RESET Setup Time	10		1, 2
T24	RESET Hold Time	3		1, 2
T25	INT/$\overline{INT}$ Valid Delay	1	20	

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C–+85°C, V_{CC} = 5V ±10%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	25 MHz		Notes
		Min	Max	
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	2 T1		1, 2, 3
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	6		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	4.5		2
T29	$\overline{PORT}$ Setup Time	7		2
T30	$\overline{PORT}$ Hold Time	3		2
T31	$\overline{BOFF}$ Setup Time	10		2
T32	$\overline{BOFF}$ Hold Time	3		2

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

T_C = 0°C to +85°C, V_{CC} = 5V ±5%. These timing assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however timings must be derated. All timing requirements are given in nanoseconds.

Symbol	Parameter	33 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	33 MHz	1X CLK Input
T1	CLK Period	30	80	
T1a	CLK Period Stability		0.1%	Adjacent CLK Δ
T2	CLK High	11		2.0V
T3	CLK Low	11		0.8V
T4	CLK Rise Time		3	0.8V to 2.0V
T5	CLK Fall Time		3	2.0V to 0.8V
T6	$\overline{BEn}$ Valid Delay	3	17	
T6a	$\overline{BLAST}$ Valid Delay	3	20	
T6b	$\overline{LOCK}$ Valid Delay	3	16	
T6c	A2–A31 Valid Delay	3	18	
T6d	$\overline{PCHK}$ Valid Delay	3	23	
T7	$\overline{BEn}$, $\overline{LOCK}$, $\overline{BLAST}$, A2–A31 Float Delay	3	20	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	16	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	3	20	
T10	D0–D31, DPn Write Data Valid Delay	3	19	
T11	D0–D31, DPn Write Data Float Delay	3	20	
T12	HOLD Valid Delay	3	19	
T13	CA and BREQ Setup Time	7		1, 2
T14	CA and BREQ Hold Time	3		1, 2
T15	$\overline{BS16}$ Setup Time	7		2
T16	$\overline{BS16}$ Hold Time	3		2
T17	$\overline{BRDY}$ Setup Time	9		2
T17a	$\overline{RDY}$ Setup Time	8		2
T18	$\overline{BRDY}$, $\overline{RDY}$ Hold Time	3		2
T19	D0–D31, DPn READ Setup Time	6		2
T20	D0–D31, DPn READ Hold Time	4.5		2
T21	AHOLD Setup Time	10		1, 2
T21a	HLDA Setup Time	8		1, 2
T22	AHOLD Hold Time	3		1, 2

*Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

AC Characteristics (Continued)

82596CA C-STEP INPUT/OUTPUT SYSTEM TIMINGS

C_L on all outputs is 50 pF unless otherwise specified.
All timing requirements are given in nanoseconds.

Symbol	Parameter	33 MHz		Notes
		Min	Max	
T22a	HLDA Hold Time	3		1, 2
T23	RESET Setup Time	9		1, 2
T24	RESET Hold Time	3		1, 2
T25	INT/$\overline{INT}$ Valid Delay	1	20	
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	2T1		1, 2, 3
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	6		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	4.5		2
T29	$\overline{PORT}$ Setup Time	7		2
T30	$\overline{PORT}$ Hold Time	3		2
T31	$\overline{BOFF}$ Setup Time	10		2
T32	$\overline{BOFF}$ Hold Time	3		2

NOTES:
*Timings shown are for the 82596CA C-stepping. For information regarding timings for the 82596CA A1 or B-step, contact your local Intel representative.
1. RESET, HLDA, and CA are internally synchronized. This timing is to guarantee recognition at next clock for RESET, HLDA and CA.
2. All set-up, hold and delay timings are at maximum frequency specification Fmax, and must be derated according to the following equation for operation at lower frequencies:
   Tderated = (Fmax/Fopr) × T
   where:
   Tderate = Specifies the value to derate the specification.
   Fmax = Maximum operating frequency.
   Fopr = Actual operating frequency.
   T = Specification at maximum frequency.
   This calculation only provides a rough estimate for derating the frequency. For more detailed information, contact your Intel Sales Office for the data sheet supplement.
3. CA pulse width need only be 1 T1 wide if the set up and hold times are met; BREQ must meet setup and hold times and need only be 1 T1 wide.

TRANSMIT/RECEIVE CLOCK PARAMETERS

Symbol	Parameter	20 MHz		Notes
		Min	Max	
T36	$\overline{TxC}$ Cycle	50		1, 3
T38	$\overline{TxC}$ Rise Time		5	1
T39	$\overline{TxC}$ Fall Time		5	1
T40	$\overline{TxC}$ High Time	19		1, 3
T41	$\overline{TxC}$ Low Time	18		1, 3
T42	TxD Rise Time		10	4
T43	TxD Fall Time		10	4
T44	TxD Transition	20		2, 4
T45	$\overline{TxC}$ Low to TxD Valid		25	4, 6
T46	$\overline{TxC}$ Low to TxD Transition		25	2, 4
T47	$\overline{TxC}$ High to TxD Transition		25	2, 4
T48	$\overline{TxC}$ Low to TxD High (At End of Transition)		25	4

TRANSMIT/RECEIVE CLOCK PARAMETERS (Continued)

Symbol	Parameter	20 MHz		Notes
		Min	Max	
$\overline{\text{RTS}}$ AND $\overline{\text{CTS}}$ PARAMETERS				
T49	$\overline{\text{TxC}}$ Low to $\overline{\text{RTS}}$ Low, Time to Activate $\overline{\text{RTS}}$		25	5
T50	$\overline{\text{CTS}}$ Low to $\overline{\text{TxC}}$ Low, $\overline{\text{CTS}}$ Setup Time		20	
T51	$\overline{\text{TxC}}$ Low to $\overline{\text{CTS}}$ Invalid, $\overline{\text{CTS}}$ Hold Time	10		7
T52	$\overline{\text{TxC}}$ Low to $\overline{\text{RTS}}$ High		25	5
RECEIVE CLOCK PARAMETERS				
T53	$\overline{\text{RXC}}$ Cycle	50		1, 3
T54	$\overline{\text{RXC}}$ Rise Time		5	1
T55	$\overline{\text{RXC}}$ Fall Time		5	1
T56	$\overline{\text{RXC}}$ High Time	19		1
T57	$\overline{\text{RXC}}$ Low Time	18		1
RECEIVED DATA PARAMETERS				
T58	RXD Setup Time	20		6
T59	RXD Hold Time	10		6
T60	RXD Rise Time		10	
T61	RXD Fall Time		10	
$\overline{\text{CRS}}$ AND $\overline{\text{CDT}}$ PARAMETERS				
T62	$\overline{\text{CDT}}$ Low to $\overline{\text{TXC}}$ HIGH External Collision Detect Setup Time	20		
T63	$\overline{\text{TXC}}$ High to $\overline{\text{CDT}}$ Inactive, $\overline{\text{CDT}}$ Hold Time	10		
T64	$\overline{\text{CDT}}$ Low to Jam Start			10
T65	$\overline{\text{CRS}}$ Low to $\overline{\text{TXC}}$ High, Carrier Sense Setup Time	20		
T66	$\overline{\text{TXC}}$ High to $\overline{\text{CRS}}$ Inactive, $\overline{\text{CRS}}$ Hold Time (Internal Collision Detect)	10		
T67	$\overline{\text{CRS}}$ High to Jamming Start,			12
T68	Jamming Period			11
T69	$\overline{\text{CRS}}$ High to $\overline{\text{RXC}}$ High, $\overline{\text{CRS}}$ Inactive Setup Time	30		
T70	$\overline{\text{RXC}}$ High to $\overline{\text{CRS}}$ High, $\overline{\text{CRS}}$ Inactive Hold Time	10		

TRANSMIT/RECEIVE CLOCK PARAMETERS (Continued)

Symbol	Parameter	20 MHz		Notes
		Min	Max	
INTERFRAME SPACING PARAMETERS				
T71	Interframe Delay			9
EXTERNAL LOOPBACK-PIN PARAMETERS				
T72	$\overline{TXC}$ Low to $\overline{LPBK}$ Low		T36	4
T73	$\overline{TXC}$ Low to $\overline{LPBK}$ High		T36	4

NOTES:
1. Special MOS levels. V_{CIL} = 0.9V and V_{CIH} = 3.0V.
2. Manchester only.
3. Manchester. Needs 50% duty cycle.
4. 1 TTL load + 50 pF.
5. 1 TTL load + 100 pF.
6. NRZ only.
7. Abnormal end of transmission—CTS expires before RTS.
8. Normal end to transmission.
9. Programmable value:
   T71 = N_{IFS} • T36
   where: N_{IFS} = the IFS configuration value
   (if N_{IFS} is less than 12 then N_{IFS} is forced to 12).
10. Programmable value:
    T64 = (N_{CDF} • T36) + x • T36
    (If the collision occurs after the preamble)
    where:
    N_{CDF} = the collision detect filter configuration value,
    and
    x = 12, 13, 14, or 15
11. T68 = 32 • T36
12. Programmable value:
    T67 = (N_{CSF} • T36) + x • T36
    where: N_{CSF} = the Carrier Sense Filter configuration value, and
    x = 12, 13, 14, or 15
13. To guarantee recognition on the next clock.

82596CA BUS OPERATION

The following figures show the 82596CA basic bus cycle and basic burst cycle.

Please refer to the *32-Bit LAN Component User's Manual.*

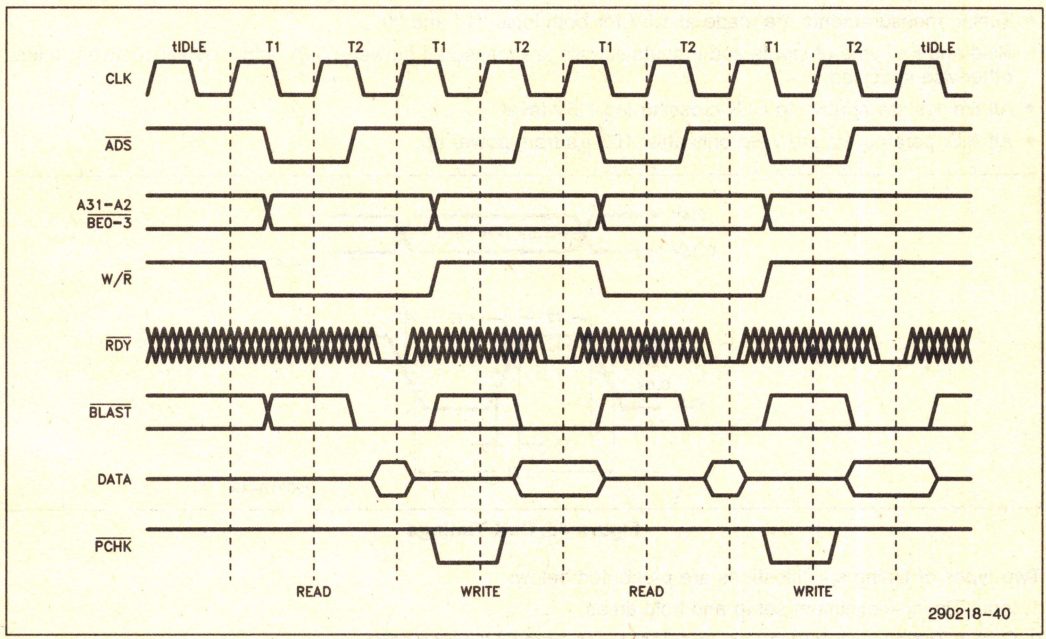


Figure 44. Basic 82596CA Bus Cycle

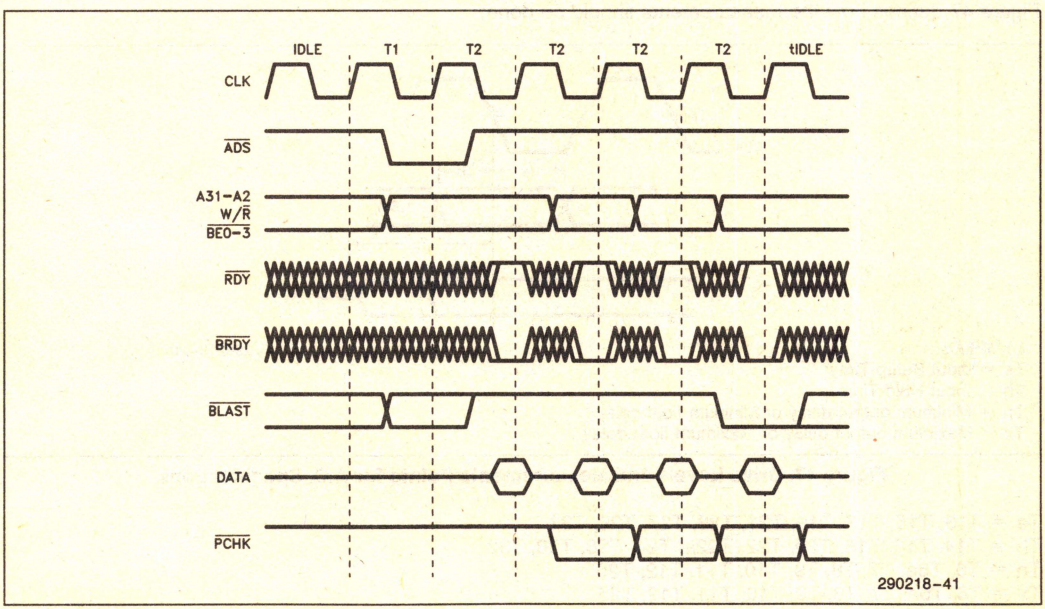


Figure 45. Basic 82596CA Burst Cycle

SYSTEM INTERFACE A.C. TIMING CHARACTERISTICS

The measurements should be done at:

- T_C = 0°C to +85°C, V_{CC} = 5V ±10%, C = 50 pF unless otherwise specified.
- A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
- Timing measurements are made at 1.5V for both logic "1" and "0".
- Rise and Fall time of inputs and outputs signals are measured between 0.8V and 2.0V respectively unless otherwise specified.
- All timings are relative to CLK crossing the 1.5V level.
- All A.C. parameters are valid only after 100 μs from power up.

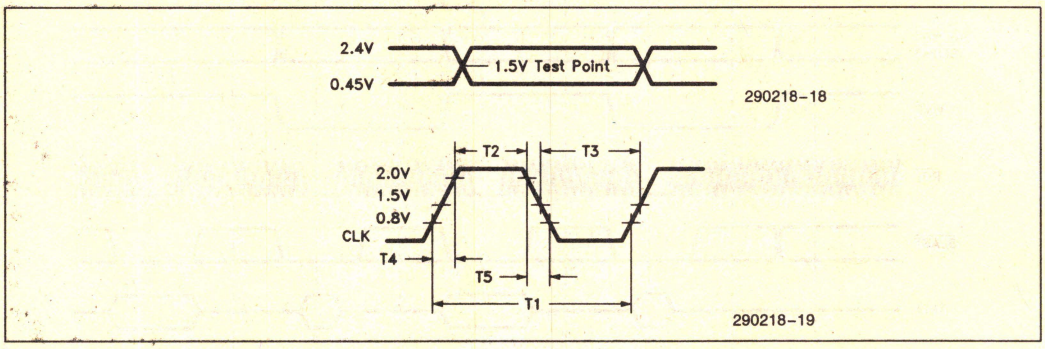


Figure 46. CLK Timings

Two types of timing specifications are presented below:

1. Input Timing—minimum setup and hold times.
2. Output Timings—output delays and float times from CLK rising edge.

Figure 47 defines how the measurements should be done:

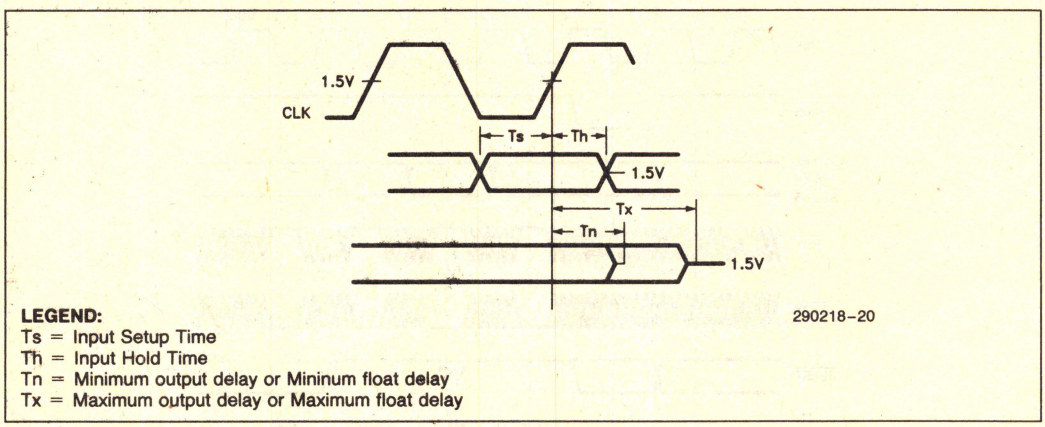


Figure 47. Drive Levels and Measurements Points for A.C. Specifications

Ts = T13, T15, T17, T19, T21, T23, T27, T29, T31
Th = T14, T16, T18, T20, T22, T22a, T24, T28, T30, T32
Tn = T6, T6a, T7, T8, T9, T10, T11, T12, T25
Tx = T6, T6a, T7, T8, T9, T10, T11, T12, T25

INPUT WAVEFORMS

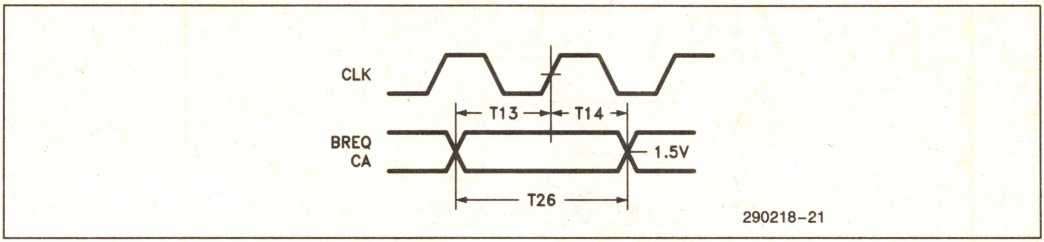


Figure 48. CA and BREQ Input Timing

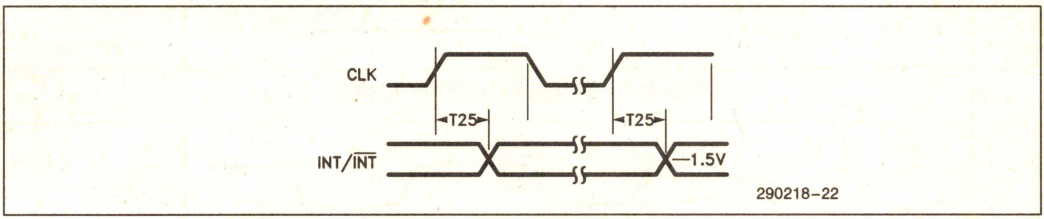


Figure 49. INT/INT Output Timing

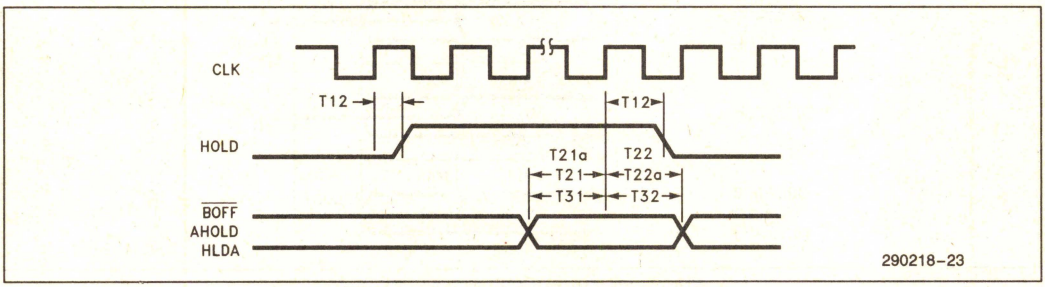


Figure 50. HOLD/HLDA Timings

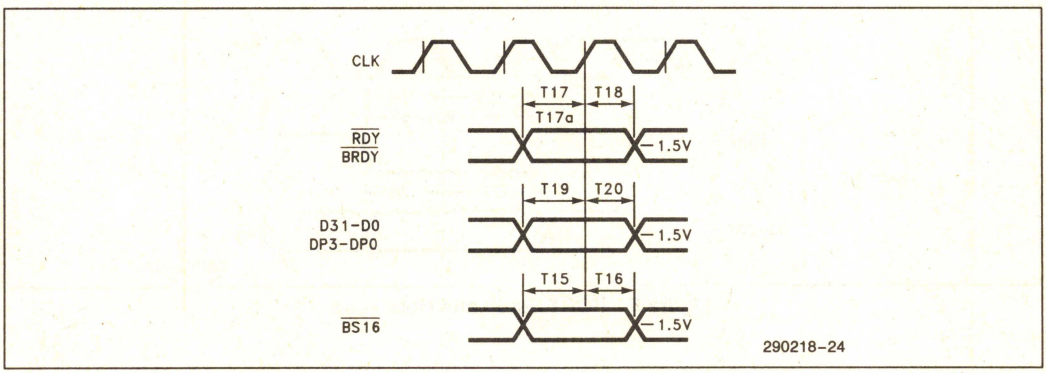


Figure 51. Input Setup and Hold Time

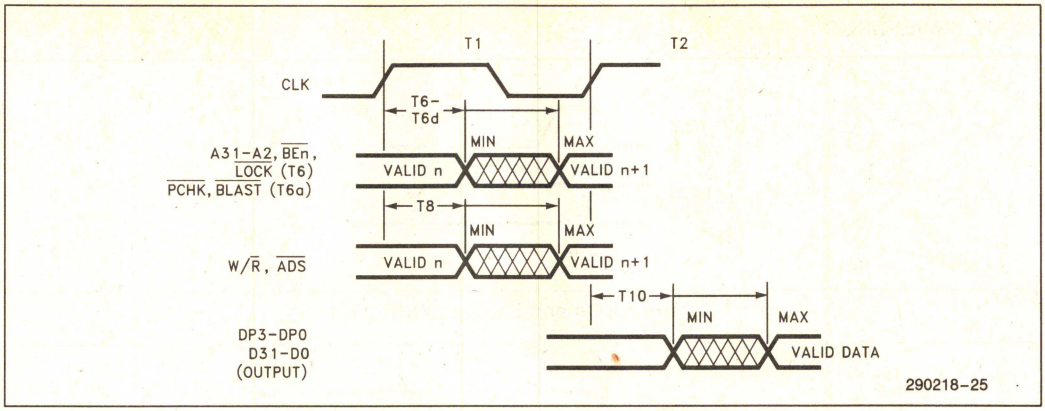


Figure 52. Output Valid Delay Timing

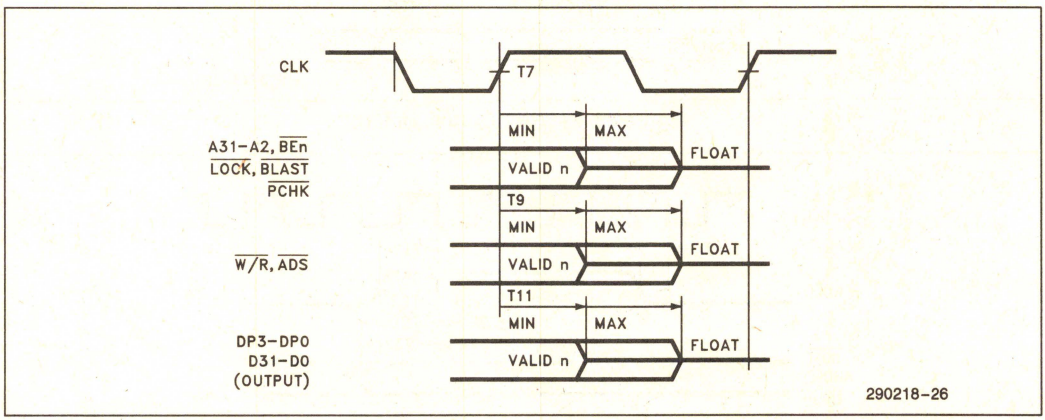


Figure 53. Output Float Delay Timing

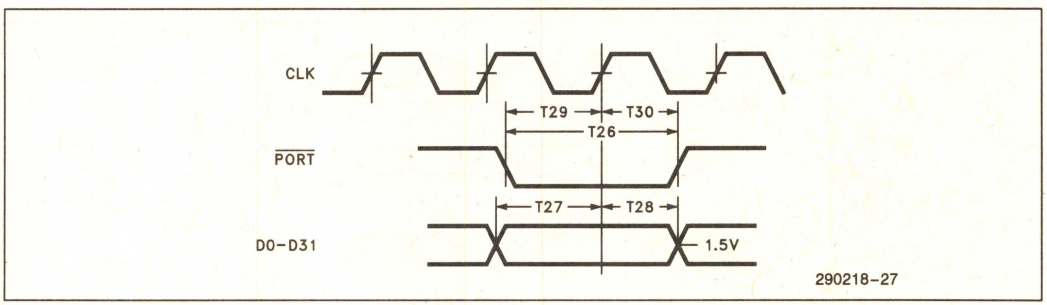


Figure 54. PORT Setup and Hold Time

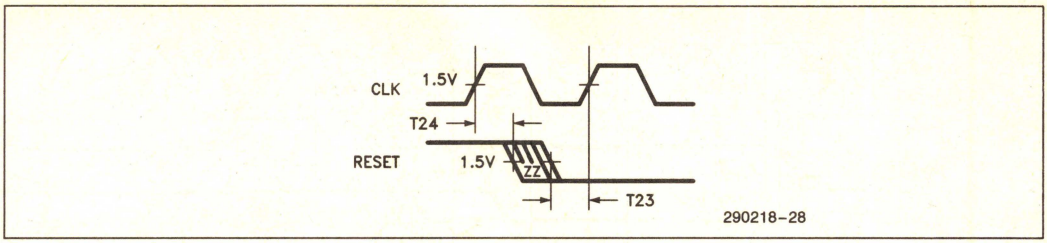


Figure 55. RESET Input Timing

SERIAL AC TIMING CHARACTERISTICS

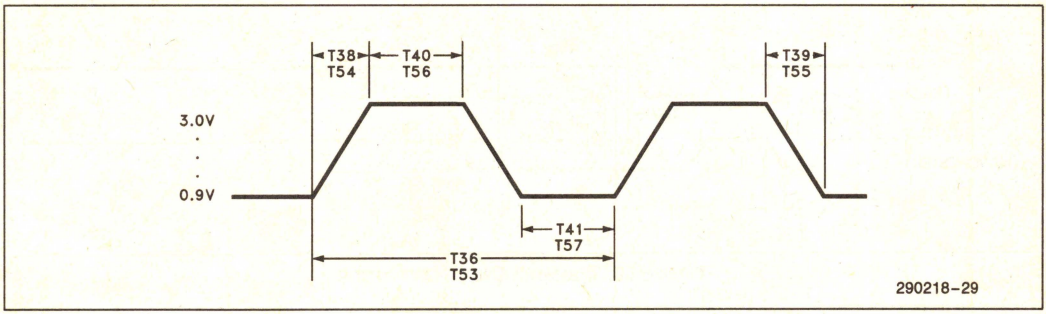


Figure 56. Serial Input Clock Timing

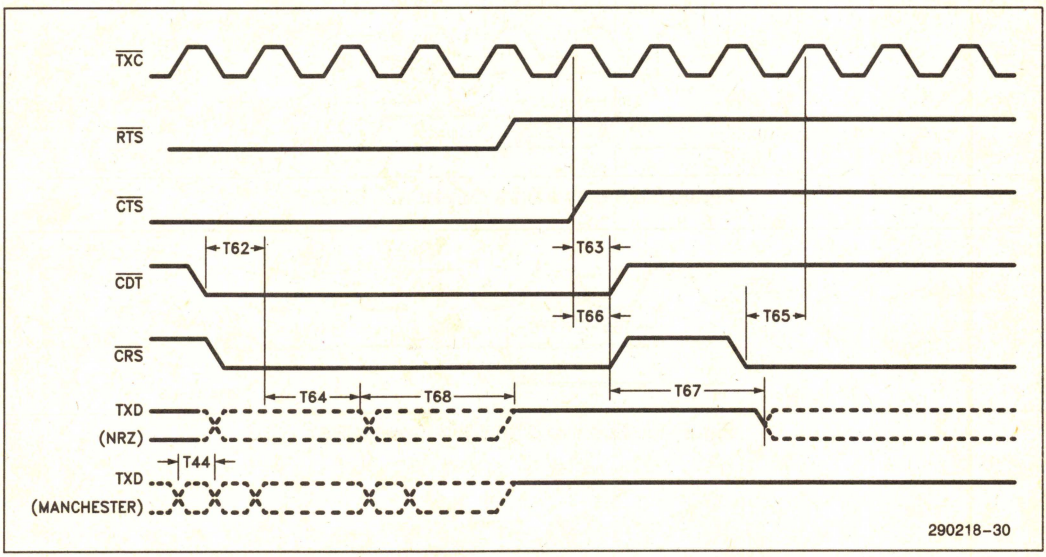


Figure 57. Transmit Data Waveforms

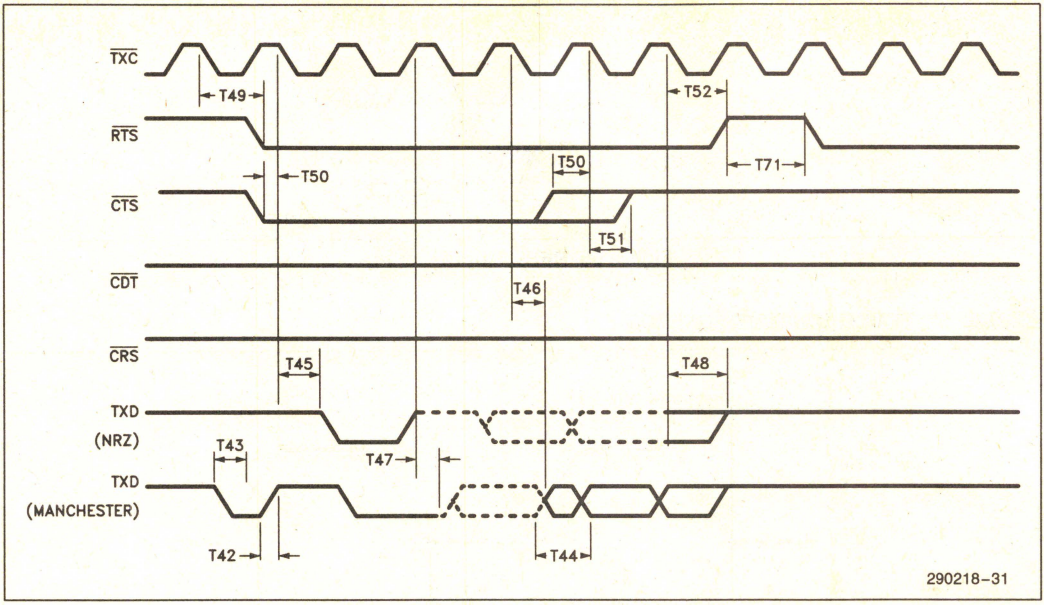


Figure 58. Transmit Data Waveforms

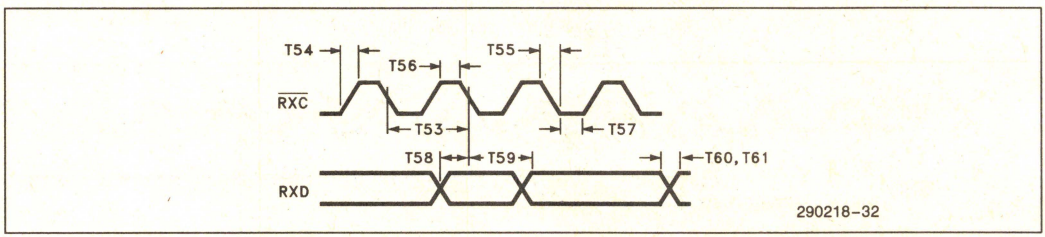


Figure 59. Receive Data Waveforms (NRZ)

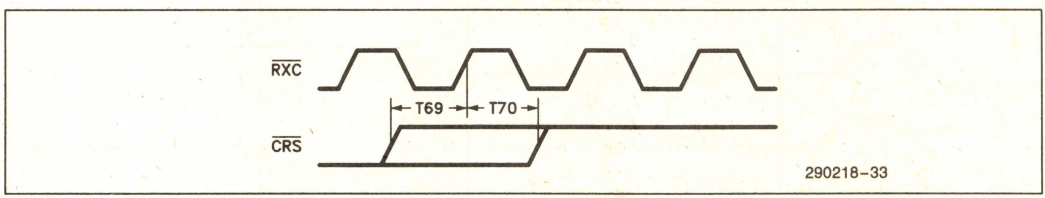
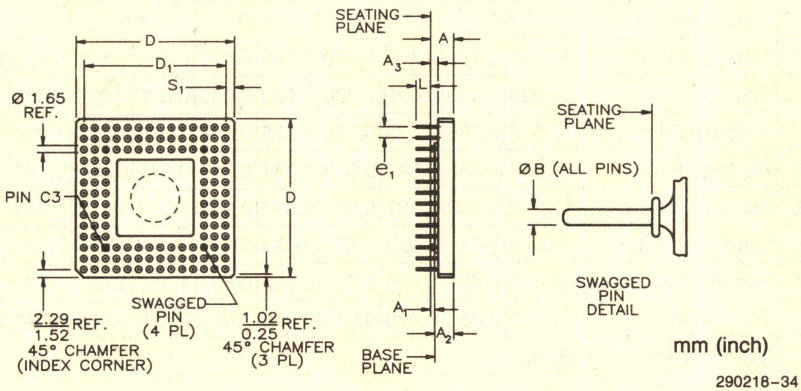


Figure 60. Receive Data Waveforms (CRS)

OUTLINE DIAGRAMS

132 LEAD CERAMIC PIN GRID ARRAY PACKAGE INTEL TYPE A



Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A_2	2.67	3.43	Solid Lid	0.105	0.135	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	36.45	37.21		1.435	1.465	
D_1	32.89	33.15		1.295	1.305	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	132			132		
S_1	1.27	2.54		0.050	0.100	
ISSUE	IWS 10/12/88					

intel

Intel Case Outline Drawings
Plastic Quad Flat Pack (PQFP)
0.025 Inch (0.635mm) Pitch

Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170
A1	Standoff	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
D, E	Terminal Dimension	0.675	0.685	0.775	0.785	0.875	0.885	1.075	1.085	1.275	1.285	1.475	1.485
D1, E1	Package Body	0.547	0.553	0.647	0.653	0.747	0.753	0.947	0.953	1.147	1.153	1.347	1.353
D2, E2	Bumper Distance	0.697	0.703	0.797	0.803	0.897	0.903	1.097	1.103	1.297	1.303	1.497	1.503
D3, E3	Lead Dimension	0.400 REF		0.500 REF		0.600 REF		0.800 REF		1.000 REF		1.200 REF	
D4, E4	Foot Radius Location	0.623	0.637	0.723	0.737	0.823	0.837	1.023	1.037	1.223	1.237	1.423	1.437
L1	Foot Length	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
Issue	IWS Preliminary 12/12/88												INCH

Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32
A1	Standoff	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
D, E	Terminal Dimension	17.15	17.40	19.69	19.94	22.23	22.48	27.31	27.56	32.39	32.64	37.47	37.72
D1, E1	Package Body	13.89	14.05	16.43	16.59	18.97	19.13	24.05	24.21	29.13	29.29	34.21	34.37
D2, E2	Bumper Distance	17.70	17.85	20.24	20.39	22.78	22.93	27.86	28.01	32.94	33.09	38.02	38.18
D3, E3	Lead Dimension	10.16 REF		12.70 REF		15.24 REF		20.32 REF		25.40 REF		30.48 REF	
D4, E4	Foot Radius Location	15.82	16.17	18.36	18.71	21.25	21.25	25.89	26.33	31.06	31.41	36.14	36.49
L1	Foot Length	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
Issue	IWS Preliminary 12/12/88												mm

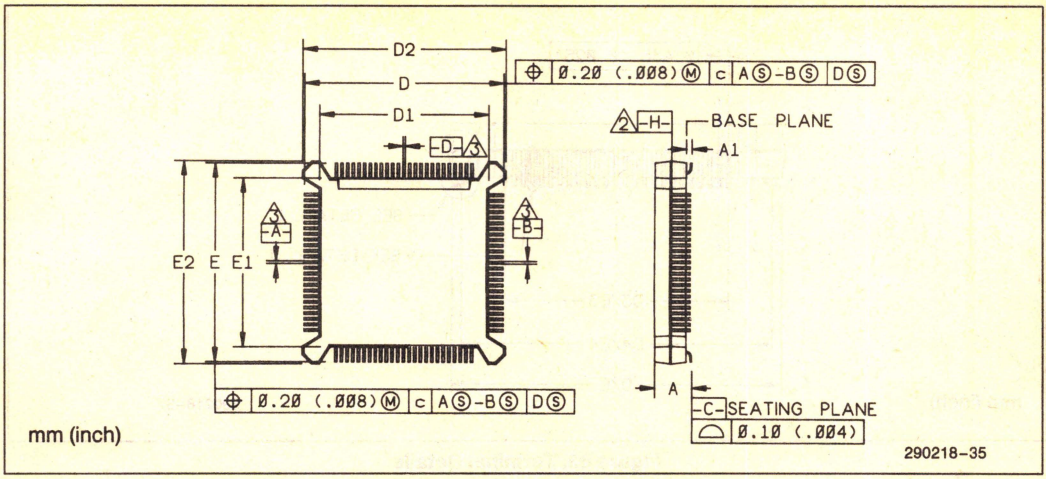


Figure 61. Principal Dimensions and Datums

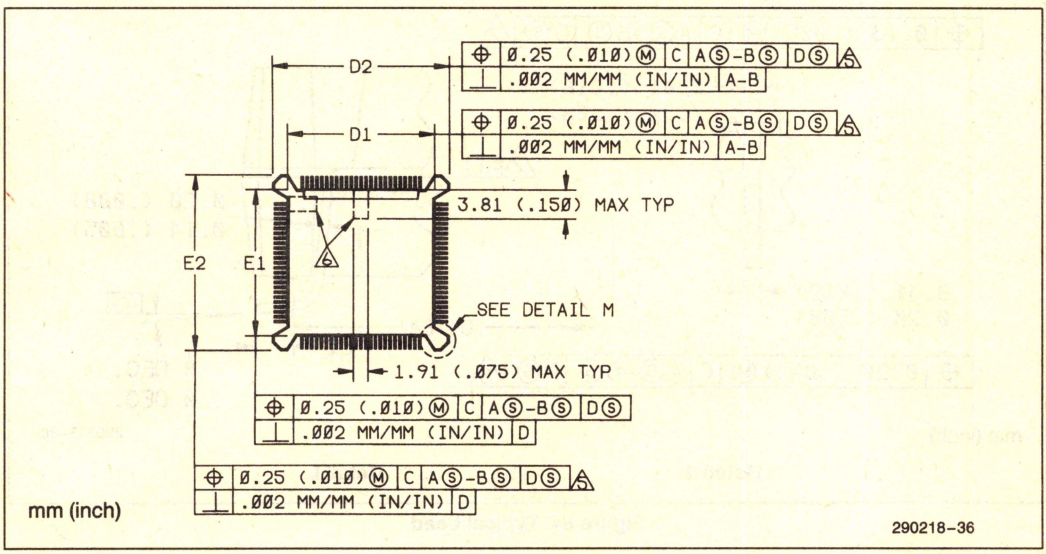


Figure 62. Molded Details

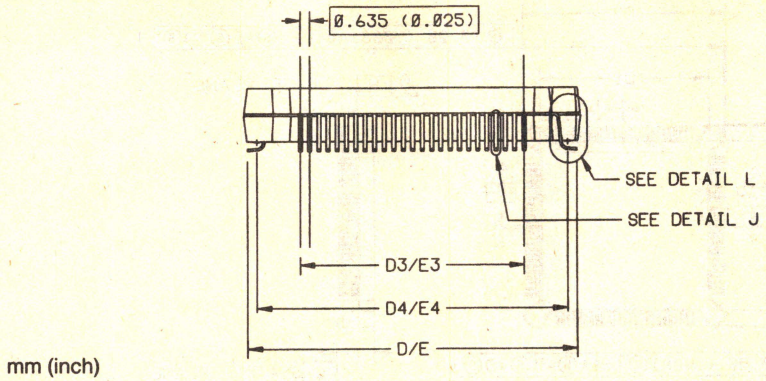


Figure 63. Terminal Details

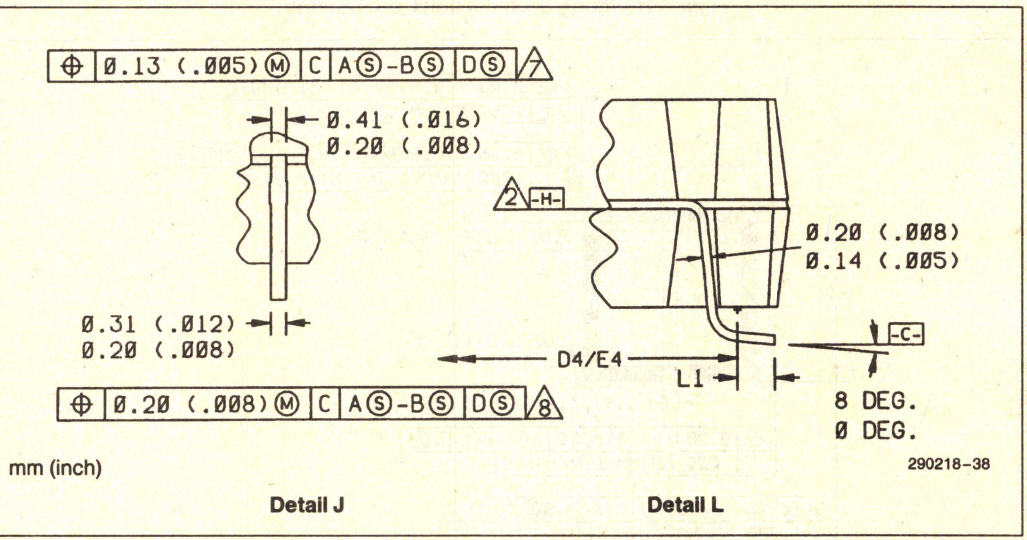
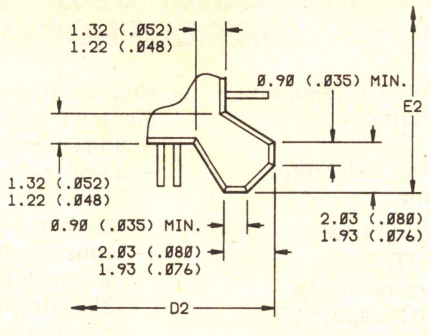


Figure 64. Typical Lead



mm (inch)

Figure 65. Detail M

REVISION SUMMARY

The following represents the key differences between version 004 and version 005 of the 82596CA Data Sheet.

1. Timings added for -16 MHz and -20 MHz specfications.

The following represents the key differences between version 005 and version 006 of the 82596CA Data Sheet.

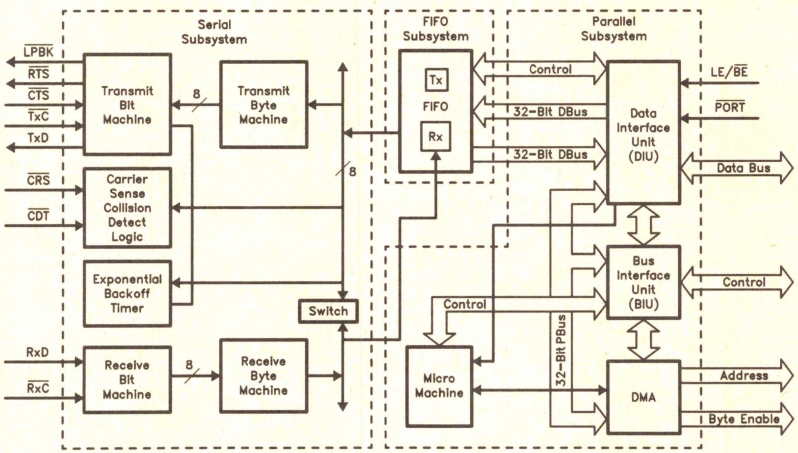
1. A description of the 82596CA C-stepping enhancements was added and the 82596CA B-step information was removed.
2. Description of BOFF pin changed. BOFF may be asserted in T1 in the 82596 C-step.
3. Recommendation to use only one type of buffer (either Simplified or Flexible) in any given linked list.
4. Added detailed description regarding operation or RCVCDT counter.
5. Added New Enhanced Big Endian Mode section. The New Enhanced Big Endian Mode applies only to the 82596 C-stepping.
6. Added programming recommendations regarding RU and CU Start commands. These warn against Starting the CU while it is Active and Starting the RU while it is Ready.
7. Emphasized that the TDR command is a static command and should not be used in an active network.
8. Improved 82596CA C-step timings were added for all speeds.

82596DX AND 82596SX HIGH-PERFORMANCE 32-BIT LOCAL AREA NETWORK COPROCESSOR

- **Performs Complete CSMA/CD Medium Access Control (MAC) Functions—Independently of CPU**
  - **— IEEE 802.3 (EOC) Frame Delimiting**
  - **— HDLC Frame Delimiting**
- **Supports Industry Standard LANs**
  - **— IEEE TYPE 10BASE-T (TPE), IEEE TYPE 10BASE5 (Ethernet*), IEEE TYPE 10BASE2 (Cheapernet), IEEE TYPE 1BASE5 (StarLAN), and the Proposed Standard TYPE 10BASE-F**
  - **— Proprietary CSMA/CD Networks Up to 20 Mb/s**
- **On-Chip Memory Management**
  - **— Automatic Buffer Chaining**
  - **— Buffer Reclamation after Receipt of Bad Frames; Optional Save Bad Frames**
  - **— 32-Bit Segmented or Linear (Flat) Memory Addressing Formats**
- **82586 Software Compatible**
- **Optimized CPU Interface**
  - **— 82596DX Bus Interface Optimized to Intel's 32-Bit i386™DX**
  - **— 82596SX Bus Interface Optimized to Intel's 16-Bit i386™SX**
  - **— Supports Big Endian and Little Endian Byte Ordering**
- **High-Performance 16-/32-Bit Bus Master Interface**
  - **— 66-MB/s Bus Bandwidth**
  - **— 33-MHz Clock, Two Clocks Per Transfer**
  - **— Bus Throttle Timers**
  - **— Transfers Data at 100% of Serial Bandwidth**
  - **— 128-Byte Receive FIFO, 64-Byte Transmit FIFO**
- **Network Management and Diagnostics**
  - **— Monitor Mode**
  - **— 32-Bit Statistical Counters**
- **Self-Test Diagnostics**
- **Configurable Initialization Root for Data Structures**
- **High-Speed, 5-V, CHMOS** IV Technology**
- **132-Pin Plastic Quad Flat Pack (PQFP) and PGA Package**

  (See Packaging Specifications Order Number: 240800-001, Package Type KU and A)

i386™ is a trademark of Intel Corporation
*Ethernet is a registered trademark of Xerox Corporation.
**CHMOS is a patented process of Intel Corporation.



290219-1

Figure 1. 82596DX/SX Block Diagram

October 1993
Order Number: 290219-006

82596DX and 82596SX High-Performance 32-Bit Local Area Network Coprocessor

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INTRODUCTION

The 82596DX/SX is an intelligent, high-performance 32-bit Local Area Network coprocessor. The 82596DX/SX implements the CSMA/CD access method and can be configured to support all existing IEEE 802.3 standards—TYPEs 10BASE-T, 10BASE5, 10BASE2, 1BASE5, and 10BROAD36. It can also be used to implement the proposed standard TYPE 10BASE-F. The 82596DX/SX performs high-level commands, command chaining, and interprocessor communications via shared memory, thus relieving the host CPU of many tasks associated with network control. All time-critical functions are performed independently of the CPU, this increases network performance and efficiency. The 82596DX/SX bus interface is optimized for Intel's i386™ DX and i386™ SX microprocessors.

The 82596DX/SX implements all IEEE 802.3 Medium Access Control and channel interface functions, these include framing, preamble generation and stripping, source address generation, destination address checking, short-frame detection, and automatic length-field handling. Data rates up to 20 Mb/s are supported.

The 82596DX/SX provides a powerful host system interface. It manages memory structures automatically, with command chaining and bidirectional data chaining. An on-chip DMA controller manages four channels, this allows autonomous transfer of data blocks (buffers and frames) and relieves the CPU of byte transfer overhead. Buffers containing errored or collided frames can be automatically recovered without CPU intervention. The 82596DX/SX provides an upgrade path for existing 82586 software drivers by providing an 82586-software-compatible mode that supports the current 82586 memory structure. The 82596DX/SX also has a Flexible memory structure and a Simplified memory structure. The 82596DX/SX can address up to 4 gigabytes of memory. The 82596DX/SX supports Little Endian and Big Endian byte ordering.

The 82596DX/SX bus interface is optimized to Intel's i386™ DX and i386 SX microprocessors, providing a bus transfer rate of up to 66 MB/s at 33 MHz. The bus interface employs bus throttle timers to regulate 82596DX/SX bus use. Two large, independent FIFOs—128 bytes for Receive and 64 bytes for Transmit—tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case bus latency.

The 82596DX/SX provides a wide range of diagnostics and network management functions, these include internal and external loopback, exception condition tallies, channel activity indicators, optional capture of all frames regardless of destination address (promiscuous mode), optional capture of errored or collided frames, and time domain reflectometry for locating fault points on the network cable. The statistical counters, in 32-bit segmented and linear modes, are 32-bits each and include CRC errors, alignment errors, overrun errors, resource errors, short frames, and received collisions. The 82596DX/SX also features a monitor mode for network analysis. In this mode the 82596DX/SX can capture status bytes, and update statistical counters, of frames monitored on the link without transferring the contents of the frames to memory. This can be done concurrently while transmitting and receiving frames destined for that station.

The 82596DX/SX can be used in both baseband and broadband networks. It can be configured for maximum network efficiency (minimum contention overhead) with networks of any length. Its highly flexible CSMA/CD unit supports address field lengths of zero through six bytes—configurable to either IEEE 802.3/Ethernet or HDLC frame delimitation. It also supports 16- or 32-bit cyclic redundancy checks. The CRC can be transferred directly to memory for receive, operations or dynamically inserted for transmit operations. The CSMA/CD unit can also be configured for full duplex operation for high throughput in point-to-point connections.

The 82596 C-Step incorporates several new features not found in previous steppings. The following is a summary of the 82596 C-step's new features.

- The 82596 C-step fixes Errata found in the A1 and B steppings.
- The 82596 C-step has improved AC timings over both the A and B steppings.
- The 82596 C-step has a New Enhanced Big Endian Mode where in Linear Addressing mode, true 32-bit Big Endian functionality is achieved. New Enhanced Big Endian Mode is enabled by setting bit 7 of the SYSBUS byte. This mode is software compatible with the big endian mode of the B-step with one exception—no 32-bit addresses need to be swapped by software in the C-step. In this new mode, the 82596 C-step treats 32-bit address pointers as true 32-bit entities and the SCB absolute address and statistical counters are still treated as two 16-bit big endian entities. Not setting this mode will configure the 82596 C-step to be 100% compatible to the A1-step bit endian mode.
- The 82596 C-step is hardware and software compatible to both the A1 and B steppings allowing for easy "drop-in" to current designs. Pinout and control structures remain unchanged.

The 82596DX/SX is fabricated with Intel's reliable, 5-V, CHMOS IV (Process 648.8) technology. It is available in a 132-pin PQFP or PGA package.

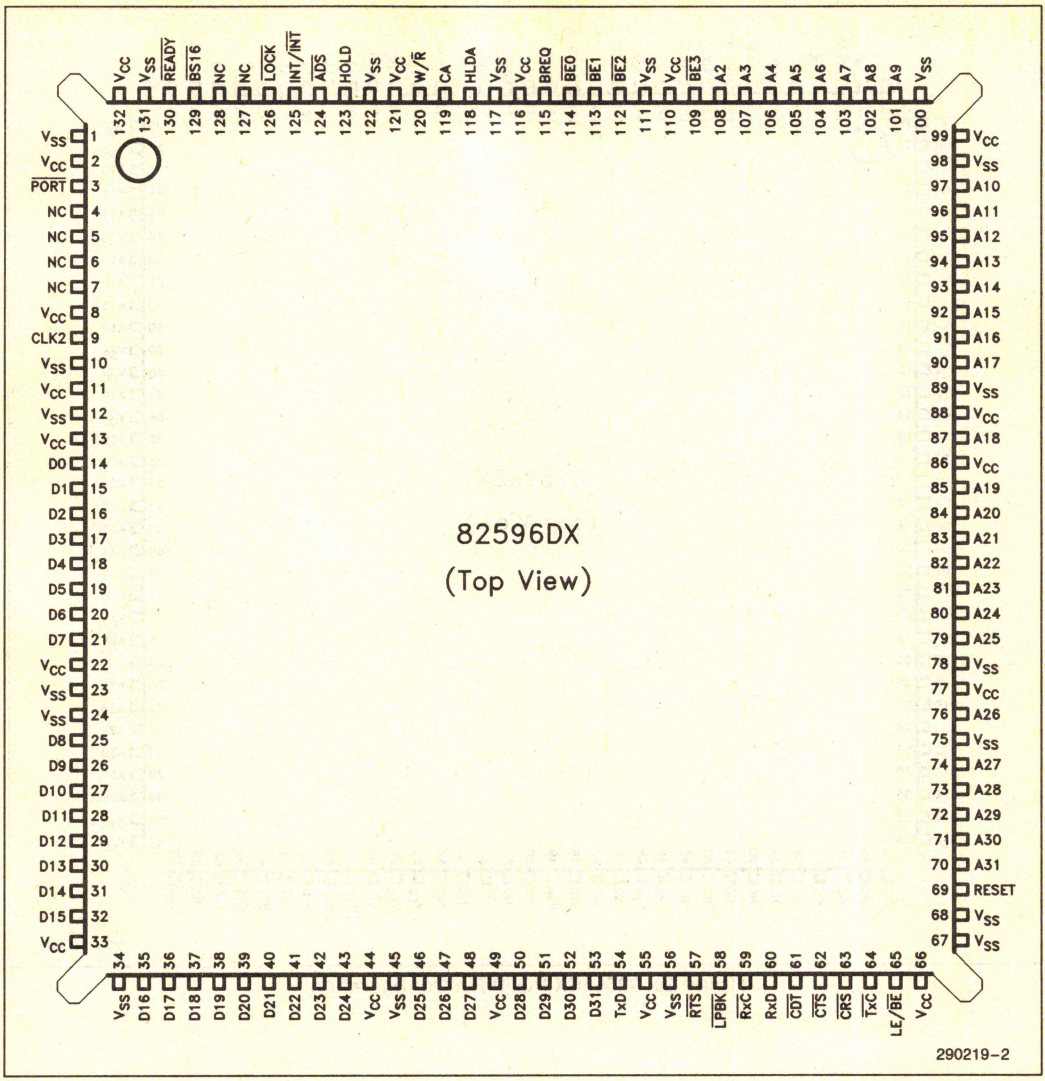


Figure 2a. 82596DX PQFP Pin Configuration

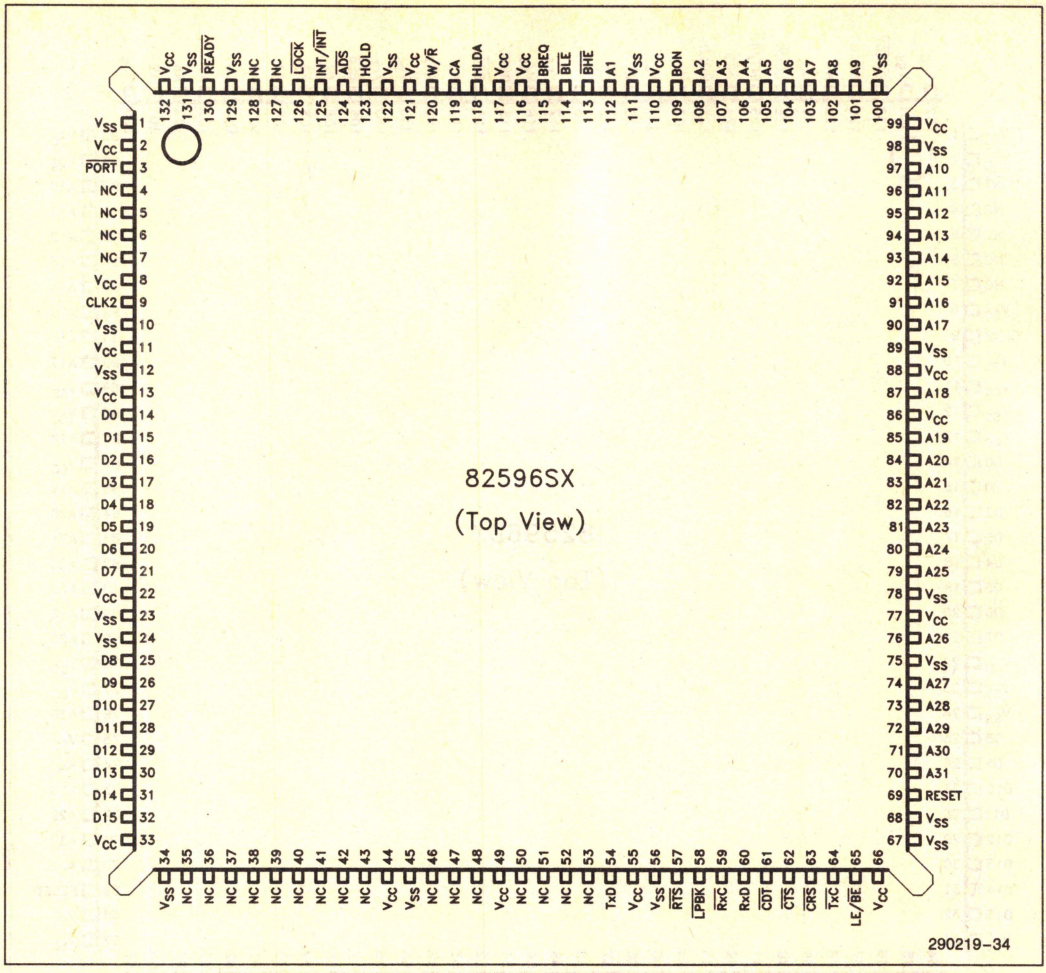


Figure 2b. 82596SX PQFP Pin Configuration

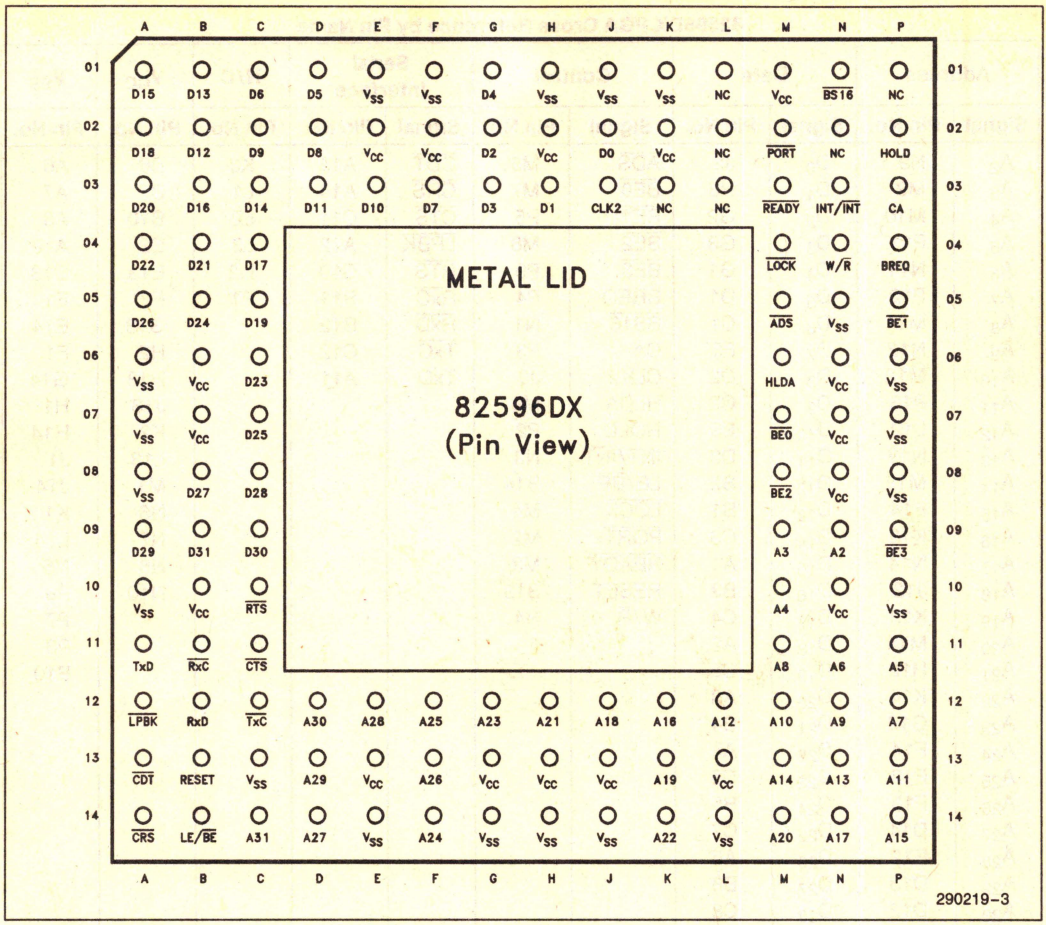


Figure 3a. 82596DX PGA Pin View Side

82596DX PGA Cross Reference by Pin Name

Address		Data		Control		Serial Interface		N/C	V_{CC}	V_{SS}
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Pin No.	Pin No.	Pin No.
A_2	N9	D_0	J2	$\overline{ADS}$	M5	$\overline{CDT}$	A13	K3	B6	A6
A_3	M9	D_1	H3	$\overline{BE0}$	M7	$\overline{CRS}$	A14	L1	B7	A7
A_4	M10	D_2	G2	$\overline{BE1}$	P5	$\overline{CTS}$	C11	L2	B10	A8
A_5	P11	D_3	G3	$\overline{BE2}$	M8	$\overline{LPBK}$	A12	L3	E2	A10
A_6	N11	D_4	G1	$\overline{BE3}$	P9	$\overline{RTS}$	C10	N2	E13	C13
A_7	P12	D_5	D1	BREQ	P4	$\overline{RxC}$	B11	P1	F2	E1
A_8	M11	D_6	C1	$\overline{BS16}$	N1	$\overline{RxD}$	B12		G13	E14
A_9	N12	D_7	F3	CA	P3	$\overline{TxC}$	C12		H2	F1
A_{10}	M12	D_8	D2	CLK2	J3	TxD	A11		H13	G14
A_{11}	P13	D_9	C2	HLDA	M6				J13	H1
A_{12}	L12	D_{10}	E3	HOLD	P2				K2	H14
A_{13}	N13	D_{11}	D3	INT/$\overline{INT}$	N3				L13	J1
A_{14}	M13	D_{12}	B2	LE/$\overline{BE}$	B14				M1	J14
A_{15}	P14	D_{13}	B1	$\overline{LOCK}$	M4				N6	K1
A_{16}	K12	D_{14}	C3	$\overline{PORT}$	M2				N7	L14
A_{17}	N14	D_{15}	A1	$\overline{READY}$	M3				N8	N5
A_{18}	J12	D_{16}	B3	RESET	B13				N10	P6
A_{19}	K13	D_{17}	C4	W/$\overline{R}$	N4					P7
A_{20}	M14	D_{18}	A2							P8
A_{21}	H12	D_{19}	C5							P10
A_{22}	K14	D_{20}	A3							
A_{23}	G12	D_{21}	B4							
A_{24}	F14	D_{22}	A4							
A_{25}	F12	D_{23}	C6							
A_{26}	F13	D_{24}	B5							
A_{27}	D14	D_{25}	C7							
A_{28}	E12	D_{26}	A5							
A_{29}	D13	D_{27}	B8							
A_{30}	D12	D_{28}	C8							
A_{31}	C14	D_{29}	A9							
		D_{30}	C9							
		D_{31}	B9							

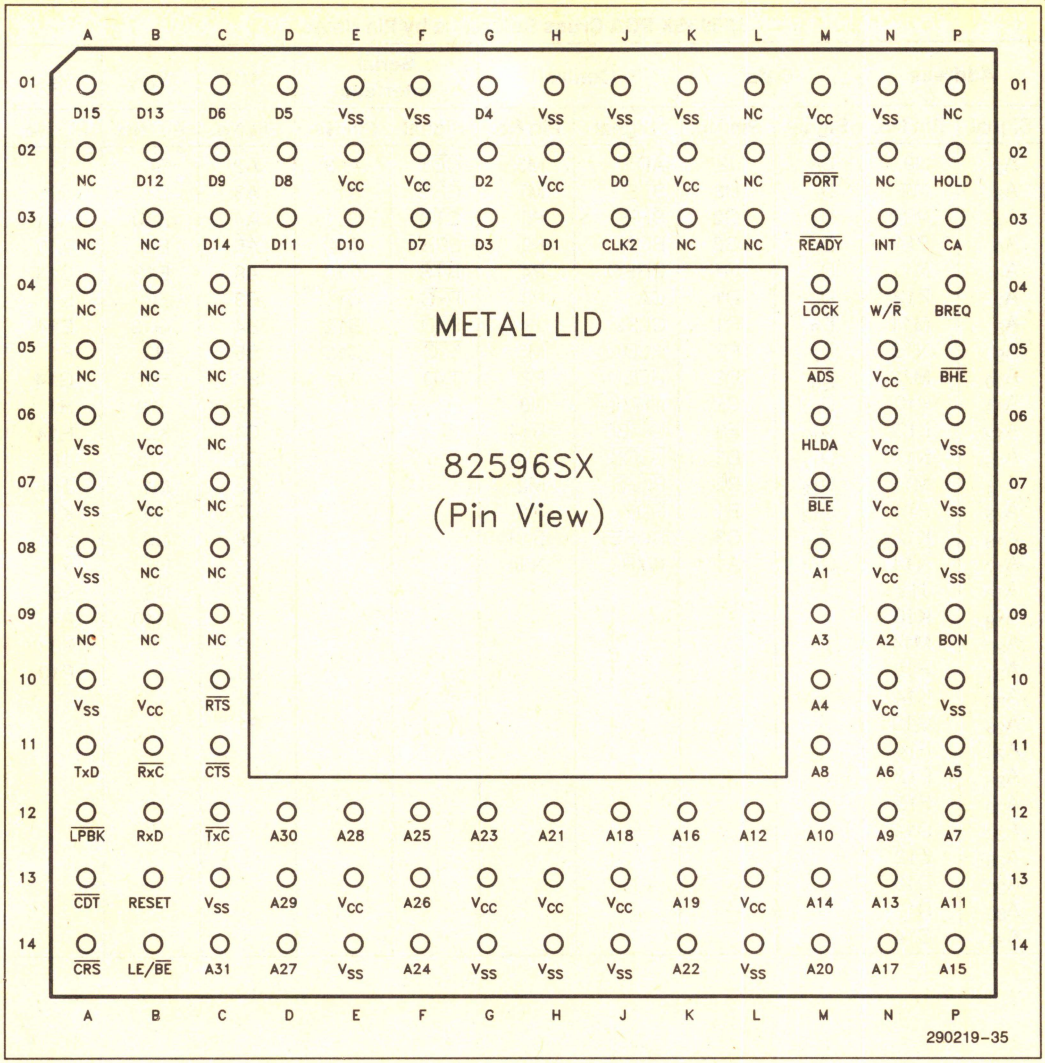


Figure 3b. 82596SX PGA Pin View Side

82596SX PGA Cross Reference by Pin Name

Address		Data		Control		Serial Interface		N/C	V_{CC}	V_{SS}
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Pin No.	Pin No.	Pin No.
A_2	N9	D_0	J2	$\overline{ADS}$	M5	$\overline{CDT}$	A13	A2	B6	A6
A_3	M9	D_1	H3	$\overline{BLE}$	M7	$\overline{CRS}$	A14	A3	B7	A7
A_4	M10	D_2	G2	$\overline{BHE}$	P5	$\overline{CTS}$	C11	A4	B10	A8
A_5	P11	D_3	G3	BON	P9	$\overline{LPBK}$	A12	A5	E2	A10
A_6	N11	D_4	G1	BREQ	P4	$\overline{RTS}$	C10	A9	E13	C13
A_7	P12	D_5	D1	CA	P3	$\overline{RxC}$	B11	B3	F2	E1
A_8	M11	D_6	C1	CLK2	J3	$\overline{RxD}$	B12	B4	G13	E14
A_9	N12	D_7	F3	HLDA	M6	$\overline{TxC}$	C12	B5	H2	F1
A_{10}	M12	D_8	D2	HOLD	P2	TxD	A11	B8	H13	G14
A_{11}	P13	D_9	C2	INT/$\overline{INT}$	N3			B9	J13	H1
A_{12}	L12	D_{10}	E3	LE/$\overline{BE}$	B14			C4	K2	H14
A_{13}	N13	D_{11}	D3	$\overline{LOCK}$	M4			C5	L13	J1
A_{14}	M13	D_{12}	B2	$\overline{PORT}$	M2			C6	M1	J14
A_{15}	P14	D_{13}	B1	$\overline{RDY}$	M3			C7	N5	K1
A_{16}	K12	D_{14}	C3	RESET	B13			C8	N6	L14
A_{17}	N14	D_{15}	A1	W/$\overline{R}$	N04			C9	N7	N1
A_{18}	J12							K3	N8	P6
A_{19}	K13							L1	N10	P7
A_{20}	M14							L2		P8
A_{21}	H12							L3		P10
A_{22}	K14							N2		
A_{23}	G12							P1		
A_{24}	F14									
A_{25}	F12									
A_{26}	F13									
A_{27}	D14									
A_{28}	E12									
A_{29}	D13									
A_{30}	D12									
A_{31}	C14									

PIN DESCRIPTIONS

<table>
<tr><th>Symbol</th><th>PQFP Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>CLK2</td><td>9</td><td>I</td><td>CLOCK. The system clock input provides the fundamental timing for the 82596. It is internally divided by two to generate the 82596 clock. All external timing parameters are specified in reference to the rising edge of CLK2. For clock levels see D.C. Characteristics.</td></tr>
<tr><td>D31–D0</td><td>14–53</td><td>I/O</td><td>DATA BUS. The 32 Data Bus lines are bidirectional, tri-state lines that provide the general purpose data path between the 82596 and memory. With the 82596DX the bus can be either 16 or 32 bits wide; this is determined by the $\overline{BS16}$ signal which is static. The 82596 always drives all 32 data lines during Write operations, even with a 16-bit bus. D0–D31 are floated after a Reset or when the bus is not acquired.
These lines are inputs during a CPU Port access; in this mode the CPU writes the next address to the 82596 through the Data lines. During $\overline{PORT}$ commands (Relocatable SCP, Self-Test, and Dump) the address must be aligned to a 16 byte boundary. This frees the D_3–D_0 lines so they can be used to distinguish the commands. The following is a summary of the decoding data.
<table>
<tr><th>D0</th><th>D1</th><th>D2</th><th>D3</th><th>D4–D31</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0000</td><td>Reset</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>ADDR</td><td>Relocatable SCP</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>ADDR</td><td>Self-Test</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>ADDR</td><td>Dump Command</td></tr>
</table></td></tr>
<tr><td>(D15–D0)</td><td>14–32</td><td>I/O</td><td>These 16 Data Bus lines are bidirectional, tri-state lines that provide the entire data path for the 82596SX. In the 82596SX D16–D31 are not connected (NC).</td></tr>
<tr><td>A31–A2</td><td>70–108</td><td>O</td><td>ADDRESS LINES. These 30 tri-stated Address lines output the address bits required for memory operation. These lines are floated after a Reset or when the bus is not acquired.</td></tr>
<tr><td>A1</td><td>112</td><td>O</td><td>The 82596SX requires this additional address line to output the address bits required for memory operation.</td></tr>
<tr><td>$\overline{BE3}$–$\overline{BE0}$</td><td>109–114</td><td>O</td><td>BYTE ENABLE. (82596DX only.) These tri-stated signals are used to indicate which bytes are involved with the current memory access. The number of Byte Enable signals asserted indicates the physical size of the data being transferred (1, 2, 3, or 4 bytes).
• $\overline{BE0}$ indicates D0–D7
• $\overline{BE1}$ indicates D8–D15
• $\overline{BE2}$ indicates D16–D23
• $\overline{BE3}$ indicates D24–D31
These lines are floated after a Reset or when the bus is not acquired.</td></tr>
<tr><td>$\overline{BHE}$, $\overline{BLE}$</td><td>113–114</td><td>O</td><td>(82596SX only.) These signals are the Byte High Enable and Byte Low Enable signals for the 82596SX.</td></tr>
<tr><td>BON</td><td>109</td><td>O</td><td>BUS ON. (82596SX only.) This signal is driven high when the 82596 is holding the bus. This signal is tri-stated when the bus is relinquished. BON has the same timing as the Byte Enables.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
W/$\overline{R}$	120	O	**WRITE/READ.** This dual-function pin is used to distinguish Write and Read cycles. This line is floated after a Reset or when the bus is not acquired.
$\overline{ADS}$	124	O	**ADDRESS STATUS.** This tri-state pin is used by the 82596 to indicate that a valid bus cycle has begun and that A31–A2, $\overline{BE3}$–$\overline{BE0}$, and W/$\overline{R}$ are being driven. It is asserted during t1 bus states. This line is floated after a Reset or when the bus is not acquired.
$\overline{RDY}$	130	I	**READY.** Active low. This signal is the acknowledgment from addressed memory that the transfer cycle can be completed. When high, it causes wait states to be inserted. It is ignored at the end of the first clock of the bus cycle's data cycle. This active-low signal does not have an internal pull-up resistor. This signal must meet the setup and hold times to operate correctly.
$\overline{LOCK}$	126	O	**LOCK.** This tri-state pin is used to distinguish locked and unlocked bus cycles. $\overline{LOCK}$ generates a semaphore handshake to the CPU. $\overline{LOCK}$ can be active for several memory cycles, it goes active during the first locked memory cycle (t1) and goes inactive at the last locked cycle (t2). This line is floated after a Reset or when the bus is not acquired. $\overline{LOCK}$ can be disabled via the sysbus byte in software.
$\overline{BS16}$	129	I	**BUS SIZE.** This signal allows the 82596DX to work with either 16- or 32-bit bytes. This signal is static and should be tied high for 32-bit operation or low for 16-bit operation. In Little Endian mode the D0–D15 lines are driven when $\overline{BS16}$ is inserted, in Big Endian mode the D16–D31 lines are driven.
HOLD	123	O	**HOLD.** The HOLD signal is active high, the 82596 uses it to request local bus mastership. In normal operation HOLD goes inactive before HLDA. The 82596 can be forced off the bus by deasserting HLDA or if the bus throttle timers expire.
HLDA	118	I	**HOLD ACKNOWLEDGE.** The HLDA signal is active high, it indicates that bus mastership has been given to the 82596. HLDA is internally synchronized; after HOLD is detected low, the CPU drives HLDA low. **NOTE** *Do not connect HLDA to V_{CC}—it will cause a deadlock.* A user wanting to give the 82596 permanent access to the bus should connect HLDA to HOLD. If HLDA goes inactive before HOLD, the 82596 will release the bus (by deasserting HOLD) within a specified number of system clocks.
BREQ	115	I	**BUS REQUEST.** This signal, when configured to an externally activated mode, is used to trigger the bus throttle timers.

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
$\overline{PORT}$	3	I	**PORT.** When this signal is received, the 82596 latches the data on the data bus into an internal 32-bit register. When the CPU is asserting this signal it can write into the 82596 (via the data bus). This pin must be activated twice during all CPU Port access commands.
RESET	69	I	**RESET.** This active high, internally synchronized signal causes the 82596 to terminate current activity. The signal must be high for at least five system clock cycles. After five system clock cycles and four TxC clock cycles the 82596 will execute a Reset when it receives a high RESET signal. When RESET returns to low, the 82596 waits for the first CA signal and then begins the initialization sequence.
LE/$\overline{BE}$	65	I	**LITTLE ENDIAN/BIG ENDIAN.** This dual-function pin is used to select byte ordering. When LE/$\overline{BE}$ is high, little endian byte ordering is used; when low, big endian byte ordering is used for data in frames (bytes) and for control (SCB, RFD, CBL, etc.).
CA	119	I	**CHANNEL ATTENTION.** The CPU uses this pin to force the 82596 to begin executing memory resident Command blocks. The CA signal is internally synchronized. The signal must be high for at least one system clock. It is latched internally on the high to low edge and then detected by the 82596. The first CA after a Reset forces the 82596 into the initialization sequence beginning at location 00FFFFF6h or an SCP address written to the 82596 using CPU Port access. All subsequent CA signals cause the 82596 to begin executing new command sequences from the SCB.
INT/$\overline{INT}$	125	O	**INTERRUPT.** A high signal on this pin notifies the CPU that the 82596 is requesting an interrupt. This signal is an edge triggered interrupt signal, and can be configured to be active high or low.
V_{CC}	18 Pins (DX) 19 Pins (SX)		**POWER.** +5V ±10%.
V_{SS}	19 Pins (DX and SX)		**GROUND.** 0V.
TxD	54	O	**TRANSMIT DATA.** This pin transmits data to the serial link. It is high when not transmitting.
$\overline{TxC}$	64	I	**TRANSMIT CLOCK.** This signal provides the fundamental timing for the serial subsystem. The clock is also used to transmit data synchronously on the TxD pin. For NRZ encoding, data is transferred to the TxD pin on the high to low clock transition. For Manchester encoding, the transmitted bit center is aligned with the low to high transition. Transmit clock should always be running for proper device operation.

PIN DESCRIPTIONS (Continued)

Symbol	PQFP Pin No.	Type	Name and Function
$\overline{\text{LPBK}}$	58	O	**LOOPBACK.** This TTL-level control signal enables the loopback mode. In this mode serial data on the TxD input is routed through the 82C501 internal circuits and back to the RxD output without driving the transceiver cable. To enable this signal, both internal and external loopback need to be set with the Configure command.
RxD	60	I	**RECEIVE DATA.** This pin receives NRZ serial data only. It must be high when not receiving.
$\overline{\text{RxC}}$	59	I	**RECEIVE CLOCK.** This signal provides timing information to the internal shifting logic. For NRZ data the state of the RxD pin is sampled on the high to low transition of the clock.
$\overline{\text{RTS}}$	57	O	**REQUEST TO SEND.** When this signal is low the 82596 informs the external interface that it has data to transmit. It is forced high after a Reset or when transmission is stopped.
$\overline{\text{CTS}}$	62	I	**CLEAR TO SEND.** An active-low signal that enables the 82596 to send data. It is normally used as an interface handshake to $\overline{\text{RTS}}$. Asserting $\overline{\text{CTS}}$ high stops transmission. $\overline{\text{CTS}}$ is internally synchronized. If $\overline{\text{CTS}}$ goes inactive, meeting the setup time to the $\overline{\text{TxC}}$ negative edge, the transmission will stop and $\overline{\text{RTS}}$ will go inactive within, at most, two $\overline{\text{TxC}}$ cycles.
$\overline{\text{CRS}}$	63	I	**CARRIER SENSE.** This signal is active low, it is used to notify the 82596 that traffic is on the serial link. It is only used if the 82596 is configured for external Carrier Sense. In this configuration external circuitry is required for detecting traffic on the serial link. $\overline{\text{CRS}}$ is internally synchronized. To be accepted, the signal must remain active for at least two serial clock cycles (for CRSF = 0).
$\overline{\text{CDT}}$	61	I	**COLLISION DETECT.** This active-low signal informs the 82596 that a collision has occurred. It is only used if the 82596 is configured for external Collision Detect. External circuitry is required for collision detection. $\overline{\text{CDT}}$ is internally synchronized. To be accepted, the signal must remain active for at least two serial clock cycles (for CDTF = 0).

82596 AND HOST CPU INTERACTION

The 82596DX/SX and the host CPU communicate through shared memory. Because of its on-chip DMA capability, the 82596 can make data block transfers (buffers and frames) independently of the CPU; this greatly reduces the CPU byte transfer overhead.

NOTE:
The 82596DX and 82596SX differ in their address pin definitions and their data bus sizes. Information in this data sheet applies to both versions unless otherwise stated.

The 82596 is a multitasking coprocessor that comprises two independent logical units—the Command Unit (CU) and the Receive Unit (RU). The CU executes commands from shared memory. The RU handles all activities related to frame reception. The independence of the CU and RU enables the 82596 to engage in both activities simultaneously—the CU can fetch and execute commands from memory while the RU is storing received frames in memory. The CPU is only involved with this process after the CU has executed a sequence of commands or the RU has finished storing a sequence of frames.

The CPU and the 82596 use the hardware signals Interrupt (INT) and Channel Attention (CA) to initiate communication with the System Control Block (SCB), see Figure 4. The 82596 uses INT to alert the CPU of a change in the contents of the SCB, the CPU uses CA to alert the 82596.

The 82596 has a CPU Port Access state that allows the CPU to execute certain functions without accessing memory. The 82596 $\overline{\text{PORT}}$ pin and data bus pins are used to enable this feature. The CPU can directly activate four operations when the 82596 is in this state.

- Write an alternative System Configuration Pointer (SCP). This can be used when the 82596 cannot use the default SCP address space.
- Write a different Dump Command Pointer and execute Dump. This can be used for troubleshooting No Response problems.
- The CPU can reset the 82596 via software without disturbing the rest of the system.
- A self-test can be used for board testing; the 82596 will execute a self-test and write the results to memory.

82596 BUS INTERFACE

The 82596DX/SX has bus interface timings and pin definitions that are compatible with Intel's 32-bit i386 DX and i386 SX microprocessors. This eliminates the need for additional bus interface logic. Operating at 33 MHz, the 82596's bus bandwidth can be as high as 66 MB/s. Since Ethernet only requires 1.25 MB/s, this leaves a considerable amount of bandwidth for the CPU. The 82596 also has a bus throttle to regulate its use of the bus. Two timers can be programmed through the SCB: one controls the maximum time the 82596 can remain on the bus, the other controls the time the 82596 must stay off the bus (see Figure 5). The bus throttle can be programmed to trigger internally with HLDA or externally with BREQ. These timers can restrict the 82596 HOLD activation time and improve bus utilization.

82596 MEMORY ADDRESSING

The 82596 has a 32-bit memory address range, which allows addressing up to four gigabytes of memory. The 82596 has three memory addressing modes (see Table 1).

- **82586 Mode.** The 82596 has a 24-bit memory address range. The System Control Block, Command List, Receive Descriptor List, and Buffer Descriptors must reside in one 64-kB memory segment. Transmit and Receive buffers can reside in a 24-bit address space.
- **32-Bit Segmented Mode.** The 82596 has a 32-bit memory address range. The System Control Block, Command List, Receive Descriptor List, and Buffer Descriptors must reside in one 64-kB memory segment. Transmit and Receive buffers can reside in a 32-bit address space.
- **Linear Mode.** The 82596 has a 32-bit memory address range. Any memory structure can reside anywhere within the 32-bit memory address range.

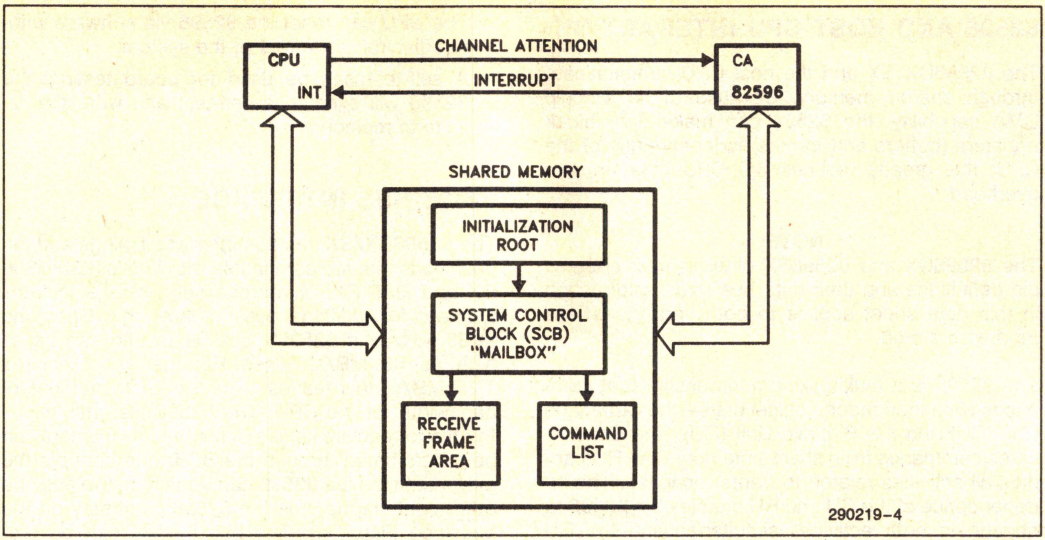


Figure 4. 82596 and Host CPU Intervention

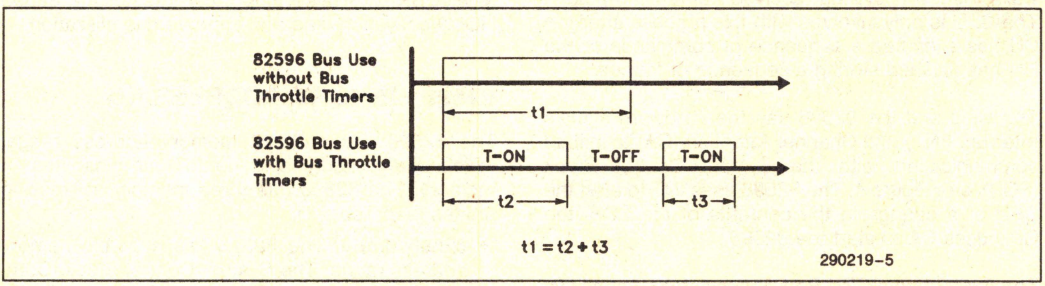


Figure 5. Bus Throttle Timers

Table 1. 82596 Memory Addressing Formats

Pointer or Offset	Operation Mode		
	82586	32-Bit Segmented	Linear
ISCP ADDRESS	24-Bit Linear	32-Bit Linear	32-Bit Linear
SCB ADDRESS	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Command Block Pointers	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Frame Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Tx Frame Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Buffer Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Tx Buffer Descriptors	Base (24) + Offset (16)	Base (32) + Offset (16)	32-Bit Linear
Rx Buffers	24-Bit Linear	32-Bit Linear	32-Bit Linear
Tx Buffers	24-Bit Linear	32-Bit Linear	32-Bit Linear

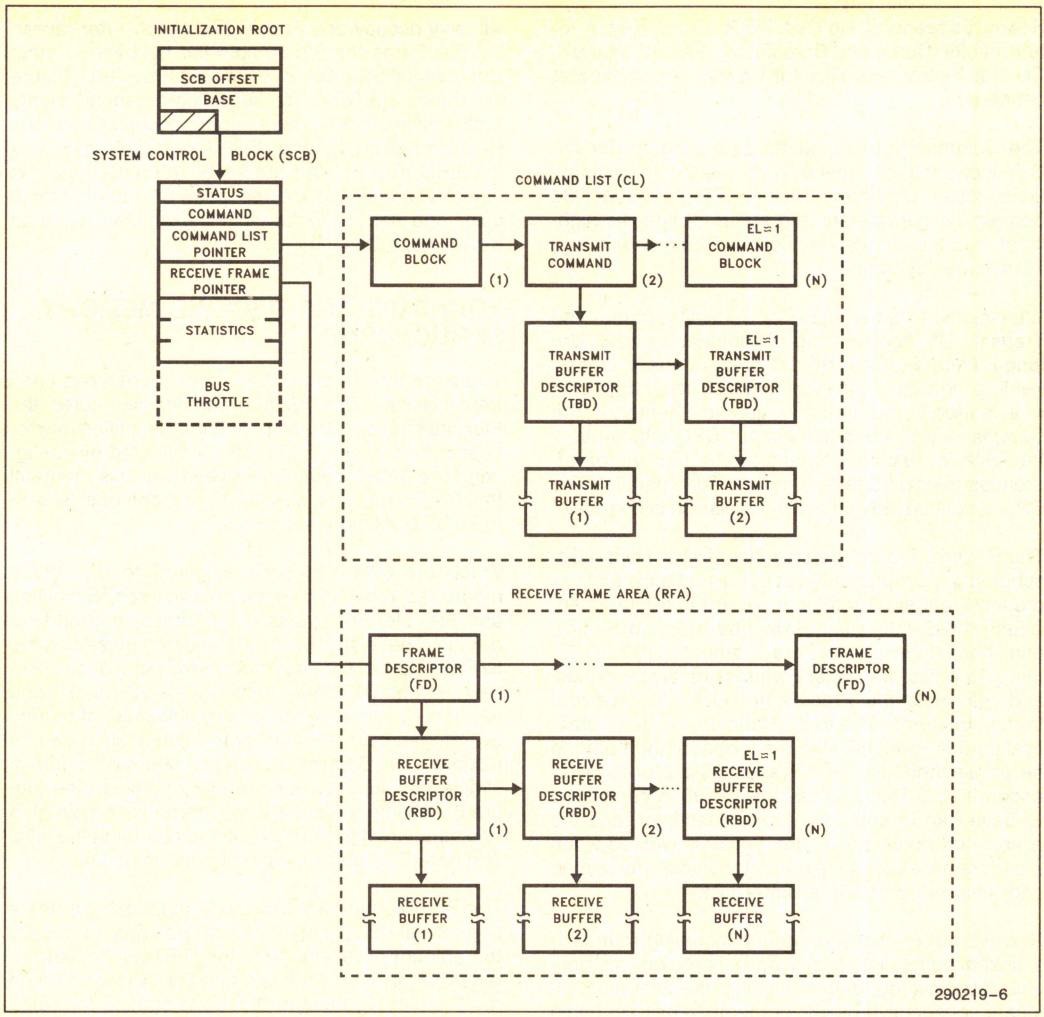


Figure 6. 82596 Shared Memory Structure

82596 SYSTEM MEMORY STRUCTURE

The Shared Memory structure consists of four parts: the Initialization Root, the System Control Block, the Command List, and the Receive Frame Area (see Figure 6).

The Initialization Root is in an established location known to the host CPU and the 82596 (00FFFFF6h). However, the CPU can establish the Initialization Root in another location by using the CPU Port access. This root is accessed during initialization, and points to the System Control Block.

The System Control Block serves as a bidirectional mail drop for the host CPU and the 82596 CU and RU. It is the central point through which the CPU and the 82596 exchange control and status information. The SCB has two areas. The first contains instructions from the CPU to the 82596. These include: control of the CU and RU (Start, Abort, Suspend, and Resume), a pointer to the list of CU commands, a pointer to the Receive Frame Area, a set of Interrupt Acknowledge bits, and the T-ON and T-OFF timers for the bus throttle. The second area contains status information the 82596 is sending to the CPU. Such as, the CU and RU states (Idle, Active

Ready, Suspended, No Receive Resources, etc.), interrupt bits (Command Completed, Frame Received, CU Not Ready, and RU Not Ready), and statistical counters.

The Command List functions as a program for the CU; individual commands are placed in memory units called Command Blocks (CBs). These CBs contain the parameters and status of specific high-level commands called Action Commands; e.g., Transmit or Configure.

Transmit causes the 82596 to transmit a frame. The Transmit CB contains the destination address, the length field, and a pointer to a list of linked buffers holding the frame that is to be constructed from several buffers scattered throughout memory. The Command Unit operates without CPU intervention; the DMA for each buffer, and the prefetching of references to new buffers, is performed in parallel. The CPU is notified only after a transmission is complete.

The Receive Frame Area is a list of Free Frame Descriptors (descriptors not yet used) and a list of user-prepared buffers. Frames arrive at the 82596 unsolicited; the 82596 must always be ready to receive and store them in the Free Frame Area. The Receive Unit fills the buffers when it receives frames, and reformats the Free Buffer List into received-frame structures. The frame structure is, for all practical purposes, identical to the format of the frame to be transmitted. The first Frame descriptor is referenced by the SCB. Unless the 82596 is configured to Save Bad Frames, the frame descriptor, and the associated buffer descriptor, which is wasted when a bad frame is received, are automatically reclaimed and returned to the Free Buffer List.

Receive buffer chaining (storing incoming frames in a linked buffer list) significantly improves memory utilization. Without buffer chaining, the user must allocate consecutive blocks of memory, each capable of containing a maximum frame (for Ethernet, 1518 bytes). Since an average frame is about 200 bytes, this is very inefficient. With buffer chaining, the user can allocate small buffers and the 82596 will only use those that are needed.

Figure 7 A–D illustrates how the 82596 uses the Receive Frame Area. Figure 7A shows an unused Receive Frame Area composed of Free Frame Descriptors and Free Receive Buffers prepared by the user. The SCB points to the first Frame Descriptor of the Frame Descriptor List. Figure 7B shows the same Receive Frame Area after receiving one frame. This first frame occupies two Receive Buffers and one Frame Descriptor—a valid received frame will only occupy one Frame Descriptor. After receiving this frame the 82596 sets the next Free Frame Descriptor RBD pointer to the next Free RBD. Figure 7C shows the RFA after receiving a second frame. In this example the second frame occupies only one Receive Buffer and one RFD. The 82596 again sets the RBD pointer. This process is repeated again in Figure 7D, showing the reception of another frame using one Receive Buffer; in this example there is an extra Frame Descriptor.

TRANSMIT AND RECEIVE MEMORY STRUCTURES

There are three memory structures for reception and transmission. The 82586 memory structure, the Flexible memory structure, and the Simplified memory structure. The 82586 mode is selected by configuring the 82596 during initialization. In this mode all the 82596 memory structures are compatible with the 82586 memory structures.

When the 82596 is not configured to the 82586 mode, the other two memory structures, Simplified and Flexible, are available for transmitting and receiving. These structures are selected by setting the S/F bit in the Transmit Command and/or the Receive Frame Descriptor (see Figures 29, 30, 41, and 42). It is recommended that any linked list of buffers be relegated to a single type—either simplified or flexible. The Simplified memory structure offers a simple structure for ease of programming (see Figure 8). All information about a frame is contained in one structure; for example, during reception the RFD and data field are contained in one structure.

The Flexible memory structure (see Figure 9) has a control field that allows the programmer to specify the amount of receive data the RFD will contain for receive operations and the amount of transmit data the Transmit Command Block will contain for transmit operations. For example, when the control field in the RFD is set to 20 bytes during a reception, the first 20 bytes of the data field are stored in the RFD (6 Bytes of Destination Address, 6 Bytes of Source Address, 2 Bytes of Length Field, and 6 Bytes of Data), and the remainder of the data field is stored in the Receive Data Buffers. This is useful for capturing frame headers when header information is contained in the data field. The header information can then be automatically stored in the RFD partitioned from the Receive Data Buffer.

The control field can also be used for the Transmit Command when the Flexible memory structure is used. The quantity of data field bytes to be transmitted from the Transmit Command Block is specified by the variable control field.

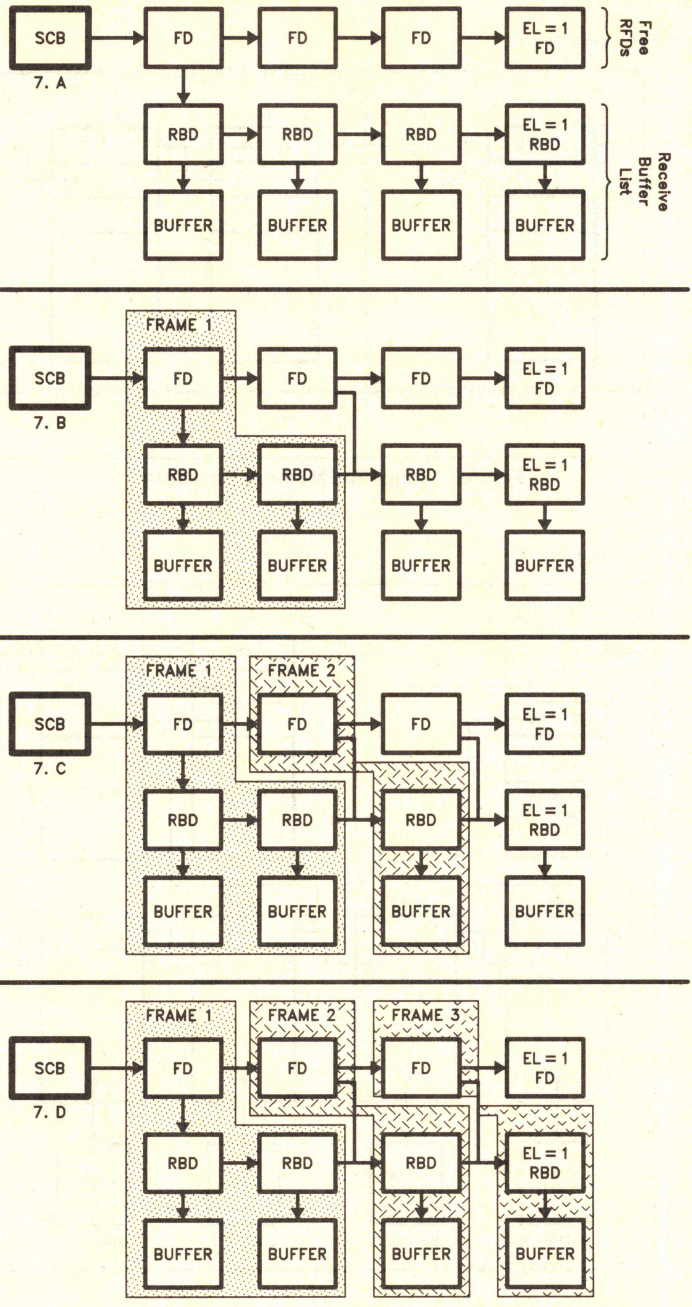


Figure 7. Frame Reception in the RFA

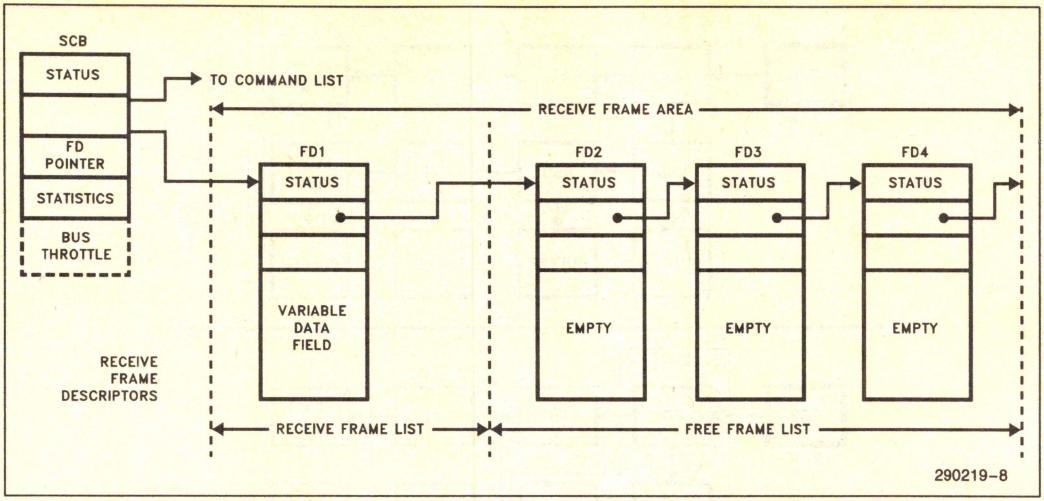


Figure 8. Simplified Memory Structure

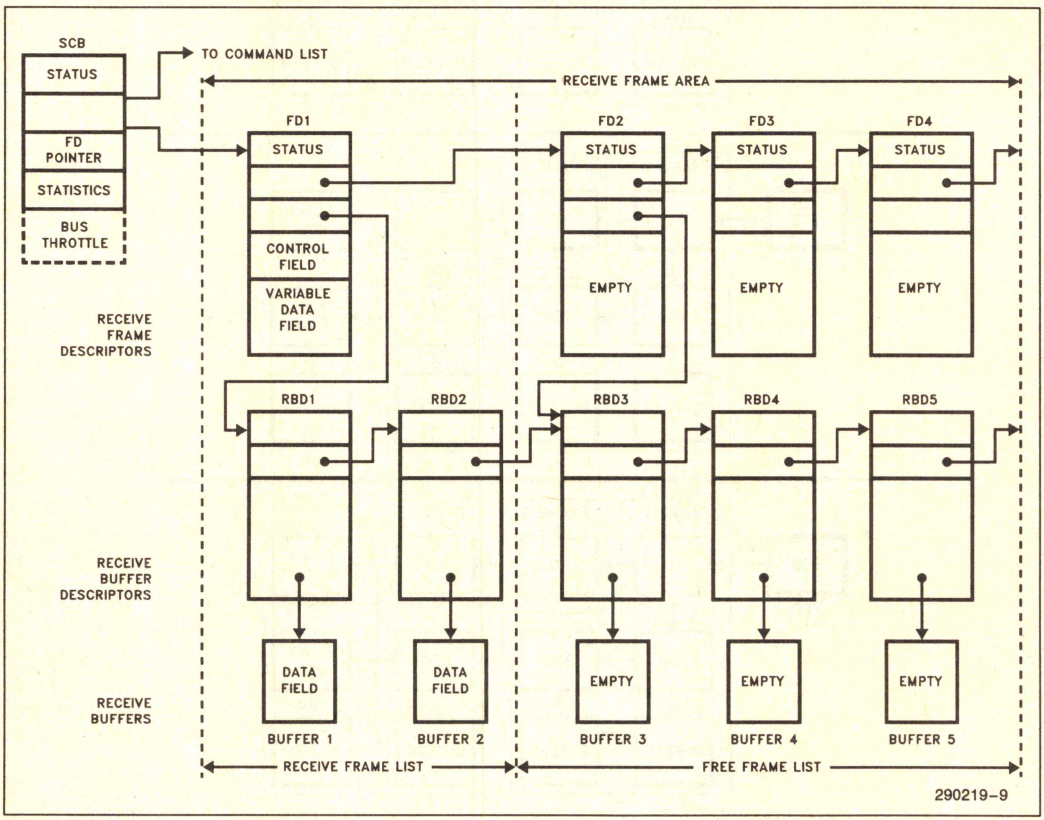


Figure 9. Flexible Memory Structure

TRANSMITTING FRAMES

The 82596 executes high-level Action Commands from the Command List in system memory. Action Commands are fetched and executed in parallel with the host CPU operation, thereby significantly improving system performance. The format of the Action Commands is shown in Figure 10. Figure 28 shows the 82586 mode, and Figures 29 and 30 shows the command formats of the Linear and 32-bit Segmented modes.

A single Transmit command contains, as part of the command-specific parameters, the destination address and length field of the transmitted frame and a pointer to buffer area in memory containing the data portion of the frame. The data field is contained in a memory data structure consisting of a buffer descriptor (BD) and a data buffer—or a linked list of buffer descriptors and buffers—as shown in Figure 11.

Multiple data buffers can be chained together using the BDs. Thus, a frame with a long data field can be transmitted using several (shorter) data buffers chained together. This chaining technique allows the system designer to develop efficient buffer management.

The 82596 automatically generates the preamble (alternating 1s and 0s) and start frame delimiter, fetches the destination address and length field from the Transmit command, inserts its unique address as the source address, fetches the data field specified by the Transmit command, and computes and appends the CRC to the end of the frame (see Figure 12). In the Linear and 32-bit Segmented mode the CRC can be optionally inserted on a frame-by-frame basis by setting the NC bit in the Transmit Command Block (see Figures 29 and 30).

The 82596 can be configured to generate two types of start and end frame delimiters—End of Carrier (EOC) or HDLC. In EOC mode the start frame delimiter is 10101011 and the end frame delimiter is indicated by the lack of a signal after the last bit of the frame check sequence field has been transmitted. In EOC mode the 82596 can be configured to extend short frames by adding pad bytes (7Eh) during transmission, according to the length field. In HDLC mode the 82596 will generate the 01111110 flag for the start and end frame delimiters, and do standard bit stuffing and stripping. Furthermore, the 82596 can be configured to pad frames shorter than the specified minimum frame length by appending the appropriate number of flags to the end of the frame.

When a collision occurs, the 82596 manages the jam, random wait, and retry processes, reinitializing DMA pointers without CPU intervention. Multiple frames can be sent by linking the appropriate number of Transmit commands together. This is particularly useful when transmitting a message larger than the maximum frame size (1518 bytes for Ethernet).

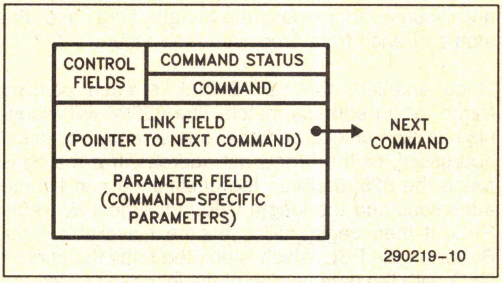


Figure 10. Action Command Format

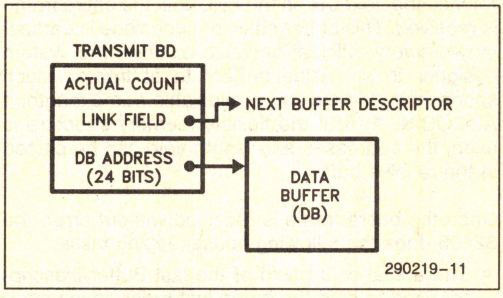


Figure 11. Data Buffer Descriptor and Data Buffer Structure

PREAMBLE	START FRAME DELIMITER	DESTINATION ADDRESS	SOURCE ADDRESS	LENGTH FIELD	DATA FIELD	FRAME CHECK SEQUENCE	END FRAME DELIMITER

Figure 12. Frame Format

RECEIVING FRAMES

To reduce CPU overhead, the 82596 is designed to receive frames without CPU supervision. The host CPU first sets aside an adequate receive buffer space and then enables the 82596 Receive Unit. Once enabled, the RU watches for arriving frames and automatically stores them in the Receive Frame Area (RFA). The RFA contains Receive Frame Descriptors, Receive Buffer Descriptors, and Data Buffers (see Figure 13). The individual Receive Frame Descriptors make up a Receive Descriptor List (RDL) used by the 82596 to store the destination and source addresses, the length field, and the status of each frame received (see Figure 14).

Once enabled, the 82596 checks each passing frame for an address match. The 82596 will recognize its own unique address, one or more multicast addresses, or the broadcast address. If a match is found the 82596 stores the destination and source addresses and the length field in the next available RFD. It then begins filling the next available Data Buffer on the FBL, which is pointed to by the current RFD, with the data portion of the incoming frame. As one Data Buffer is filled, the 82596 automatically fetches the next DB on the FBL until the entire frame is received. This buffer chaining technique is particularly memory efficient because it allows the system designer to set aside buffers to fit frames much shorter than the maximum allowable frame length. If AL-LOC = 1, or if the flexible memory structure is used, the addresses and length field can be placed in the receive buffer.

Once the entire frame is received without error, the 82596 does the following housekeeping tasks.

- The actual count field of the last Buffer Descriptor used to hold the frame just received is updated with the number of bytes stored in the associated Data Buffer.
- The next available Receive Frame Descriptor is fetched.
- The address of the next available Buffer Descriptor is written to the next available Receive Frame Descriptor.
- A frame received interrupt status bit is posted in the SCB.
- An interrupt is sent to the CPU.

If a frame error occurs, for example a CRC error, the 82596 automatically reinitializes its DMA pointers and reclaims any data buffers containing the bad frame. The 82596 will continue to receive frames without CPU help as long as Receive Frame Descriptors and Data Buffers are available.

82596 NETWORK MANAGEMENT AND DIAGNOSTICS

The behavior of data communication networks is normally very complex because of their distributed and asynchronous nature. It is particularly difficult to pinpoint a failure when it occurs. The 82596 has extensive diagnostic and network management functions that help improve reliability and testability. The 82596 reports on the following events after each frame is transmitted.

- Transmission successful.
- Transmission unsuccessful. Lost Carrier Sense.
- Transmission unsuccessful. Lost Clear to Send.
- Transmission unsuccessful. A DMA underrun occurred because the system bus did not keep up with the transmission.
- Transmission unsuccessful. The number of collisions exceeded the maximum allowed.
- Number of Collisions. The number of collisions experienced during transmission of the frame.
- Heartbeat Indicator. This indicates the presence of a heartbeat during the last Interframe Spacing (IFS) after transmission.

When configured to Save Bad Frames the 82596 checks each incoming frame and reports the following errors.

- CRC error. Incorrect CRC in a properly aligned frame.
- Alignment error. Incorrect CRC in a misaligned frame.
- Frame too short. The frame is shorter than the value configured for minimum frame length.
- Overrun. Part of the frame was not placed in memory because the system bus did not keep up with incoming data.
- Out of buffer. Part of the frame was discarded because of insufficient memory storage space.
- Receive collision. A collision was detected during reception and the destination address of the incoming frame passes 82596 address filtering. Collisions in the preamble are not counted.
- Length error. A frame not matching the frame length parameter was detected.

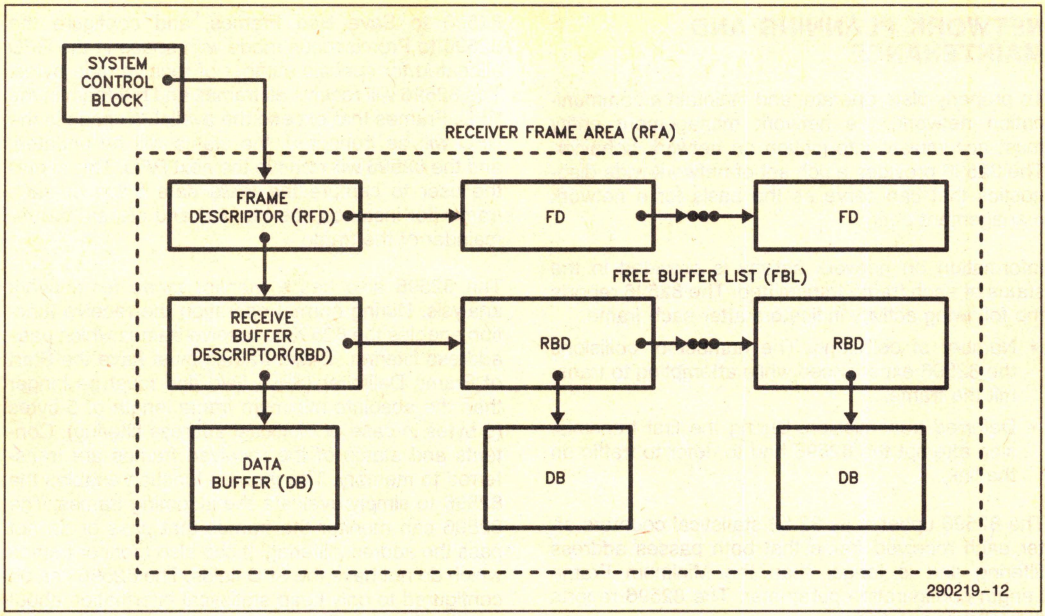


Figure 13. Receive Frame Area Diagram

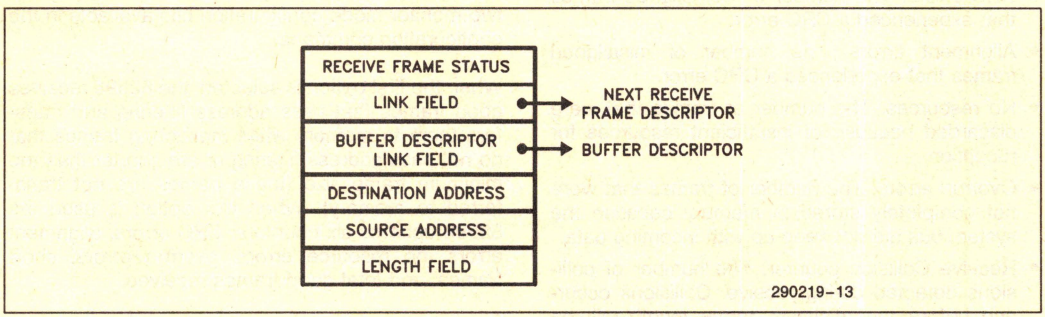


Figure 14. Receive Frame Descriptor

NETWORK PLANNING AND MAINTENANCE

To properly plan, operate, and maintain a communication network, the network management entity must accumulate information on network behavior. The 82596 provides a rich set of network-wide diagnostics that can serve as the basis for a network management entity.

Information on network activity is provided in the status of each frame transmitted. The 82596 reports the following activity indicators after each frame.

- Number of collisions. The number of collisions the 82596 experienced while attempting to transmit the frame.
- Deferred transmission. During the first transmission attempt the 82596 had to defer to traffic on the link.

The 82596 updates its 32-bit statistical counters after each received frame that both passes address filtering and is longer than the Minimum Frame Length configuration parameter. The 82596 reports the following statistics.

- CRC errors. The number of well-aligned frames that experienced a CRC error.
- Alignment errors. The number of misaligned frames that experienced a CRC error.
- No resources. The number of frames that were discarded because of insufficient resources for reception.
- Overrun errors. The number of frames that were not completely stored in memory because the system bus did not keep up with incoming data.
- Receive Collision counter. The number of collisions detected during receive. Collisions occurring before the minimum frame length will be counted as short frames. Collisions in the preamble will not be counted at all.
- Short Frame counter. The number of frames that were discarded because they were shorter than the configured minimum frame length.

Once again, these counters are not updated until the 82596 decodes a destination address match.

The 82596 can be configured to Promiscuous mode. In this mode it captures all frames transmitted on the network without checking the Destination Address. This is useful when implementing a monitoring station to capture all frames for analysis.

A useful method of capturing frame headers is to use the Simplified memory mode, configure the 82596 to Save Bad Frames, and configure the 82596 to Promiscuous mode with space in the RFD allocated for specific number of receive data bytes. The 82596 will receive all frames and put them in the RFD. Frames that exceed the available space in the RFD will be truncated, the status will be updated, and the 82596 will retrieve the next RFD. This allows the user to capture the initial data bytes of each frame (for instance, the header) and discard the remainder of the frame.

The 82596 also has a monitor mode for network analysis. During normal operation the receive function enables the 82596 to receive frames which pass address filtering. These frames must have the Start of Frame Delimiter (SFD) field and must be longer than the absolute minimum frame length of 5 bytes (6 bytes in case of Multicast address filtering). Contents and status of the received frames are transferred to memory. The monitor function enables the 82596 to simply evaluate the incoming frames. The 82596 can monitor the frames that pass or do not pass the address filtering. It can also monitor frames which do not have the SFD fields. The 82596 can be configured to only keep statistical information about monitor frames. Three options are available in the Monitor mode. These modes are selectable by the two monitor mode configuration bits available in the configuration command.

When the first option is selected, the 82596 receives good frames that pass address filtering and transfers them to memory while monitoring frames that do not pass address filtering or are shorter than the minimum frame size (these frames are not transferred to memory). When this option is used the 82596 updates six counters: CRC errors, alignment errors, no resource errors, overrun errors, short frames, and total good frames received.

When the second option is selected, the receive function is completely disabled. The 82596 monitors only those frames that pass address filterings and meet the minimum frame length requirement. When this option is used the 82596 updates six counters: CRC errors, alignment errors, total frames (good and bad), short frames, collisions detected, and total good frames.

When the third option is selected, the receive function is completely disabled. The 82596 monitors all frames, including frames that do not have a Start Frame Delimiter. When this option is used the 82596 updates six counter (CRC errors, alignment errors, total frames (good and bad), short frames, collisions detected, and total good frames.

STATION DIAGNOSTICS AND SELF-TEST

The 82596 provides a large set of diagnostic and network management functions. These include internal and external loopback and time domain reflectometry for locating fault points in the network cable. The 82596 ensures software reliability by dumping the contents of the 82596 internal registers into system memory. The 82596 has a self-test mode that enables it to run an internal self-test and place the results in system memory.

82586 SOFTWARE COMPATIBILITY

The 82596 has a software-compatible state in which all its memory structures are compatible with the 82586 memory structure. This includes all the Action Commands, the Receive Frame Area (including the RFD, Buffer Descriptors, and Data Buffers), the System Control Block, and the initialization procedures. There are two minor differences between the 82596 in the 82586-Compatible memory structure and the 82586.

- When the internal and external loopback bits in the Configure command are set to 11 the 82596 is in external loopback and the $\overline{\text{LPBK}}$ pin is activated; in the 82586 this situation would produce internal loopback.
- During a Dump command both the 82596 and 82586 dump the same number of bytes; however, the data format is different.

INITIALIZING THE 82596

A Reset command is issued to the 82596 to prepare it for normal operation. The 82596 is initialized through two data structures that are addressed by two pointers, the System Configuration Pointer (SCP) and the Intermediate System Configuration Pointer (ISCP). The initialization procedure begins when a Channel Attention signal is asserted after RESET. The 82596 uses the address of the double word that contains the SCP as a default—00FFFFF4h. Before the CA signal is asserted this default address can be changed to any other available address by asserting the $\overline{\text{PORT}}$ pin and providing the desired address over the $D_{31}-D_4$ pins of the address bus. Pins D_3-D_0 must be 0010; i.e., any alternative address must be aligned to 16 byte boundaries. All addresses sent to the 82596 must be word aligned, which means that all pointers and memory structures must start on an even address (A_0 = zero).

SYSTEM CONFIGURATION POINTER (SCP)

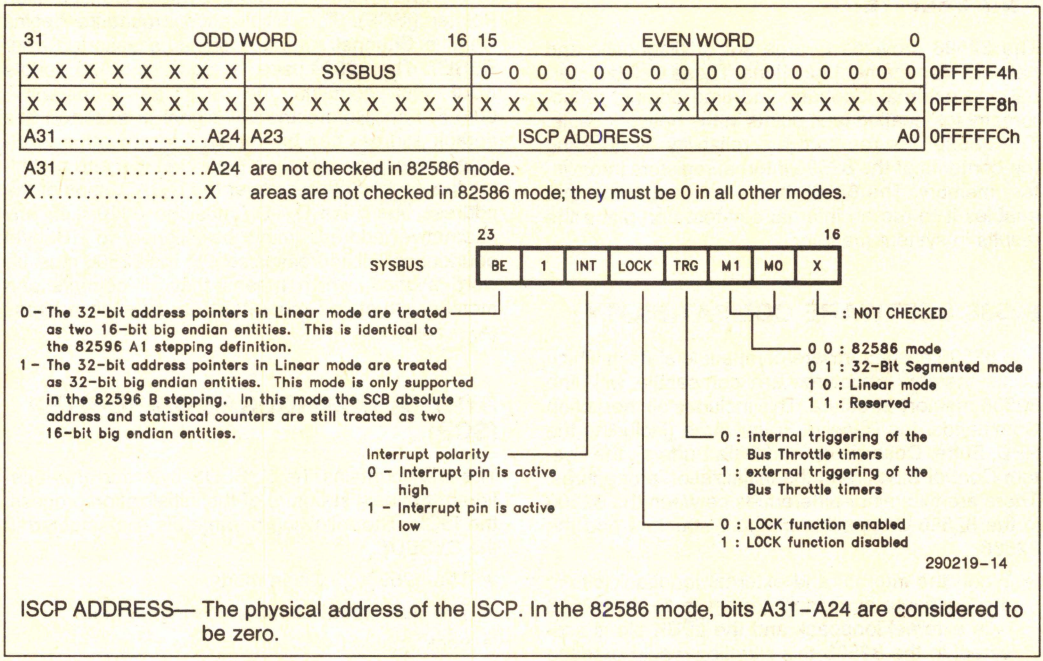
The SCP contains the SYSBUS byte and the location of the next structure of the initialization process, the ISCP. The following parameters are selected in the SYSBUS.

- The 82596 operation mode.
- The Bus Throttle timer triggering method.
- Lock enabled.
- Interrupt polarity.
- Big Endian 32-bit entity mode.

Byte ordering is determined by the LE/$\overline{\text{BE}}$ pin. LE/$\overline{\text{BE}}$ = 1 selects little endian byte ordering and LE/$\overline{\text{BE}}$ = 0 selects big endian byte ordering.

NOTE:
In the following, X indicates a bit not checked in 82586 mode. This bit must be set to 0 in all other modes.

The following diagram illustrates the format of the SCP.



ISCP ADDRESS— The physical address of the ISCP. In the 82586 mode, bits A31–A24 are considered to be zero.

Figure 15. The System Configuration Pointer

Writing the Sysbus

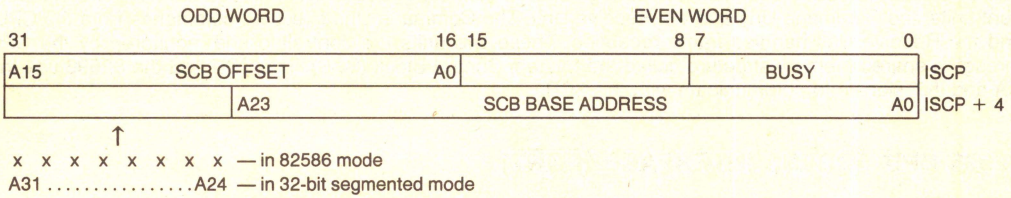
When writing the Sysbus byte it is important to pay attention to the byte order.

- When a Little Endian processor is used, the Sysbus byte is located at byte address 00FFFFF6h (or address $n+2$ if an alternative SCP address n was programmed).
- When a processor using Big Endian byte ordering is used, the SYSBUS, alternative SCP, and ISCP addresses will be different.
  - The Sysbus byte is located at 00FFFFF7h.
  - If an alternative SCP address is programmed, the SYSBUS byte should be at byte address $n+1$.

INTERMEDIATE SYSTEM CONFIGURATION POINTER (ISCP)

The ISCP indicates the location of the System Control Block. Often the SCP is in ROM and the ISCP is in RAM. The CPU loads the SCB address (or an equivalent data structure) into the ISCP and asserts CA. This Channel Attention signal causes the 82596 to begin its initialization procedure and to get the SCB address from the ISCP and SCP. In 82586 and 32-bit Segmented modes the SCP base address is also the base address of all Command Blocks, Frame Descriptors, and Buffer Descriptors (but not buffers). All these data structures must reside in one 64-kB segment; however, in Linear mode no such limitation is imposed.

The following diagram illustrates the ISCP format.

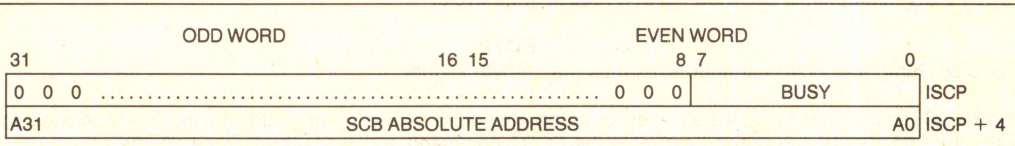


BUSY — Indicates that the 82596 is being initialized. The CPU sets the ISCP to 01h before it gives the first CA to the 82596. The ISCP is cleared by the 82596 after the SCB base and offset are read. Note that the most significant byte of the first word of the ISCP is not modified when BUSY is cleared.

SCB OFFSET— This 16-bit quantity specifies the offset portion of the address of the SCB.

SCB BASE — Specifies the base portion of the address of the SCB. The base of SCB is also the base of all 82596 Command Blocks, Frame Descriptors and Buffer Descriptors. In the 82586 mode, bits A31–A24 are considered to be zero.

Figure 16. The Intermediate System Configuration Pointer—82586 and 32-Bit Segmented Modes



BUSY — Indicates that the 82596 is being initialized. The ISCP is set to 01h by the CPU before its first CA to the 82596. It is cleared by the 82596 after the SCB address is read.

SCB ADDRESS— This 32-bit quantity specifies the physical address of the SCB.

Figure 17. The Intermediate System Configuration Pointer—Linear Mode.

INITIALIZATION PROCESS

The CPU sets up the SCP, ISCP, and the SCB structures, and, if desired, an alternative SCP address. It also sets BUSY to 01h. The 82596 is initialized when a Channel Attention signal follows a Reset signal, causing the 82596 to access the System Configuration Pointer. The sysbus byte, the operational mode, the bus throttle timer triggering method, the interrupt polarity, and the state of LOCK are read. After reset the bus throttle

timers are essentially disabled—the T-ON value is infinite, the T-OFF value is zero. After the SCP is read, the 82596 reads the ISCP and saves the SCB address. In 82586 and 32-bit Segmented modes this address is represented as a base address plus the offset (this base address is also the base address of all the control blocks). In Linear mode the base address is also an absolute address. The 82596 clears BUSY, sets CX and CNR to equal 1 in the SCB, clears the SCB command word, sends an interrupt to the CPU, and awaits another Channel Attention signal. RESET configures the 82596 to its default state before CA is asserted.

CONTROLLING THE 82596DX/SX

The host CPU controls the 82596 with the commands, data structures, and methods described in this section. The CPU and the 82596 communicate through shared memory structures. The 82596 contains two independent units: the Command Unit and the Receive Unit. The Command Unit executes commands from the CPU, and the Receive Unit handles frame reception. These two units are controlled and monitored by the CPU through a shared memory structure called the System Control Block (SCB). The CPU and the 82596 use the CA and INT signals to communicate with the SCB.

82596 CPU ACCESS INTERFACE ($\overline{\text{PORT}}$)

The 82596 has a CPU access interface that allows the host CPU to do four things.

- Write an alternative System Configuration Pointer address.
- Write an alternative Dump area pointer and perform Dump.
- Execute a software reset.
- Execute a self-test.

The following events initiate the CPU access state.

- Presence of an address on the $D_{31}-D_4$ data bus pins.
- The D_3-D_0 pins are used to select one of the four functions.
- The $\overline{\text{PORT}}$ input pin is asserted, as in a regular write cycle.

NOTE

The SCP Dump and Self-Test addresses must be 16-byte aligned.

The 82596 requires two 16-bit write cycles for a port command. The first write holds the internal machines and reads the first 16 bits, the second activates the $\overline{\text{PORT}}$ command and reads the second 16 bits.

The $\overline{\text{PORT}}$ Reset is useful when only the 82596 needs to be reset. The CPU must wait for 10-system and 5-serial clocks before issuing another CA to the 82596; this new CA begins a new initialization process.

The Dump function is useful for troubleshooting No Response problems. If the chip is in a No Response state, the $\overline{\text{PORT}}$ Dump operation can be executed and a $\overline{\text{PORT}}$ Reset can be used to reinitialize the 82596 without disturbing the rest of the system.

The Self-Test function can be used for board testing; the 82596 will execute a self-test and write the results to memory.

Table 2. $\overline{\text{PORT}}$ Function Selection

	D_{31} ..... D_4 ..... D_0						
Function	**Addresses and Results**			D_3	D_2	D_1	D_0
Reset	A31	Don't Care	A4	0	0	0	0
Self-Test	A31	Self-Test Results Address	A4	0	0	0	1
SCP	A31	Alternative SCP Address	A4	0	0	1	0
Dump	A31	Dump Area Pointer	A4	0	0	1	1

MEMORY ADDRESSING FORMATS

The 82596 accesses memory by 32-bit addresses. There are two types of 32-bit addresses: linear and segmented. The type of address used depends on the 82596 operating mode and the type of memory structure it is addressing. The 82596 has three operating modes.

- 82586 Mode
  - A Linear address is a single 24-bit entity. Address pins $A_{31}-A_{24}$ are always zero.
  - A Segmented address uses a 24-bit base and a 16-bit offset.
- 32-bit Segmented Mode
  - A Linear address is a single 32-bit entity.
  - A Segmented address uses a 32-bit base and a 16-bit offset.

NOTE:
In the previous two memory addressing modes, each command header (CB, TBD, RFD, RBD, and SCB) must wholly reside within one segment. If the 82596 encounters a memory structure that does not follow this restriction, the 82596 will fetch the next contiguous location in memory (beyond the segment).

- Linear Mode
  - A Linear address is a single 32-bit entity.
  - There are no Segmented addresses.

Linear addresses are primarily used to address transmit and receive data buffers. In the 82586 and 32-bit Segmented modes, segmented addresses (base plus offset) are used for all Command Blocks, Buffer Descriptors, Frame Descriptors, and System Control Blocks. When using Segmented addresses, only the offset portion of the entity being addressed is specified in the block. The base for all offsets is the same—that of the SCB. See Table A.

LITTLE ENDIAN AND BIG ENDIAN BYTE ORDERING

The 82596 supports both Little Endian and Big Endian byte ordering for its memory structures.

The 82596A1 stepping supports Big Endian byte ordering for word and byte entities. Dword entities are not supported with 82596A1 Big Endian byte ordering. This results in slightly different 82596 memory structures for Big Endian operation. These structures are defined in the *32-Bit LAN Components A1 Manual.*

The 82596 B stepping supports Big Endian byte ordering for dword, word, and byte entities in Linear mode only. All 82596 B 32-bit address pointers are treated as 32-bit Big Endian entities, however, the SCB absolute address and statistical counters are treated as two 16-bit Big Endian entities. This 32-bit Big Endian entity support is configured via bit 7 in the SYSBUS byte.

The 82596 C-step has a New Enhanced Big Endian Mode where in Linear Addressing mode, true 32-bit Big Endian functionality is achieved. New Enhanced Big Endian Mode is enabled exactly the same as the B-step, by setting bit 7 of the SYSBUS byte. This mode is software compatible with the big endian mode of the B-step with one exception—no 32-bit addresses need to be swapped by software in the C-step. In this new mode, the 82596 C-step treats 32-bit address pointers as true 32-bit entities and the SCB absolute address and statistical counters are still treated as two 16-bit big endian entities. Not setting this mode will configure the 82596 C-step to be 100% compatible to the A1-step big endian mode.

NOTE:
All 82596 memory entities must be word or dword aligned, except the transmit buffers can be byte aligned for the 82596 B or C steppings.

An example of a double word entity is a frame descriptor command/status dword, whereas the raw data of the frame are byte entities. Both 32- and 16-bit buses are supported. When a 16-bit bus is used with Big Endian memory organization, data lines D_{15}–D_0 are used. The 82596 has an internal crossover that handles these swap operations.

COMMAND UNIT (CU)

The Command Unit is the logical unit that executes Action Commands from a list of commands very similar to a CPU program. A Command Block is associated with each Action Command. The CU is modeled as a logical machine that takes, at any given time, one of the following states.

- **Idle.** The CU is not executing a command and is not associated with a CB on the list. This is the initial state.
- **Suspended.** The CU is not executing a command; however, it is associated with a CB on the list. The suspend state can only be reached if the CPU forces it through the SCB or sets the suspend bit in the RFD.
- **Active.** The CU is executing an Action Command and pointing to its CB.

The CPU can affect CU operation in two ways: by issuing a CU Control Command or by setting bits in the Command word of the Action Command.

When programming the 82596 CU, it is important to consider the asynchronous way the 82596 processes commands. If a command is issued to the 82596 CU, it may be busy processing other commands. In order to avoid asynchronous race conditions, the following guidelines are recommended to the 82596 programmer:

- If the CU is already in the Active state, and another command needs to be executed, it is unwise to immediately issue another CU Start command. If a new command (or list of commands) needs to be started, first issue a CU Suspend command, wait for the CU to become Suspended, then issue the new CU Start. This will insure that all commands are processed correctly.
- In general, it is a good idea to make sure any CU command has been accepted and executed before issuing a new control command to the CU.

RECEIVE UNIT (RU)

The Receive Unit is the logical unit that receives frames and stores them in memory. The RU is modeled as a logical machine that takes, at any given time, one of the following states.

- **Idle.** The RU has no memory resources and is discarding incoming frames. This is the initial state.
- **No Resources.** The RU has no memory resources and is discarding incoming frames. This state differs from Idle in that the RU accumulates statistics on the number of discarded frames.
- **Suspended.** The RU has memory available for storing frames, but is discarding them. The suspend state can only be reached if the CPU forces it through the SCB or sets the suspend bit in the RFD.
- **Ready.** The RU has memory available and is storing incoming frames.

The CPU can affect RU operation in three ways: by issuing a RU Control Command, by setting bits in the Frame Descriptor Command word of the frame being received, or by setting the EL bit of the current buffer's Buffer Descriptor.

When programming the 82596 RU, it is important to consider the asynchronous way the 82596 processes receive frames. If an RU Start is issued to the 82596 RU, it may be busy processing other incoming packets. In order to avoid asynchronous race conditions, the following guidelines are recommended to the 82596 programmer:

- If the RU is already in the Ready state, and a new RFA is required to be started, it is unwise to immediately issue another RU Start command. If the new RFA needs to be started, first issue an RU Suspend command, wait for the RU to become Suspended, then issue the new RU Start. This will insure that all incoming frames are received correctly.
- In general, it is a good idea to make sure any RU command has been accepted and executed before issuing a new control command to the RU.

SYSTEM CONTROL BLOCK (SCB)

The SCB is a memory block that plays a major role in communications between the CPU and the 82596. Such communications include the following.

- Commands issued by the CPU
- Status reported by the 82596

Control commands are sent to the 82596 by writing them into the SCB and then asserting CA. The 82596 examines the command, performs the required action, and then clears the SCB command word. Control commands perform the following types of tasks.

- Operation of the Command Unit (CU). The SCB controls the CU by specifying the address of the Command Block List (CBL) and by starting, suspending, resuming, or aborting execution of CBL commands.

- Operation of the Bus Throttle. The SCB controls the Bus Throttle timers by providing them with new values and sending the Load and Start timer commands. The timers can be operated in both the 32-bit Segmented and Linear modes.
- Reception of frames by the Receive Unit (RU). The SCB controls the RU by specifying the address of the Receive Frame Area and by starting, suspending, resuming, or aborting frame reception.
- Acknowledgment of events that cause interrupts.
- Resetting the chip.

The 82596 sends status reports to the CPU via the System Control Block. The SCB contains four types of status reports.

- The cause of the current interrupts. These interrupts are caused by one or more of the following 82596 events.
  - The Command Unit completes an Action Command that has its I bit set.
  - The Receive Unit receives a frame.
  - The Command Unit becomes inactive.
  - The Receive Unit becomes not ready.
- The status of the Command Unit.
- The status of the Receive Unit.
- Status reports from the 82596 regarding reception of corrupted frames.

Events can be cleared only by CPU acknowledgment. If some events are not acknowledged by the ACK field the Interrupt signal (INT) will be reissued after Channel Attention (CA) is processed. Furthermore, if a new event occurs while an interrupt is set, the interrupt is temporarily cleared to trigger edge-triggered interrupt controllers.

The CPU uses the Channel Attention line to cause the 82596 to examine the SCB. This signal is trailing-edge triggered—the 82596 latches CA on the trailing edge. The latch is cleared by the 82596 before the SCB control command is read.

31 ODD WORD 16	15 EVEN WORD 0	
ACK X CUC R RUC X X X X	STAT 0 CUS 0 RUS 0 0 0 0	SCB
RFA OFFSET	CBL OFFSET	SCB + 4
ALIGNMENT ERRORS	CRC ERRORS	SCB + 8
OVERRUN ERRORS	RESOURCE ERRORS	SCB + 12

Figure 18. SCB—82586 Mode

31 ODD WORD 16	15 EVEN WORD 0	
ACK 0 CUC R RUC 0 0 0 0	STAT 0 CUS RUS T 0 0 0	SCB
RFA OFFSET	CBL OFFSET	SCB + 4
CRC ERRORS		SCB + 8
ALIGNMENT ERRORS		SCB + 12
RESOURCE ERRORS (*)		SCB + 16
OVERRUN ERRORS (*)		SCB + 20
RCVCDT ERRORS (*)		SCB + 24
SHORT FRAME ERRORS		SCB + 28
T-ON TIMER	T-OFF TIMER	SCB + 32

*In MONITOR mode these counters change function

Figure 19. SCB—32-Bit Segmented Mode

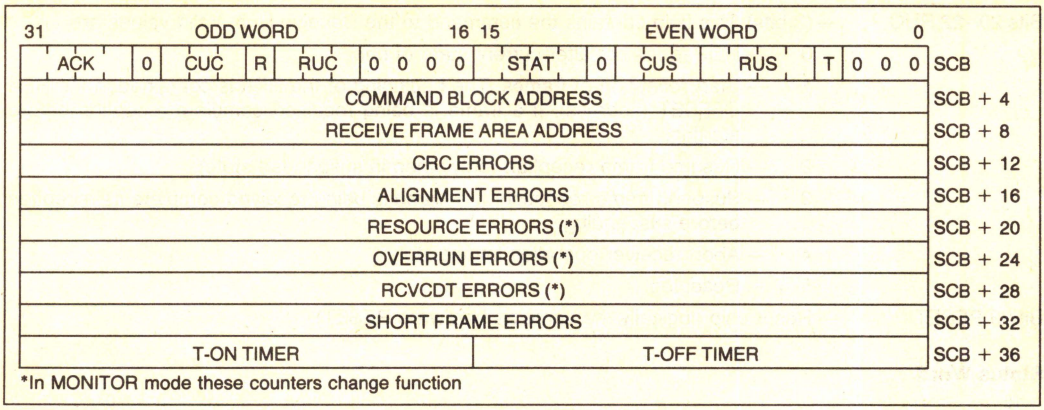
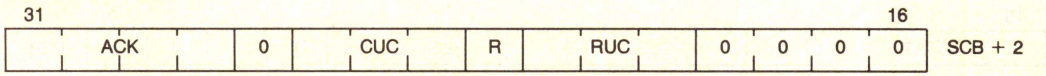


Figure 20. SCB—Linear Mode

Command Word



These bits specifiy the action to be performed as a result of a CA. This word is set by the CPU and cleared by the 82596. Defined bits are:

Bit 31 ACK-CX — Acknowledges that the CU completed an Action Command.

Bit 30 ACK-FR — Acknowledges that the RU received a frame.

Bit 29 ACK-CNA — Acknowledges that the Command Unit became not active.

Bit 28 ACK-RNR — Acknowledges that the Receive Unit became not ready.

Bits 24–26 CUC — (3 bits) This field contains the command to the Command Unit. Valid values are:

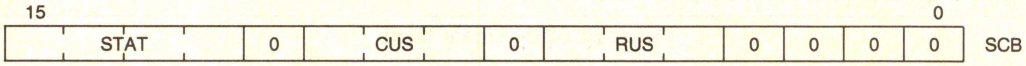
- 0 — NOP (does not affect current state of the unit).
- 1 — Start execution of the first command on the CBL. If a command is executing, complete it before starting the new CBL. The beginning of the CBL is in CBL OFFSET (address).
- 2 — Resume the operation of the Command Unit by executing the next command. This operation assumes that the Command Unit has been previously suspended.
- 3 — Suspend execution of commands on CBL after current command is complete.
- 4 — Abort current command immediately.
- 5 — Loads the Bus Throttle timers so they will be initialized with their new values after the active timer (T-ON or T-OFF) reaches Terminal Count. If no timer is active new values will be loaded immediately. This command is not valid in 82586 mode.
- 6 — Loads and immediately restarts the Bus Throttle timers with their new values. This command is not valid in 82586 mode.
- 7 — Reserved.

Bits 20–22 RUC — (3 bits) This field contains the command to the Receive Unit. Valid values are:

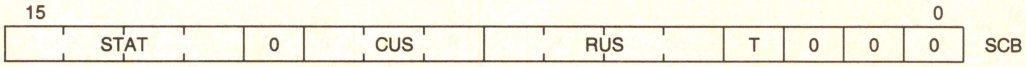
- 0 — NOP (does not alter current state of unit).
- 1 — Start reception of frames. The beginning of the RFA is contained in the RFA OFFSET (address). If a frame is being received complete reception before starting.
- 2 — Resume frame reception (only when in suspended state).
- 3 — Suspend frame reception. If a frame is being received complete its reception before suspending.
- 4 — Abort receiver operation immediately.
- 5–7 — Reserved.

Bit 23 RESET — Reset chip (logically the same as hardware RESET).

Status Word



82586 Mode



32-Bit Segmented and Linear Modes

Indicates the status of the 82596. This word is modified only by the 82596. Defined bits are:

Bit 15 CX — The CU finished executing a command with its I (interrupt) bit set.

Bit 14 FR — The RU finished receiving a frame.

Bit 13 CNA — The Command Unit left the Active state.

Bit 12 RNR — The Receive Unit left the Ready state.

Bits 8–10 CUS — (3 bits) This field contains the status of the command unit. Valid values are:

- 0 — Idle
- 1 — Suspended
- 2 — Active
- 3–7 — Not used

Bits 4–7 RUS — This field contains the status of the receive unit. Valid values are:

- 0h (0000) — Idle
- 1h (0001) — Suspended
- 2h (0010) — No resources. This bit indicates both no resources due to lack of RFDs in the RDL and no resources due to lack of RBDs in the FBL.
- 4h (0100) — Ready
- Ah (1010) — No resources due to no more RBDs. (Not in the 82586 mode.)
- Ch (1100) — No more RBDs (not in the 82586 mode).

No other combinations are allowed.

Bit 3 T — Bus Throttle timers loaded (not in 82586 mode).

SCB OFFSET ADDRESSES

CBL Offset (Address)

In 82586 and 32-bit Segmented modes this 16-bit quantity indicates the offset portion of the address for the first Command Block on the CBL. In Linear mode it is a 32-bit linear address for the first Command Block on the CBL. It is accessed only if CUC equals Start.

RFA Offset (Address)

In 82586 and 32-bit Segmented modes this 16-bit quantity indicates the offset portion of the address for the Receive Frame Area. In Linear mode it is a 32-bit linear address for the Receive Frame Area. It is accessed only if RUC equals Start.

SCB STATISTICAL COUNTERS

Statistical Counter Operation

- The CPU is responsible for clearing all error counters before initializing the 82596. The 82596 updates these counters by reading them, adding 1, and then writing them back to the SCB.
- The counters are wraparound counters. After reaching FFFFFFFFh the counters wrap around to zero.
- The 82596 updates the required counters for each frame. It is possible for more than one counter to be updated; multiple errors will result in all affected counters being updated.
- The 82596 executes the read-counter/increment/write-counter operation without relinquishing the bus (locked operation). This is to ensure that no logical contention exists between the 82596 and the CPU due to both attempting to write to the counters simultaneously. In the dual-port memory configuration the CPU should not execute any write operation to a counter if $\overline{\text{LOCK}}$ is asserted.
- The counters are 32-bits wide and their behavior is fully compatible with the IEEE 802.3 standard. The 82596 supports all relevant statistics (mandatory, optional, and desired) through the status of the transmit and receive header and directly through SCB statistics.

CRCERRS

This 32-bit quantity contains the number of aligned frames discarded because of a CRC error. This counter is updated, if needed, regardless of the RU state.

ALNERRS

This 32-bit quantity contains the number of frames that both are misaligned (i.e., where $\overline{\text{CRS}}$ deasserts on a nonoctet boundary) and contain a CRC error. The counter is updated, if needed, regardless of the RU state.

SHRTFRM

This 32-bit quantity contains the number of received frames shorter than the minimum frame length.

The last three counters change function in monitor mode.

RSCERRS

This 32-bit quantity contains the number of good frames discarded because there were no resources to contain them. Frames intended for a host whose RU is in the No Receive Resources state, fall into this category. This counter is updated only if the RU is in the No Resources state. When in Moniitor mode, this counter counts the total number of frames.

OVRNERRS

This 32-bit quantity contains the number of frames known to be lost because the local system bus was not available. If the traffic problem lasts longer than the duration of one frame, the frames that follow the first are lost without an indicator, and they are not counted. This counter is updated, if needed, regardless of the RU state.

RCVCDT

This 32-bit counter contains the number of collisions detected during frame reception. This counter will only be updated if at least 64 bytes of data are received before the collision occurs. If a collision occurs before 64 bytes of data are received, the frame is counted as a short frame. If the collisions occurs in the preamble, no counters are incremented.

ACTION COMMANDS AND OPERATING MODES

This section lists all the Action Commands of the Command Unit Command Block List (CBL). Each command contains the Command field, the Status and Control fields, the link to the next Action Command, and any command-specific parameters. There are three basic types of action commands: 82596 Configuration and Setup, Transmission, and Diagnostics. The following is a list of the actual commands.

- NOP
- Individual Address Setup
- Configure
- MC Setup
- Transmit
- TDR
- Dump
- Diagnose

The 82596 has three addressing modes. In the 82586 mode all the Action Commands look exactly like those of the 82586.

- **82586 Mode.** The 82596 software and memory structure is compatible with the 82586.
- **32-Bit Segmented Mode.** The 82596 can access the entire system memory and use the two new memory structures—Simplified and Flexible—while still using the segmented approach. This does not require any significant changes to existing software.
- **Linear Mode.** The 82596 operates in a flat, linear, 4 gigabyte memory space without segmentation. It can also use the two new memory structures.

In the 32-bit Segmented mode there are some differences between the 82596 and 82586 action commands, mainly in programming and activating new 82596 features. Those bits marked "don't care" in the compatible mode are not checked; however, we strongly recommend that those bits all be zeroes; this will allow future enchancements and extensions.

In the Linear mode all of the address offsets become 32-bit address pointers. All new 82596 features are accessible in this mode, and all bits previously marked "don't care" must be zeroes.

The Action Commands, and all other 82596 memory structures, must begin on even byte boundaries, i.e., they must be word aligned.

NOP

This command results in no action by the 82596 except for those performed in the normal command processing. It is used to manipulate the CBL manipulation. The format of the NOP command is shown in Figure 21.

NOP—82586 and 32-Bit Segmented Modes

31																16	15															0	
ODD WORD																	C	B	OK	EVEN WORD													0
EL	S	I	X	X	X	X	X	X	X	X	X	X	0	0	0					0	0	0	0	0	0	0	0	0	0	0	0		0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A15			LINK OFFSET											A0		4

NOP—Linear Mode

31																16	15															0	
ODD WORD																	C	B	OK	EVEN WORD													0
EL	S	I	0	0	0	0	0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0	0	0	0		0
A31																				LINK ADDRESS											A0		4

Figure 21

where:

LINK POINTER — In the 82586 or 32-bit Segmented modes this is a 16-bit offset to the next Command Block. In the Linear mode this is the 32-bit address of the next Command Block.

EL — If set, this bit indicates that this command block is the last on the CBL.

S — If set to one, suspend the CU upon completion of this CB.

I — If set to one, the 82596 will generate an interrupt after execution of the command is complete. If I is not set to one, the CX bit will not be set.

CMD (bits 16–18) — The NOP command. Value: 0h.

Bits 19–28 — Reserved (zero in the 32-bit Segmented and Linear modes).

C — This bit indicates the execution status of the command. The CPU initially resets it to zero when the Command Block is placed on the CBL. Following a command Completion, the 82596 will set it to one.

B — This bit indicates that the 82596 is currently executing the NOP command. It is initially reset to zero by the CPU. The 82596 sets it to one when execution begins and to zero when execution is completed. This bit is also set when the 82596 prefetches the command.

NOTE:

The C and B bits are modified in one operation.

OK — Indicates that the command was executed without error. If set to one no error occurred (command executed OK). If zero an error occur.

INDIVIDUAL ADDRESS SETUP

This command is used to load the 82596 with the Individual Address. This address is used by the 82596 for inserting the Source Address during transmission and recognizing the Destination Address during reception. After RESET, and prior to Individual Address Setup Command execution, the 82596 assumes the Broadcast Address is the Individual Address in all aspects, i.e.:

- This will be the Individual Address Match reference.
- This will be the Source Address of a transmitted frame (for AL-LOC = 0 mode only).

The format of the Individual Address Setup command is shown in Figure 22.

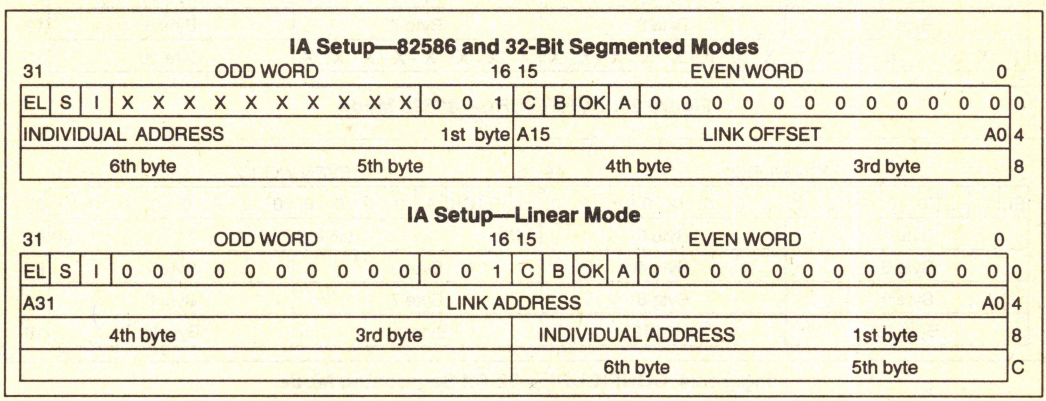


Figure 22

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted, and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (zero in the 32-bit Segmented and Linear modes).

CMD (bits 16–18) — The Address Setup command. Value: 1h.

INDIVIDUAL ADDRESS — The individual address of the node, 0 to 6 bytes long.

The least significant bit of the Individual Address must be zero for Ethernet (see the Command Structure). However, no enforcement of 0 is provided by the 82596. Thus, an Individual Address with 1 as its least significant bit is a valid Individual Address in all aspects.

The default address length is 6 bytes long, as in 802.3. If a different length is used the IA Setup command should be executed after the Configure command.

CONFIGURE

The Configure command loads the 82596 with its operating parameters. It allows changing some of the parameters by specifying a byte count less than the maximum number of configuration bytes (11 in the 82586 mode, 14 in the 32-Bit Segmented and Linear modes). The 82596 configuration depends on its mode of operation.

- In the 82586 mode the maximum number of configuration bytes is 12. Any number larger than 12 will be reduced to 12 and any number less than 4 will be increased to 4. When configuring the 12th byte (Byte 11 undefined) in 82586 mode this byte should be all ones.
- The additional features of the serial side are disabled in the 82586 mode.
- In both the 32-Bit Segmented and Linear modes there are four additional configuration bytes, which hold parameters for additional 82596 features. If these parameters are not accessed, the 82596 will follow their default values.
- For more detailed information refer to the *32-Bit LAN Components User's Manual.*

The format of the Configure command is shown in Figures 23, 24, and 25.

31 ODD WORD 16	15 EVEN WORD 0	
EL S I X X X X X X X X X X 0 1 0	C B OK A 0 0 0 0 0 0 0 0 0 0 0 0	0
Byte 1 / Byte 0	A15 LINK OFFSET A0	4
Byte 5 / Byte 4	Byte 3 / Byte 2	8
Byte 9 / Byte 8	Byte 7 / Byte 6	12
X X X X X X X X X X X X X X X X	X X X X X X X X / Byte 10	16

Figure 23. CONFIGURE—82586 Mode

31 ODD WORD 16	15 EVEN WORD 0	
EL S I 0 0 0 0 0 0 0 0 0 0 0 1 0	C B OK A 0 0 0 0 0 0 0 0 0 0 0 0	0
Byte 1 / Byte 0	A15 LINK OFFSET A0	4
Byte 5 / Byte 4	Byte 3 / Byte 2	8
Byte 9 / Byte 8	Byte 7 / Byte 6	12
Byte 13 / Byte 12	Byte 11 / Byte10	16

Figure 24. CONFIGURE—32-Bit Segmented Mode

31			ODD WORD										16	15					EVEN WORD												0	
EL	S	I	0	0	0	0	0	0	0	0	0	0	0	1	0	C	B	OK	A	0	0	0	0	0	0	0	0	0	0	0	0	0
A31																			LINK ADDRESS												A0	4
Byte 3								Byte 2								Byte 1								Byte 0								8
Byte 7								Byte 6								Byte 5								Byte 4								12
Byte 11								Byte 10								Byte 9								Byte 8								16
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Byte 13								Byte 12								20

Figure 25. CONFIGURE—Linear Mode

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to a CU Abort control command. If 1, then the command was aborted and if necessary it should be repeated. If this bit is 0, the command was not aborted.

Bits 19–28 — Reserved (zero in the 32-Bit Segmented and Linear Modes)

CMD (bits 16–18) — The CONFIGURE command. Value: 2h.

The interpretation of the fields follows:

7	6	5	4	3	2	1	0
P	X	X	X	BYTE COUNT			

BYTE 0

BYTE CNT (Bits 0–3) — Byte Count. Number of bytes, including this one, that hold parameters to be configured.

PREFETCHED (Bit 7) — Enable the 82596 to write the prefetched bit in all prefetch RBDs.

NOTE:

The P bit is valid only in the new memory structure modes. In 82586 mode this bit is disabled (i.e., no prefetched mark).

7							0
MONITOR		X	X	FIFO LIMIT			

BYTE 1

FIFO Limit (Bits 0–3) — FIFO limit.

MONITOR# (Bits 6–7) — Receive monitor options. If the Byte Count of the configure command is less than 12 bytes then these Monitor bits are ignored.

DEFAULT: C8h

7							0
SAV BF	1	0	0	0	0	RESUME_RD	0

BYTE 2

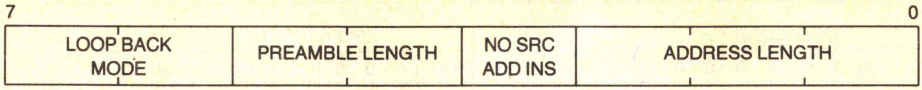
RESUME_RD (Bit 1) — 0— The 82596 does not reread the next CB on the list when a CU RESUME Control Command is issued.

1— The 82596 will reread the next CB on the list when a CU RESUME Control Command is issued. This is available only on the 82596B stepping.

SAV BF (Bit 7) — 0— Received bad frames are not saved in the memory.

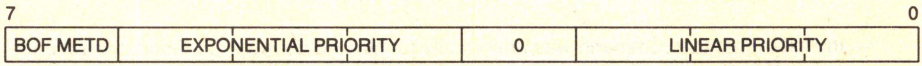
1— Received bad frames are saved in the memory.

DEFAULT: 40h



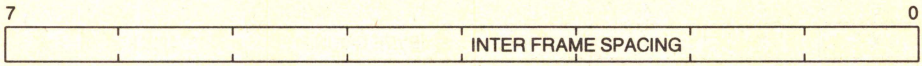
BYTE 3

ADR LEN (Bits 0–2)	Address length (any kind).
NO SCR ADD INS (Bit 3)	No Source Address Insertion. In the 82586 this bit is called AL LOC.
PREAM LEN (Bits 4–5)	Preamble length.
LP BCK MODE (Bits 6–7)	Loopback mode.
DEFAULT: 26h	



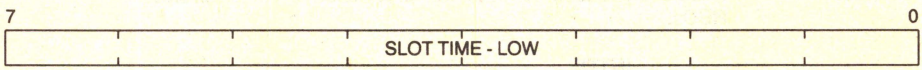
BYTE 4

LIN PRIO (Bits 0–2)	Linear Priority.
EXP PRIO (Bits 4–6)	Exponential Priority.
BOF METD (Bit 7)	Exponential Backoff method.
DEFAULT: 00h	



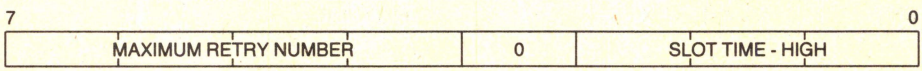
BYTE 5

INTERFRAME SPACING	Interframe spacing.
DEFAULT: 60h	



BYTE 6

SLOT TIME (L)	Slot time, low byte.
DEFAULT: 00h	



BYTE 7

SLOT TIME (H) (Bits 0–2)	Slot time, high part.
RETRY NUM (Bits 4–7)	Number of transmission retries on collision.
DEFAULT: F2h	

7							0
PAD	BIT STUFF	CRC16/ CRC32	NO CRC INSER	Tx ON NO CRS	MAN/ NRZ	BC DIS	PRM MODE

BYTE 8

PRM (Bit 0)	Promiscuous mode.
BC DIS (Bit 1)	Broadcast disable.
MANCH/NRZ (Bit 2)	Manchester or NRZ encoding. See specific timing requirements for TxC in Manchester mode.
TONO CRS (Bit 3)	Transmit on no CRS.
NOCRC INS (Bit 4)	No CRC insertion.
CRC-16/CRC-32 (Bit 5)	CRC type.
BIT STF (Bit 6)	Bit stuffing.
PAD (Bit 7)	Padding.
DEFAULT: 00h	

7			0
CDT SRC	COLLISION DETECT FILTER	CRS SRC	CARRIER SENSE FILTER

BYTE 9

CRSF (Bits 0–2)	Carrier Sense filter (length).
CRS SRC (Bit 3)	Carrier Sense source.
CDTF (Bits 4–6)	Collision Detect filter (length).
CDT SRC (Bit 7)	Collision Detect source.
DEFAULT: 00h	

7		0
	MINIMUM FRAME LENGTH	

BYTE 10

MIN FRAME LEN	Minimum frame length.
DEFAULT: 40h	

7							0
MONITOR	MC_ALL	CDBSAC	AUTOTX	CRCINM	LNGFLD	PRECRS	

BYTE 11

PRECRS (Bit 0)	Preamble until Carrier Sense
LNGFLD (Bit 1)	Length field. Enables padding at the End-of-Carrier framing (802.3).
CRCINM (Bit 2)	Rx CRC appended to the frame in memory.
AUTOTX (Bit 3)	Auto retransmit.
CDBSAC (Bit 4)	Collision Detect by source address recognition.
MC_ALL (Bit 5)	Enable to receive all MC frames.
MONITOR (Bits 6–7)	Receive monitor options.
DEFAULT: FFH	

7							0
0	FDX	0	0	0	0	0	0

BYTE 12

FDX (Bit 6) Enables Full Duplex operation.

DEFAULT: 00h

7							0
DIS_BOF	MULT_IA	1	1	1	1	1	1

BYTE 13

MULT_IA (Bit 6) Multiple individual address.

DIS_BOF (Bit 7) Disable the backoff algorithm.

DEFAULT: 3Fh

A reset (hardware or software) configures the 82596 according to the following defaults.

Table 4. Configuration Defaults

	Parameter	Default Value	Units/Meaning
	ADDRESS LENGTH	**6	Bytes
	A/L FIELD LOCATION	0	Located in FD
*	AUTO RETRANSMIT	1	Auto Retransmit Enable
	BITSTUFFING/EOC	0	EOC
	BROADCAST DISABLE	0	Broadcast Reception Enabled
*	CDBSAC	1	Disabled
	CDT FILTER	0	Bit Times
	CDT SRC	0	External Collision Detection
*	CRC IN MEMORY	1	CRC Not Transferred to Memory
	CRC-16/CRC-32	**0	CRC-32
	CRS FILTER	0	0 Bit Times
	CRS SRC	0	External CRS
*	DISBOF	0	Backoff Enabled
	EXT LOOPBACK	0	Disabled
	EXPONENTIAL PRIORITY	**0	802.3 Algorithm
	EXPONENTIAL BACKOFF METHOD	**0	802.3 Algorithm
*	FULL DUPLEX (FDX)	0	CSMA/CD Protocol (No FDX)
	FIFO THRESHOLD	8	TX: 32 Bytes, RX: 64 Bytes
	INT LOOPBACK	0	Disabled
	INTERFRAME SPACING	**96	Bit Times
	LINEAR PRIORITY	**0	802.3 Algorithm
*	LENGTH FIELD	1	Padding Disabled
	MIN FRAME LENGTH	**64	Bytes
*	MC ALL	1	Disabled
*	MONITOR	11	Disabled
	MANCHESTER/NRZ	0	NRZ
*	MULTI IA	0	Disabled
	NUMBER OF RETRIES	**15	Maximum Number of Retries
	NO CRC INSERTION	0	CRC Appended to Frame
	PREFETCH BIT IN RBD	0	Disabled (Valid Only in New Modes)
	PREAMBLE LENGTH	**7	Bytes
*	Preamble Until CRS	1	Disabled
	PROMISCUOUS MODE	0	Address Filter On
	PADDING	0	No Padding
	SLOT TIME	**512	Bit Times
	SAVE BAD FRAME	0	Discards Bad Frames
	TRANSMIT ON NO CRS	0	Disabled

NOTES:
1. This configuration setup is compatible with the IEEE 802.3 specification.
2. The Asterisk "*" signifies a new configuration parameter not available in the 82586.
3. The default value of the Auto retransmit configuration parameter is enabled (1).
4. Double Asterisk "**" signifies IEEE 802.3 requirements.

MULTICAST-SETUP

This command is used to load the 82596 with the Multicast-IDs that should be accepted. As noted previously, the filtering done on the Multicast-IDs is not perfect and some unwanted frames may be accepted. This command resets the current filter and reloads it with the specified Multicast-IDs. The format of the Multicast-addresses setup command is:

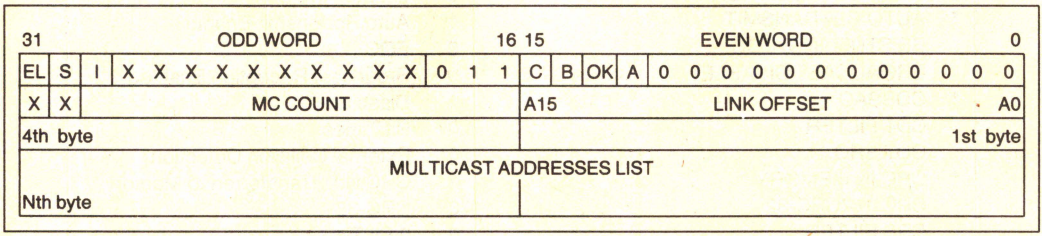


Figure 26. MC Setup—82586 and 32-Bit Segmented Modes

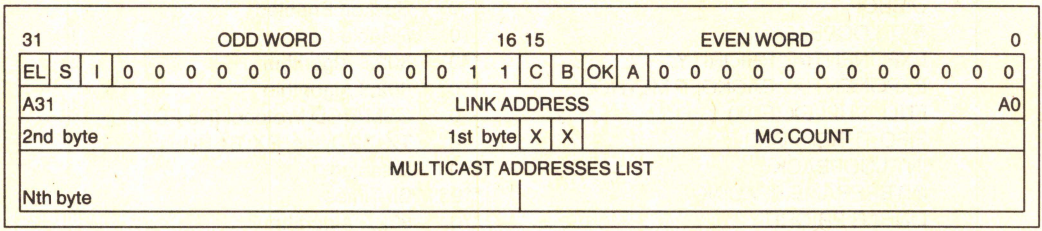


Figure 27. MC Setup—Linear Mode

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details)

A — Indicates that the command was abnormally terminated due to a CU Abort control command. If one, then the command was aborted and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (0 in both the 32-Bit Segmented and Linear Modes).

CMD (bits 16–18) — The MC SETUP command value: 3h.

MC-CNT — This 14-bit field indicates the number of bytes in the MC LIST field. The MC CNT must be a multiple of the ADDR LEN; otherwise, the 82596 reduces the MC CNT to the nearest ADDR LEN multiple. MC CNT = 0 implies resetting the Hash table which is equivalent to disabling the Multicast filtering mechanism.

MC LIST — A list of Multicast Addresses to be accepted by the 82596. The least significant bit of each MC address must be 1.

NOTE:

The list is sequential; i.e., the most significant byte of an address is immediately followed by the least significant byte of the next address.

— When the 82596 is configured to recognize multiple Individual Address (Multi-IA), the MC-Setup command is also used to set up the Hash table for the individual address.

The least significant bit in the first byte of each IA address must be 0.

TRANSMIT

This command is used to transmit a frame of user data onto the serial link. The format of a Transmit command is as follows.

31 ODD WORD 16	15 EVEN WORD 0	
EL S I X X X X X X X X X X 1 0 0	C B STATUS BITS MAXCOLL	0
A15 TBD OFFSET A0	A15 LINK OFFSET A0	4
4th byte	DESTINATION ADDRESS 1st byte	8
LENGTH FIELD	6th byte	12

Figure 28. TRANSMIT—82586 Mode

31 ODD WORD 16	15 EVEN WORD 0	
EL S I 0 0 0 0 0 0 0 0 NC SF 1 0 0	C B STATUS BITS MAXCOLL	0
A15 TBD OFFSET A0	A15 LINK OFFSET A0	4
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	EOF 0 TCB COUNT	8
4th byte	DESTINATION ADDRESS 1st byte	12
LENGTH FIELD	6th byte	16
OPTIONAL DATA		

Figure 29. TRANSMIT—32-Bit Segmented Mode

31 ODD WORD 16	15 EVEN WORD 0	
EL S I 0 0 0 0 0 0 0 0 NC SF 1 0 0	C B STATUS BITS MAXCOLL	0
A31 LINK ADDRESS A0		4
A31 TRANSMIT BUFFER DESCRIPTOR ADDRESS A0		8
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	EOF 0 TCB COUNT	12
4th byte	DESTINATION ADDRESS 1st byte	16
20 LENGTH FIELD	6th byte	
OPTIONAL DATA		

Figure 30. TRANSMIT—Linear Mode

31 COMMAND WORD 16	
EL S I 0 0 0 0 0 0 0 0 NC SF 1 0 0	2

↑ NC ↑ SF

- 0: No CRC Insertion disable; when the configure command is configured to not insert the CRC during transmission the NC has no effect.
- 1: No CRC Insertion enable; when the configure command is configured to insert the CRC during transmission the CRC will not be inserted when NC = 1.

- 0: Simplified Mode, all the Tx data is in the Transmit Command Block. The Transmit Buffer Descriptor Address field is all 1s.
- 1: Flexible Mode. Data is in the TCB and in a linked list of TBDs.

where:

EL, B, C, I, S	— As per standard Command Block (see the NOP command for details).
OK (Bit 13)	— Error free completion.
A (Bit 12)	— Indicates that the command was abnormally terminated due to CU Abort control command. If 1, then the command was aborted, and if necessary it should be repeated. If this bit is 0, the command was not aborted.
Bits 19–28	— Reserved (0 in the 32-bit Segmented and Linear modes).
CMD (Bits 16–18)	— The transmit command: 4h.
Status Bit 11	— Late collision. A late collision (a collision after the slot time is elapsed) is detected.
Status Bit 10	— No Carrier Sense signal during transmission. Carrier Sense signal is monitored from the end of Preamble transmission until the end of the Frame Check Sequence for TONOCRS = 1 (Transmit On No Carrier Sense mode) it indicates that transmission has been executed despite a lack of CRS. For TONOCRS = 0 (Ethernet mode), this bit also indicates unsuccessful transmission (transmission stopped when lack of Carrier Sense has been detected).
Status Bit 9	— Transmission unsuccessful (stopped) due to Loss of $\overline{\text{CTS}}$.
Status Bit 8	— Transmission unsuccessful (stopped) due to DMA Underrun; i.e., the system did not supply data for transmission.
Status Bit 7	— Transmission Deferred, i.e., transmission was not immediate due to previous link activity.
Status Bit 6	— Heartbeat Indicator, Indicates that after a previously performed transmission, and before the most recently performed transmission, (Interframe Spacing) the CDT signal was monitored as active. This indicates that the Ethernet Transceiver Collision Detect logic is performing properly. The Heartbeat is monitored during the Interframe Spacing period.
Status Bit 5	— Transmission attempt was stopped because the number of collisions exceeded the maximum allowable number of retries.
Status Bit 4	— 0 (Reserved).
MAX-COL (Bits 3–0)	— The number of Collisions experienced during this frame. Max Col = 0 plus S5 = 1 indicates 16 collisions.
LINK OFFSET	— As per standard Command Block (see the NOP for details).
TBD POINTER	— In the 82586 and 32-bit Segmented modes this is the offset of the first Tx Buffer Descriptor containing the data to be transmitted. In the Linear mode this is the 32-bit address of the first Tx Buffer Descriptor on the list. If the TBD POINTER is all 1s it indicates that no TBD is used.
DEST ADDRESS	— Contains the Destination Address of the frame. The least significant bit (MC) indicates the address type. MC = 0: Individual Address. MC = 1: Multicast or Broadcast Address. If the Destination Address bits are all 1s this is a Broadcast Address.
LENGTH FIELD	— The contents of this 2-byte field are user defined. In 802.3 it contains the length of the data field. It is placed in memory in the same order it is transmitted; i.e., most significant byte first, least significant byte second.
TCB COUNT	— This 14-bit counter indicates the number of bytes that will be transmitted from the Transmit Command Block, starting from the third byte after the TCB COUNT field (address $n+12$ in the 32-bit Segmented mode, $N+16$ in the Linear mode). The TCB COUNT field can be any number of bytes (including an odd byte), this allows the user to transmit a frame with a header having an odd number of bytes. The TCB COUNT field is not used in the 82586 mode.
EOF Bit	— Indicates that the whole frame is kept in the Transmit Command Block. In the Simplified memory model it must be always asserted.

The interpretation of what is transmitted depends on the No Source Address insertion configuration bit and the memory model being used.

NOTES

1. The Destination Address and the Length Field are sequential of the Length Field immediately follows the most significant byte of the Destination Address.
2. In case the 82596 is configured with No Source Address insertion bit equal to 0, the 82596 inserts its configured Source Address in the transmitted frame.
   - In the 82586 mode, or when the Simplified memory model is used, the Destination and Length fields of the transmitted frame are taken from the Transmit Command Block.
   - If the FLEXIBLE memory model is used, the Destination and Length fields of the transmitted frame can be found either in the TCB or TBD, depending on the TCB COUNT.
3. If the 82596 is configured with the Address/Length Field Location equal to 1, the 82596 does not insert its configured Source Address in the transmitted frame. The first (2 × Address Length) + 2 bytes of the transmitted frame are interpreted as Destination Address, Source Address, and Length fields respectively. The location of the first transmitted byte depends on the operational mode of the 82596:
   - In the 82586 mode, it is always the first byte of the first Tx Buffer.
   - In both the 32-bit Segmented and Linear modes it depends on the SF bit and TCB COUNT:
     — In the Simplified memory mode the first transmitted byte is always the third byte after the TCB COUNT field.
     — In the Flexible mode, if the TCB COUNT is greater than 0 then it is the third byte after the TCB COUNT field. If TCB COUNT equals 0 then it is first byte of the first Tx Buffer.
   - Transmit frames shorter than six bytes are invalid. The transmission will be aborted (only in 82586 mode) because of a DMA Underrun.
4. Frames which are aborted during transmission are jammed. Such an interruption of transmission can be caused by any reason indicated by any of the status bits 8, 9, 10 and 12.

JAMMING RULES

1. Jamming will not start before completion of preamble transmission.
2. Collisions detected during transmission of the last 11 bits will not result in jamming.

The format of a Transmit Buffer Descriptor is:

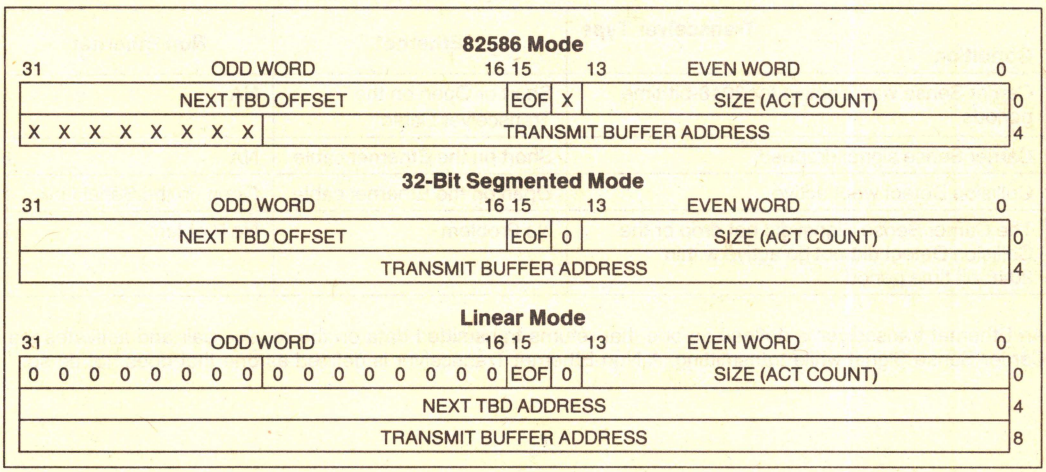


Figure 31

where:

EOF — This bit indicates that this TBD is the last one associated with the frame being transmitted. It is set by the CPU before transmit.

SIZE (ACT COUNT) — This 14-bit quantity specifies the number of bytes that hold information for the current buffer. It is set by the CPU before transmission.

NEXT TBD ADDRESS — In the 82586 and 32-bit Segmented modes, it is the offset of the next TBD on the list. In the Linear mode this is the 32-bit address of the next TBD on the list. It is meaningless if EOF = 1.

BUFFER ADDRESS — The starting address of the memory area that contains the data to be sent. In the 82586 mode, this is a 24-bit address (A31–A24 are considered to be zero). In the 32-bit Segmented and Linear modes this is a 32-bit address. This buffer can be byte aligned for the 82596 B-step.

TDR

This operation activates Time Domain Reflectometry, which is a mechanism to detect open or short circuits on the link and their distance from the diagnosing station. The TDR command has no parameters. The TDR transmit sequence was changed, compared to the 82586, to form a regular transmission. The TDR command is designed to be used statically. Make sure that both the CU and RU are idle before attempting a TDR command. The TDR bit stream is as follows.

— Preamble

— Source address

— Another Source address (the TDR frame is transmitted back to the sending station, so DEST ADR = SRC ADR).

— Data field containing 7Eh patterns.

— Jam Pattern, which is the inverse CRC of the transmitted frame.

Maximum length of the TDR frame is 2048 bits. If the 82596 senses collision while transmitting the TDR frame it transmits the jam pattern and stops the transmission. The 82596 then triggers an internal timer (STC); the timer is reset at the beginning of transmission and reset if CRS is returned. The timer measures the time elapsed from the start of transmission until an echo is returned. The echo is indicated by Collision Detect going active or a drop in the Carrier Sense signal. The following table lists the possible cases that the 82596 is able to analyze.

Conditions of TDR as Interpreted by the 82596

Transceiver Type / Condition	Ethernet	Non Ethernet
Carrier Sense was inactive for 2048-bit-time periods	Short or Open on the Transceiver Cable	NA
Carrier Sense signal dropped	Short on the Ethernet cable	NA
Collision Detect went active	Open on the Ethernet cable	Open on the Serial Link
The Carrier Sense Signal did not drop or the Collision Detect did not go active within 2048-bit time period	No Problem	No Problem

An Ethernet transceiver is defined as one that returns transmitted data on the receive pair and activates the Carrier Sense Signal while transmitting. A Non-Ethernet Transceiver is defined as one that does not do so.

The format of the Time Domain Reflectometer command is:

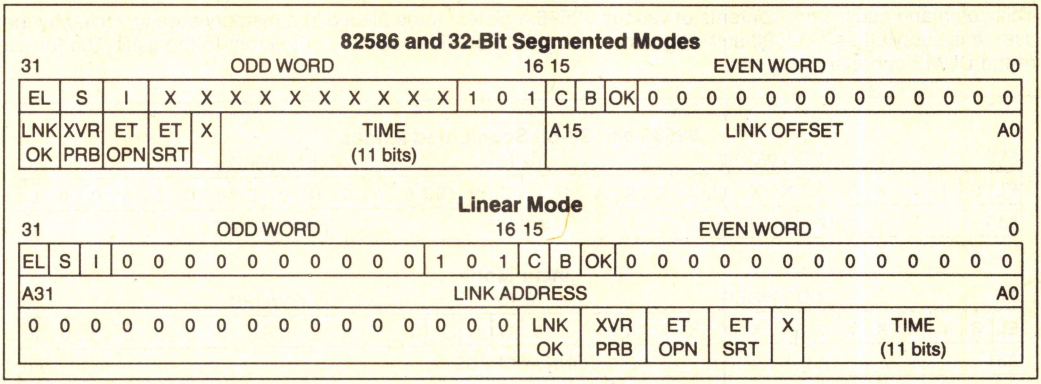


Figure 32. TDR

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details).

A — Indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted, and if necessary it should be repeated. If this bit is zero, the command was not aborted.

Bits 19–28 — Reserved (0 in the 32-bit Segmented and Linear Modes).

CMD (Bits 16–18) — The TDR command. Value: 5h.

TIME — An 11-bit field that specifies the number of TxC cycles that elapsed before an echo was observed. No echo is indicated by a reception consisting of "1s" only. Because the network contains various elements such as transceiver links, transceivers, Ethernet, repeaters etc., the TIME is not exactly proportional to the problems distance.

LNK OK (Bit 15) — No link problem identified. TIME = 7FFh.

XCVR PRB (Bit 14) — Indicates a Transceiver problem. Carrier Sense was inactive for 2048-bit time period. LNK OK = 0. TIME = 7FFh.

ET OPN (Bit 13) — The transmission line is not properly terminated. Collision Detect went active and LNK OK = 0.

ET SRT (Bit 12) — There is a short circuit on the transmission line. Carrier Sense Signal dropped and LNK OK = 0.

DUMP

This command causes the contents of various 82596 registers to be placed in a memory area specified by the user. It is supplied as a 82596 self-diagnostic tool, and to provide registers of interest to the user. The format of the DUMP command is:

82586 and 32-Bit Segmented Modes

31			ODD WORD									16	15					EVEN WORD											0
EL	S	I	X	X	X	X	X	X	X	X	X	X	1	1	0	C	B	OK	0	0	0	0	0	0	0	0	0	0	0	0
A15								BUFFER OFFSET							A0	A15								LINK OFFSET					A0

Linear Mode

31			ODD WORD									16	15					EVEN WORD											0
EL	S	I	X	X	X	X	X	X	X	X	X	X	1	1	0	C	B	OK	0	0	0	0	0	0	0	0	0	0	0	0
A31																		LINK ADDRESS											A0
A31																		BUFFER ADDRESS											A0

Figure 33. Dump

where:

LINK ADDRESS, EL, B, C, I, S — As per standard Command Block (see the NOP command for details).

OK — Indicates error free completion.

Bits 19–28 — Reserved (0 in the 32-bit Segmented and Linear Modes).

CMD (Bits 16–18) — The Dump command. Value: 6h.

BUFFER POINTER — In the 82586 and 32-bit Segmented modes this is the 16-bit-offset portion of the dump area address. In the Linear mode this is the 32-bit linear address of the dump area.

Dump Area Information Format

- The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586. The compatible data will be marked with an asterisk.
- In 82586 mode the dump area is 170 bytes.
- The dump area format of the 32-bit Segmented and Linear modes is described in Figure 35.
- The size of the dump area of the 32-bit Segmented and Linear modes is 304 bytes.
- When the dump is executed by the Port command an extra word will be appended to the Dump Area. The extra word is a copy of the Dump Area status word (containing the *C, B,* and *OK* bits). The *C* and *OK* bits are set when the 82596 has completed the Port Dump command.

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
DMA CONTROL REGISTER*	00
CONFIGURE BYTES 3, 2	02
CONFIGURE BYTES 5, 4	04
CONFIGURE BYTES 7, 6	06
CONFIGURE BYTES 9, 8	08
CONFIGURE BYTES 10	0A
I.A. BYTES 1, 0*	0C
I.A. BYTES 3, 2*	0E
I.A. BYTES 5, 4*	10
LAST T.X. STATUS*	12
T.X. CRC BYTES 1, 0*	14
T.X. CRC BYTES 3, 2*	16
R.X. CRC BYTES 1, 0*	18
R.X. CRC BYTES 3, 2*	1A
R.X. TEMP MEMORY 1, 0*	1C
R.X. TEMP MEMORY 3, 2*	1E
R.X. TEMP MEMORY 5, 4*	20
LAST RECEIVED STATUS*	22
HASH REGISTER BYTES 1, 0*	24
HASH REGISTER BYTES 3, 2*	26
HASH REGISTER BYTES 5, 4*	28
HASH REGISTER BYTES 7, 6*	2A
SLOT TIME COUNTER*	2C
WAIT TIME COUNTER*	2E
MICRO MACHINE** . REGISTER FILE . . 60 BYTES	30 6A
MICRO MACHINE LFSR**	6C
MICRO MACHINE . FLAG ARRAY . 14 BYTES	6E 7A
QUEUE MEMORY** . CU PORT 8 BYTES	7C 82
MICRO MACHINE ALU**	84
RESERVED**	86
M.M. TEMP A ROTATE R**	88
M.M. TEMP A**	8A
T.X. DMA BYTE COUNT**	8C
M.M. INPUT PORT ADDRESS**	8E
T.X. DMA ADDRESS**	90
M.M. OUTPUT PORT**	92
R.X. DMA BYTE COUNT**	94
M.M. OUTPUT PORT ADDRESS REGISTER**	96
R.X. DMA ADDRESS**	98
RESERVED**	9A
BUS THROTTLE TIMERS	9C
DIU CONTROL REGISTER**	9E
RESERVED**	A0
DMA CONTROL REGISTER**	A2
BIU CONTROL REGISTER**	A4
M.M. DISPATCHER REGISTER**	A6
M.M. STATUS REGISTER**	A8

NOTE:
*The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586. The compatible data will be marked with an asterisk.
**These bytes are not user defined, results may vary from Dump command to Dump command.

1

Figure 34. Dump Area Format—82586 Mode

31	0	
CONFIGURE BYTES 5, 4, 3, 2		00
CONFIGURE BYTES 9, 8, 7, 6		04
CONFIGURE BYTES 13, 12, 11, 10		08
I.A. BYTES 1, 0	X X X X X X X X	0C
I.A. BYTES 5, 2		10
TX CRC BYTES 0, 1	LAST T.X. STATUS	14
RX CRC BYTES 0, 1	TX CRC BYTES 3, 2	18
RX TEMP MEMORY 1, 0	RX CRC BYTES 3, 2	1C
R.X. TEMP MEMORY 5, 2		20
HASH REGISTERS 1, 0	LAST R.X. STATUS	24
HASH REGISTER BYTES 5, 2		28
SLOT TIME COUNTER	HASH REGISTERS 7, 6	2C
RECEIVE FRAME LENGTH	WAIT-TIME COUNTER	30
MICRO MACHINE**		34
REGISTER FILE		.
		.
128 BYTES		B0
MICRO MACHINE LFSR**		B4
MICRO MACHINE**		B8
FLAG ARRAY		.
		.
28 BYTES		D0
M.M. INPUT PORT**		D4
16 BYTES		E0
MICRO MACHINE ALU**		E4
RESERVED**		E8
M.M. TEMP A ROTATE R.**		EC
M.M. TEMP A**		F0
T.X. DMA BYTE COUNT**		F4
M.M. INPUT PORT ADDRESS REGISTER**		F8
T.X. DMA ADDRESS**		FC
M.M. OUTPUT PORT REGISTER**		100
R.X. DMA BYTE COUNT**		104
M.M. OUTPUT PORT ADDRESS REGISTER**		108
R.X. DMA ADDRESS REGISTER**		10C
RESERVED**		110
BUS THROTTLE TIMERS		114
DIU CONTROL REGISTER**		118
RESERVED**		11C
DMA CONTROL REGISTER**		120
BIU CONTROL REGISTER**		124
M.M. DISPATCHER REG.**		128
M.M. STATUS REGISTER**		12C

NOTE:
The 82596 is not Dump compatible with the 82586 because of the 32-bit internal architecture. In 82586 mode the 82596 will dump the same number of bytes as the 82586. The compatible data will be marked with an asterisk.
**These bytes are not user defined, results may vary from Dump command to Dump command.

Figure 35. Dump Area Format—Linear and 32-Bit Segmented Mode

DIAGNOSE

The Diagnose Command triggers an internal self-test procedure that checks internal 82596 hardware, which includes:

- Exponential Backoff Random Number Generator (Linear Feedback Shift Register).
- Exponential Backoff Timeout Counter.
- Slot Time Period Counter.
- Collision Number Counter.
- Exponential Backoff Shift Register.
- Exponential Backoff Mask Logic.
- Timer Trigger Logic.

This procedure checks the operation of the Backoff block, which resides in the serial side and is not easily controlled. The Diagnose command is performed in two phases.

The format of the 82596 Diagnose command is:

82586 and 32-Bit Segmented Modes

31													16 15																0
ODD WORD																EVEN WORD												
EL	S	I	X	X	X	X	X	X	X	X	X	X	1	1	1	C	B	OK	0	F	0	0	0	0	0	0	0	0	0	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	A15					LINK OFFSET									A0

Linear Mode

31													16 15																0
ODD WORD																EVEN WORD												
EL	S	I	0	0	0	0	0	0	0	0	0	0	1	1	1	C	B	OK	0	F	0	0	0	0	0	0	0	0	0	0
A31																					LINK ADDRESS									A0

Figure 36. Diagnose

where:

LINK ADDRESS, EL, B, C, I, S	— As per standard Command Block (see the NOP command for details).
Bits 19–28	— Reserved (0 in the 32-bit Segmented and Linear Modes).
CMD (bits 16–18)	— The Diagnose command. Value: 7h.
OK (bit 13)	— Indicates error free completion.
F (bit 11)	— Indicates that the self-test procedure has failed.

RECEIVE FRAME DESCRIPTOR

Each received frame is described by one Receive Frame Descriptor (see Figure 37). Two new memory structures are available for the received frames. The structures are available only in the Linear and 32-bit Segmented modes.

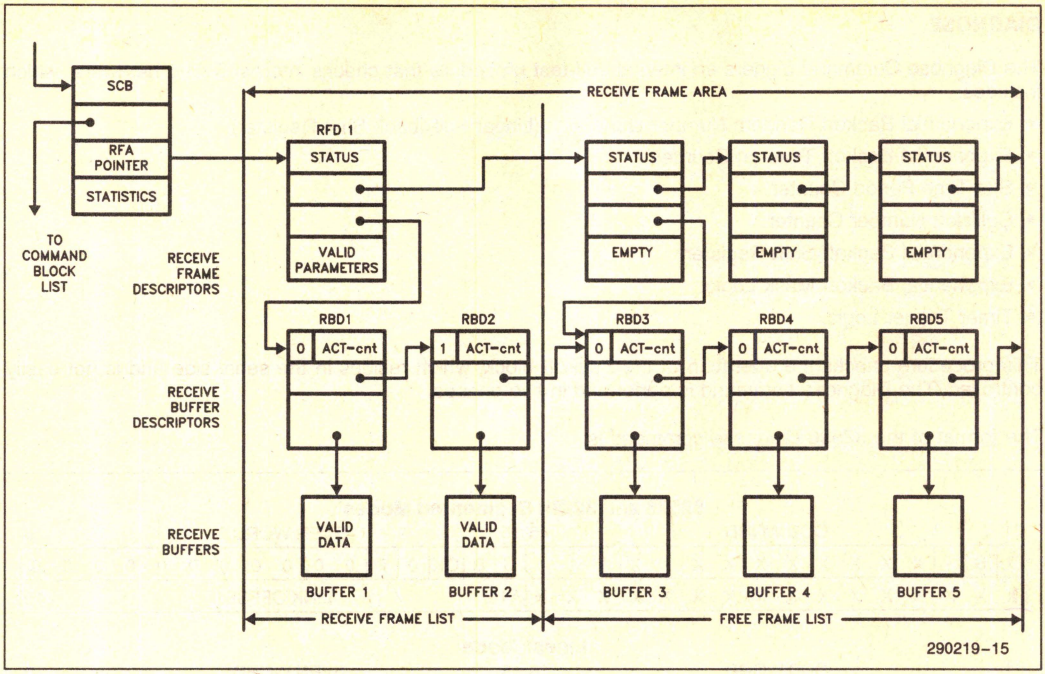


Figure 37. The Receive Frame Area

Simplified Memory Structure

The first is the Simplified memory structure, the data section of the received frame is part of the RFD and is located immediately after the Length Field. Receive Buffer Descriptors are not used with the Simplified structure, it is primarily used to make programming easier. If the length of the data area described in the Size Field is smaller than the incoming frame, the following happens.

1. The received frame is truncated.
2. The No Resource error counter is updated.
3. If the 82596 is configured to Save Bad Frames the RFD is not reused; otherwise, the same RFD is used to hold the next received frame, and the only action taken regarding the truncated frame is to update the counter.
4. The 82596 continues to receive the next frame in the next RFD.

Note that this sequence is very useful for monitoring. If the 82596 is configured to Save Bad Frames, to receive in Promiscuous mode, and to use the Simplified memory structure, any programmed length of received data can be saved in memory.

The Simplified memory structure is shown in Figure 38.

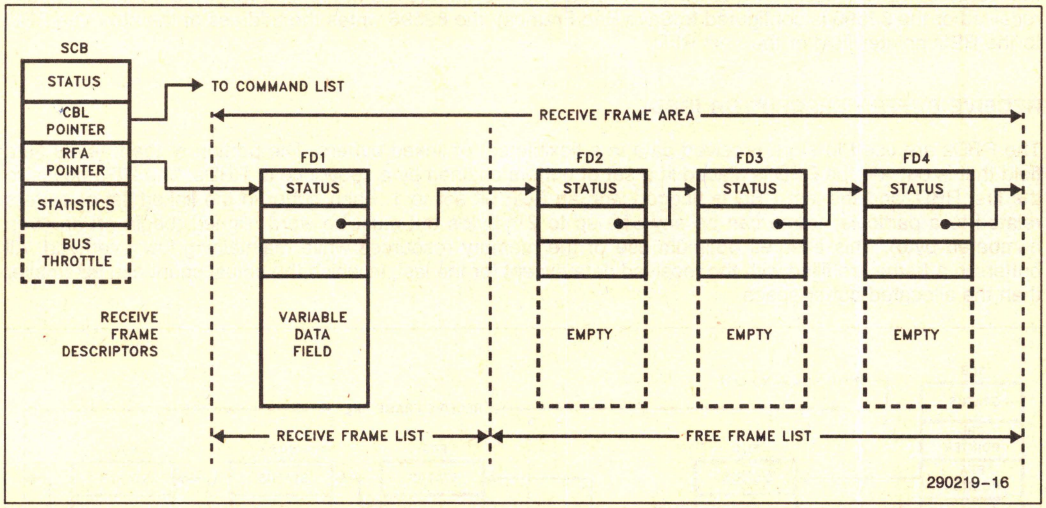


Figure 38. RFA Simplified Memory Structure

Flexible Memory Structure

The second structure is the Flexible memory structure, the data structure of the received frame is stored in both the RFD and in a linked list of Receive Buffers—Receive Buffer Descriptors. The received frame is placed in the RFD as configured in the Size field. Any remaining data is placed in a linked list of RBDs.

The Flexible memory structure is shown in Figure 39.

Buffers on the receive side can be different lengths. The 82596 will not place more bytes into a buffer than indicated in the associated RBD. The 82596 will fetch the next RBD before it is needed. The 82596 will attempt to receive frames as long as the FBL is not exhausted. If there are no more buffers, the 82596 Receive Unit will enter the No Resources state. Before starting the RU, the CPU must place the FBL pointer in the RBD pointer field of the first RFD. All remaining RBD pointer fields for subsequent RFDs should be "1s." If the Receive Frame Descriptor and the associated Receive Buffers are not reused (e.g., the frame is properly received or the 82596 is configured to Save Bad Frames), the 82596 writes the address of the next free RBD to the RBD pointer field of the next RFD.

RECEIVE BUFFER DESCRIPTOR (RBD)

The RBDs are used to store received data in a flexible set of linked buffers. The portion of the frame's data field that is outside the RFD is placed in a set of buffers chained by a sequence of RBDs. The RFD points to the first RBD, and the last RBD is flagged with an EOF bit set to 1. Each buffer in the linked list of buffers related to a particular frame can be any size up to 2^{14} bytes but must be word aligned (begin on an even numbered byte). This ensures optimum use of the memory resources while maintaining low overhead. All buffers in a frame are filled with the received data except for the last, in which the actual count can be smaller than the allocated buffer space.

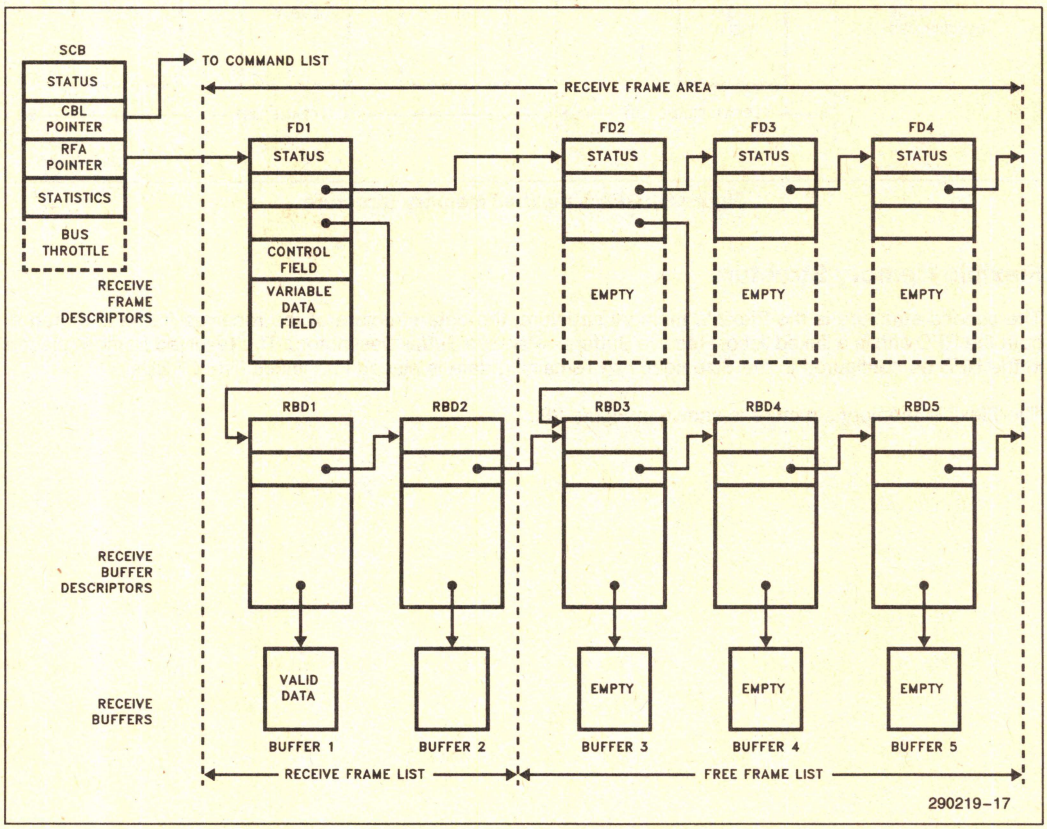


Figure 39. RFA Flexible Memory Structure

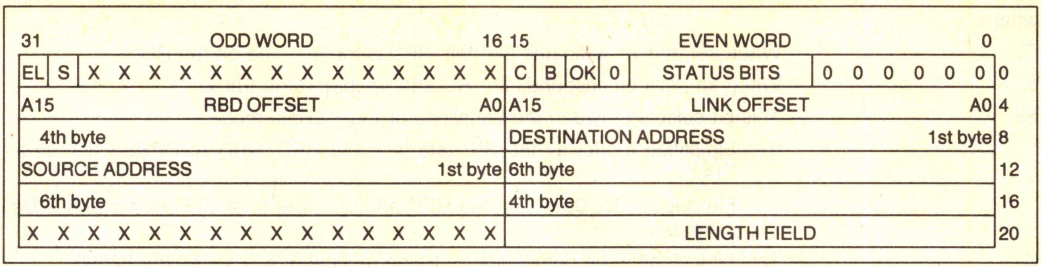


Figure 40. Receive Frame Descriptor—82586 Mode

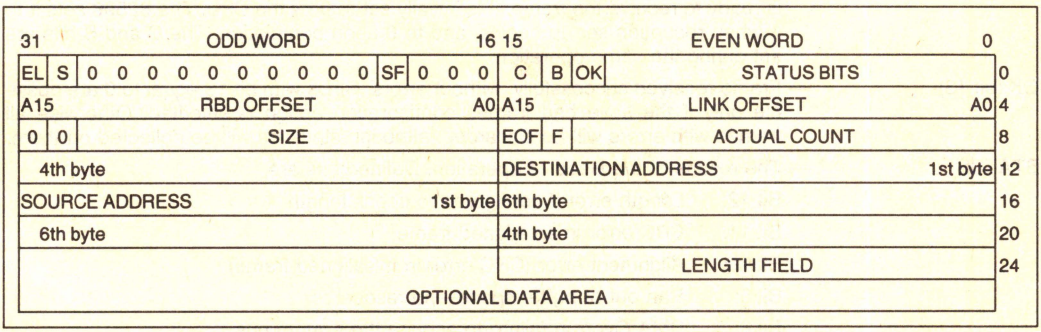


Figure 41. Receive Frame Descriptor—32-Bit Segmented Mode

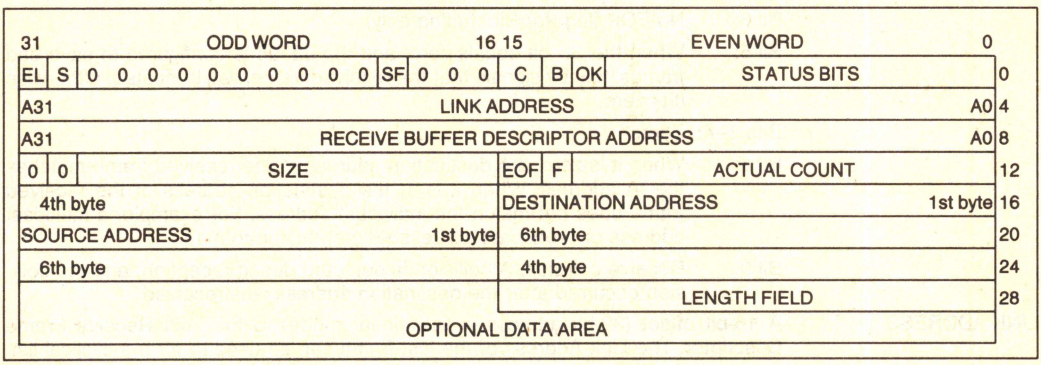


Figure 42. Receive Frame Descriptor—Linear Mode

where:

EL — When set, this bit indicates that this RFD is the last one on the RDL.

S — When set, this bit suspends the RU after receiving the frame.

SF — This bit selects between the Simplified or the Flexible mode.

0 — Simplified mode, all the RX data is in the RFD. RBD ADDRESS field is all "1s."

1 — Flexible mode. Data is in the RFD and in a linked list of Receive Buffer Descriptors.

C — This bit indicates the completion of frame reception. It is set by the 82596.

B — This bit indicates that the 82596 is currently receiving this frame, or that the 82596 is ready to receive the frame. It is initially set to 0 by the CPU. The 82596 sets it to 1 when reception set up begins, and to 0 upon completion. The C and B bits are set during the same operation.

OK (bit 13) — Frame received successfully, without errors. RFDs with bit 13 equal to 0 are possible only if the save bad frames configuration option is selected. Otherwise all frames with errors will be discarded, although statistics will be collected on them.

STATUS — The results of the Receive operation. Defined bits are,

Bit 12: Length error if configured to check length

Bit 11: CRC error in an aligned frame

Bit 10: Alignment error (CRC error in misaligned frame)

Bit 9: Ran out of buffer space—no resources

Bit 8: DMA Overrun failure to acquire the system bus.

Bit 7: Frame too short.

Bit 6: No EOP flag (for Bit stuffing only)

Bit 5: When the SF bit equals zero, and the 82596 is configured to save bad frames, this bit signals that the received frame was truncated. Otherwise it is zero.

Bits 2–4: Zeros

Bit 1: When it is zero, the destination address of the received frame matches the IA address. When it is 1, the destination address of the received frame does not match the individual address. For example, a multicast address or broadcast address will set this bit to a 1.

Bit 0: Receive collision. A collision is detected during reception, and the collision occurred after the destination address was received.

LINK ADDRESS — A 16-bit offset (32-bit address in the Linear mode) to the next Receive Frame Descriptor. The Link Address of the last frame can be used to form a cyclical list.

RBD POINTER — The offset (address in the Linear mode) of the first RBD containing the received frame data. An RBD pointer of all ones indicates no RBD.

EOF
F
SIZE
ACT COUNT — These fields are for the Simplified and Flexible memory models. They are exactly the same as the respective fields in the Receive Buffer Descriptor. See the next section for detailed explanation of their functions.

MC — Multicast bit.

DESTINATION ADDRESS — The contents of the destination address of the receive frame. The field is 0 to 6 bytes long.

SOURCE ADDRESS — The contents of the Source Address field of the received frame. It is 0 to 6 bytes long.

LENGTH FIELD — The contents of this 2-byte field are user defined. In 802.3 it contains the length of the data field. It is placed in memory in the same order it is received, i.e., most significant byte first, least significant byte second.

NOTES

1. The Destination address, Source address and Length fields are packed, i.e., one field immediately follows the next.
2. The affect of Address/Length Location (No Source Address Insertion) configuration parameter while receiving is as follows:

— 82586 Mode: The Destination address, Source address and Length field are not used, they are placed in the RX data buffers.

— 32-Bit Segmented and Linear Modes: when the Simplified memory model is used, the Destination address, Source address and Length fields reside in their respective fields in the RFD. When the Flexible memory strucrture is used the Destination address, Source address, and Length field locations depend on the SIZE field of the RFD. They can be placed in the RFD, in the RX data buffers, or partially in the RFD and the rest in the RX data buffers, depending on the SIZE field value.

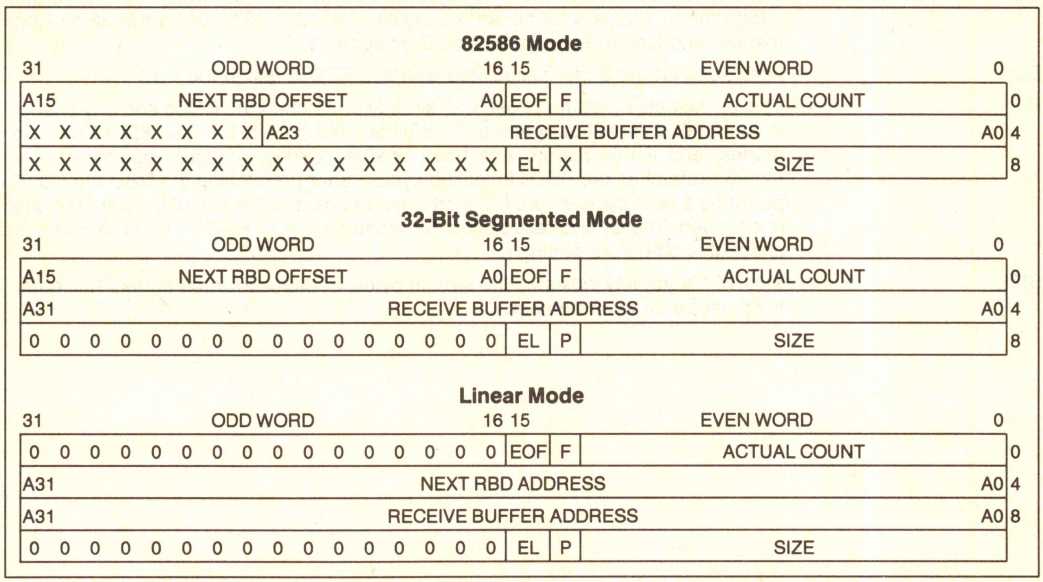


Figure 43. Receive Buffer Descriptor

where:

EOF — Indicates that this is the last buffer related to the frame. It is cleared by the CPU before starting the RU, and is written by the 82596 at the end of reception of the frame.

F — Indicates that this buffer has already been used. The Actual Count has no meaning unless the F bit equals one. This bit is cleared by the CPU before starting the RU, and is set by the 82596 after the associated buffer has been. This bit has the same meaning as the Complete bit in the RFD and CB.

ACT COUNT — This 14-bit quantity indicates the number of meaningful bytes in the buffer. It is cleared by the CPU before starting the RU, and is written by the 82596 after the associated buffer has already been used. In general, after the buffer is full, the Actual Count value equals the size field of the same buffer. For the last buffer of the frame, Actual Count can be less than the buffer size.

NEXT BD ADDRESS — The offset (absolute address in the Linear mode) of the next RBD on the list. It is meaningless if EL = 1.

BUFFER ADDRESS — The starting address of the memory area that contains the received data. In the 82586 mode, this is a 24-bit address (with pins A24–A31 = 0). In the 32-bit Segmented and Linear modes this is a 32-bit address.

EL — Indicates that the buffer associated with this RBD is last in the FBL.

P — This bit indicates that the 82596 has already prefetched the RBDs and any change in the RBD data will be ignored. This bit is valid only in the new 82596 memory modes, and if this feature has been enabled during configure command. The 82596 Prefetches the RBDs in locked cycles; after prefetching the RBD the 82596 performs a write cycle where the P bit is set to one and the rest of the data remains unchanged. The CPU is responsible for resetting it in all RBDs. The 82596 will not check this bit before setting it.

SIZE — This 14-bit quantity indicates the size, in bytes, of the associated buffer. This quantity must be an even number.

PGA PACKAGE THERMAL SPECIFICATION

Parameter	Thermal Resistance
θ_{JC}	3°C/W
θ_{JA}	24°C/W

ELECTRICAL AND TIMING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Case Temperature under Bias ... −65°C to +110°C

Supply Voltage
with Respect to V_{SS} ..... −0.5V to +6.5V

Voltage on Other Pins ..... −0.5V to V_{CC} + 0.5V

1

D.C. CHARACTERISTICS

T_C = 0°C to +85°C, V_{CC} = 5V ±10% CLK2 and LE/$\overline{BE}$ have MOS levels (see V_{MIL}, V_{MIH}).
All other signals have TTL levels (see V_{IL}, V_{IH}, V_{OL}, V_{OH}).

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage (TTL)	−0.3	+0.8	V	
V_{IH}	Input High Voltage (TTL)	2.0	V_{CC} + 0.3	V	
V_{MIL}	Input Low Voltage (MOS)	−0.3	+0.8	V	
V_{MIH}	Input High Voltage (MOS)	3.7	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage (TTL)		0.45	V	I_{OL} = 4.0 mA
V_{CIL}	$\overline{RxC}$, $\overline{TxC}$ Input Low Voltage	−0.5	0.6	V	
V_{CIH}	$\overline{RxC}$, $\overline{TxC}$ Input High Voltage	3.3	V_{CC} + 0.5	V	
V_{OH}	Output High Voltage (TTL)	2.4		V	I_{OH} = 0.9mA−1 mA
I_{LI}	Input Leakage Current		±15	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±15	μA	$0.45 < V_{OUT} < V_{CC}$
C_{IN}	Capacitance of Input Buffer		10	pF	FC = 1 MHz
C_{OUT}	Capacitance of Input/Output Buffer		12	pF	FC = 1 MHz
C_{CLK}	CLK Capacitance		20	pF	FC = 1 MHz
I_{CC}	Power Supply		150	mA	At 20 MHz for the 82596SX I_{CC} Typical = 90 mA
I_{CC}	Power Supply		200	mA	At 25 MHz I_{CC} Typical = 100 mA
I_{CC}	Power Supply		300	mA	At 33 MHz I_{CC} Typical = 150 mA

A.C. CHARACTERISTICS

82596DX C-STEP INPUT/OUTPUT SYSTEM TIMINGS $T_C = 0°C$ to $+85°$, $V_{CC} = 5V \pm 10\%$

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	25 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	25 MHz	CLK2/2
T1	CLK2 Period	20	40	
T2	CLK2 High	4		3.7V
T3	CLK2 Low	5		0.8V
T4	CLK2 Rise Time	—	7	0.8V to 3.7V
T5	CLK2 Fall Time	—	7	3.7V to 0.8V
T13	CA and BREQ Setup Time	7		1, 2, 3
T14	BREQ Hold Time	3		1, 2, 3
T14a	CA Hold Time	5		1, 2, 3
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	4 T1		3
T25	INT Valid Delay	1	26	
T6	$\overline{BEx}$ Valid Delay	3	17	
T6b	$\overline{LOCK}$ Valid Delay	3	21	
T6c	A2–A31 Valid Delay	3	18	
T7	$\overline{BEx}$, $\overline{LOCK}$, and A2–A31 Float Delay	4	30	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	21	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	4	30	
T10	D0–D31 Write Data Valid Delay	3	19	
T11	D0–D31 Write Data Float Delay	4	22	
T27	D0–D31 CPU $\overline{PORT}$ Access Setup Time	7		2
T28	D0–D31 CPU $\overline{PORT}$ Access Hold Time	5		2
T29	$\overline{PORT}$ Setup Time	7		2
T30	$\overline{PORT}$ Hold Time	3		2
T17	$\overline{RDY}$ Setup Time	9		2
T18	$\overline{RDY}$ Hold Time	3		2
T19	D0–D31 READ Setup Time	7		2
T20	D0–D31 READ Hold Time	5		2
T12	HOLD Valid Delay	3	22	
T21	HLDA Setup Time	10		1, 2
T22a	HLDA Hold Time	3		1, 2
T23	RESET Setup Time	10		2
T24	RESET Hold Time	3		2

NOTE:
Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

A.C. CHARACTERISTICS (Continued)

82596DX C-STEP INPUT/OUTPUT SYSTEM TIMINGS T_C = 0°C to +85°C, V_{CC} = 5V ±5%

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	33 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	33 MHz	CLK2/2
T1	CLK2 Period	15	40	
T2	CLK2 High	4.5		3.7V
T3	CLK2 Low	4.5		0.8V
T4	CLK2 Rise Time	—	4	3.7V to 0.8V
T5	CLK2 Fall Time	—	4	0.8V to 3.7V
T13	CA and BREQ Setup Time	7		1, 2, 3
T14	BREQ Hold Time	3		1, 2, 3
T14a	CA Hold Time	5		1, 2, 3
T26	CA and BREQ, $\overline{\text{PORT}}$ Pulse Width	4 T1		3
T25	INT Valid Delay	1	20	
T6	$\overline{\text{BEx}}$ Valid Delay	3	17	
T6b	$\overline{\text{LOCK}}$ Valid Delay	3	16	
T6c	A2–A31 Valid Delay	3	18	
T7	$\overline{\text{BEx}}$, $\overline{\text{LOCK}}$, and A2–A31 Float Delay	4	20	
T8	W/$\overline{\text{R}}$ and $\overline{\text{ADS}}$ Valid Delay	3	16	
T9	W/$\overline{\text{R}}$ and $\overline{\text{ADS}}$ Float Delay	4	20	
T10	D0–D31 Write Data Valid Delay	3	19	
T11	D0–D31 Write Data Float Delay	4	17	
T27	D0–D31 CPU $\overline{\text{PORT}}$ Access Setup Time	5		2
T28	D0–D31 CPU $\overline{\text{PORT}}$ Access Hold Time	3		2
T29	$\overline{\text{PORT}}$ Setup Time	7		2
T30	$\overline{\text{PORT}}$ Hold Time	3		2
T17	$\overline{\text{RDY}}$ Setup Time	8		2
T18	$\overline{\text{RDY}}$ Hold Time	3		2
T19	D0–D31 READ Setup Time	5.5		2
T20	D0–D31 READ Hold Time	4		2
T12	HOLD Valid Delay	3	19	
T21	HLDA Setup Time	8		1, 2
T22a	HLDA Hold Time	3		1, 2
T23	RESET Setup Time	9		2
T24	RESET Hold Time	3		2

NOTE:
Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

A.C. CHARACTERISTICS (Continued)

82596SX C-STEP INPUT/OUTPUT SYSTEM TIMINGS $T_C = 0°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	20 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	20 MHz	CLK2/2
T1	CLK2 Period	25	40	
T2	CLK2 High	8		at 2.0V
T3	CLK2 Low	8		at 2.0V
T4	CLK2 Rise Time	—	8	0.8V to 3.7V
T5	CLK2 Fall Time	—	8	3.7V to 0.8V
T13	CA and BREQ Setup Time	10		1, 2, 3
T14	BREQ Hold Time	7		1, 2, 3
T14a	CA Hold Time	8		1, 2, 3
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	4 T1		3
T25	INT Valid Delay	1	35	
T6	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$, BON, and A1–A31 Valid Delay	3	30	
T7	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$, BON, and A1–A31 Float Delay	4	30	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	3	26	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	4	30	
T10	D0–D15 Write Data Valid Delay	3	38	
T11	D0–D15 Write Data Float Delay	4	27	
T27	D0–D15 CPU $\overline{PORT}$ Access Setup Time	9		2
T28	D0–D15 CPU $\overline{PORT}$ Access Hold Time	6		2
T29	$\overline{PORT}$ Setup Time	10		2
T30	$\overline{PORT}$ Hold Time	7		2
T17	$\overline{RDY}$ Setup Time	12		2
T18	$\overline{RDY}$ Hold Time	4		2
T19	D0–D15 READ Setup Time	9		2
T20	D0–D15 READ Hold Time	5		2
T12	HOLD Valid Delay	3	28	
T21	HLDA Setup Time	15		1, 2
T22a	HLDA Hold Time	7		1, 2
T23	RESET Setup Time	12		1, 2
T24	RESET Hold Time	4		1, 2

NOTE:
Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.

A.C. CHARACTERISTICS (Continued)

82596SX C-STEP INPUT/OUTPUT SYSTEM TIMINGS T_C = 0°C to +85°C, V_{CC} = 5V ±10%

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	16 MHz		Notes
		Min	Max	
	Operating Frequency	12.5 MHz	16 MHz	CLK2/2
T1	CLK2 Period	31	40	
T2	CLK2 High	9		2.0V
T3	CLK2 Low	9		2.0V
T4	CLK2 Rise Time	—	8	0.8V to 3.7V
T5	CLK2 Fall Time	—	8	3.7V to 0.8V
T13	CA and BREQ Setup Time	11		1, 2, 3
T14	CA and BREQ Hold Time	8		1, 2, 3
T26	CA and BREQ, $\overline{PORT}$ Pulse Width	4 T1		3
T25	INT Valid Delay	1	40	
T6	$\overline{BHE}$, $\overline{BLE}$, BON, and A1–A31 Valid Delay	3	36	
T6b	LOCK# Valid Delay	1	33	
T7	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$, BON, and A1–A31 Float Delay	4	40	
T8	W/$\overline{R}$ and $\overline{ADS}$ Valid Delay	1	33	
T9	W/$\overline{R}$ and $\overline{ADS}$ Float Delay	4	35	
T10	D0–D15 Write Data Valid Delay	3	40	
T11	D0–D15 Write Data Float Delay	4	35	
T27	D0–D15 CPU $\overline{PORT}$ Access Setup Time	9		2
T28	D0–D15 CPU $\overline{PORT}$ Access Hold Time	6		2
T29	$\overline{PORT}$ Setup Time	11		2
T30	$\overline{PORT}$ Hold Time	8		2
T17	$\overline{RDY}$ Setup Time	19		2
T18	$\overline{RDY}$ Hold Time	6		2
T19	D0–D15 READ Setup Time	9		2
T20	D0–D15 READ Hold Time	6		2
T12	HOLD Valid Delay	2	33	

A.C. CHARACTERISTICS (Continued)

82596SX C-STEP INPUT/OUTPUT SYSTEM TIMINGS T_C = 0°C to +85°C, V_{CC} = 5V ±10% (Continued)

These timings assume the C_L on all outputs is 50 pF unless otherwise specified. C_L can be 20 pF to 120 pF, however, timings must be derated.
All timing requirements are given in nanoseconds.

Symbol	Parameter	16 MHz		Notes
		Min	Max	
T21	HLDA Setup Time	15		1, 2
T22a	HLDA Hold Time	7		1, 2
T23	RESET Setup Time	13		1, 2
T24	RESET Hold Time	4		1, 2

NOTES:
Timings shown are for the 82596CA C-Stepping. For information regarding timings for the 82596CA A1 or B-Step, contact your local Intel representative.
1. RESET, HLDA, and CA are internally synchronized. This timing is to guarantee recognition at next clock for RESET, HLDA, and CA.
2. All set-up, hold, and delay timings are at the maximum frequency specification Fmax, and must be derated according to the following equation for operation at lower frequencies:
   Tderated = (Fmax/Fopr) × T
   where:
   Tderated = Specifies the value to derate the specification.
   Fmax = Maximum operating frequency.
   Fopr = Actual operating frequency.
   T = Specification at maximum frequency.
This calculation only provides a rough estimate for derating the frequency. For more detailed information contact your Intel sales office for the data sheet supplement.
3. CA is internally synchronized; if the setup and hold times are met then CA needs to be only 2 T1. BREQ and $\overline{\text{PORT}}$ are not internally synchronized. BREQ must meet setup and hold times and need only be 2 T1 wide.

TRANSMIT/RECEIVE CLOCK PARAMETERS

Symbol	Parameter	20 MHz		Notes
		Min	Max	
T36	$\overline{TxC}$ Cycle	50		1, 3
T38	$\overline{TxC}$ Rise Time		5	1
T39	$\overline{TxC}$ Fall Time		5	1
T40	$\overline{TxC}$ High Time	19		1, 3
T41	$\overline{TxC}$ Low Time	18		1, 3
T42	TxD Rise Time		10	4
T43	TxD Fall Time		10	4
T44	TxD Transition	20		2, 4
T45	$\overline{TxC}$ Low to TxD Valid		25	4, 6
T46	$\overline{TxC}$ Low to TxD Transition		25	2, 4
T47	$\overline{TxC}$ High to TxD Transition		25	2, 4
T48	$\overline{TxC}$ Low to TxD High (At End of Transition)		25	4
$\overline{RTS}$ AND $\overline{CTS}$ PARAMETERS				
T49	$\overline{TxC}$ Low to $\overline{RTS}$ Low, Time to Activate $\overline{RTS}$		25	5
T50	$\overline{CTS}$ Low to $\overline{TxC}$ Low, $\overline{CTS}$ Setup Time		20	
T51	$\overline{TxC}$ Low to $\overline{CTS}$ Invalid, $\overline{CTS}$ Hold Time	10		7
T52	$\overline{TxC}$ Low to $\overline{RTS}$ High		25	5
RECEIVE CLOCK PARAMETERS				
T53	$\overline{RxC}$ Cycle	50		1, 3
T54	$\overline{RxC}$ Rise Time		5	1
T55	$\overline{RxC}$ Fall Time		5	1
T56	$\overline{RxC}$ High Time	19		1
T57	$\overline{RxC}$ Low Time	18		1
RECEIVED DATA PARAMETERS				
T58	RxD Setup Time	20		6
T59	RxD Hold Time	10		6

TRANSMIT/RECEIVE CLOCK PARAMETERS (Continued)

Symbol	Parameter	20 MHz		Notes
		Min	Max	
RECEIVED DATA PARAMETERS (Continued)				
T60	RxD Rise Time		10	
T61	RxD Fall Time		10	
$\overline{\text{CRS}}$ AND $\overline{\text{CDT}}$ PARAMETERS				
T62	$\overline{\text{CDT}}$ Low to $\overline{\text{TxC}}$ HIGH External Collision Detect Setup Time	20		
T63	$\overline{\text{TxC}}$ High to $\overline{\text{CDT}}$ Inactive, $\overline{\text{CDT}}$ Hold Time	10		
T64	$\overline{\text{CDT}}$ Low to Jam Start			10
T65	$\overline{\text{CRS}}$ Low to $\overline{\text{TxC}}$ High, Carrier Sense Setup Time	20		
T66	$\overline{\text{TxC}}$ High to $\overline{\text{CRS}}$ Inactive, $\overline{\text{CRS}}$ Hold Time	10		
T67	$\overline{\text{CRS}}$ High to Jamming Start, (Internal Collision Detect)			12
T68	Jamming Period			11
T69	$\overline{\text{CRS}}$ High to $\overline{\text{RxC}}$ High, $\overline{\text{CRS}}$ Inactive Setup Time	30		
T70	$\overline{\text{RxC}}$ High to $\overline{\text{CRS}}$ High, $\overline{\text{CRS}}$ Inactive Hold Time	10		
INTERFRAME SPACING PARAMETERS				
T71	Interframe Delay			9
EXTERNAL LOOPBACK-PIN PARAMETERS				
T72	$\overline{\text{TxC}}$ Low to $\overline{\text{LPBK}}$ Low		T36	4
T73	$\overline{\text{TxC}}$ Low to $\overline{\text{LPBK}}$ High		T36	4

NOTES:
1. Special MOS levels, V_{CIL} = 0.9V and V_{CIH} = 3.0V.
2. Manchester only.
3. Manchester. Needs 50% duty cycle.
4. 1 TTL load + 50 pF.
5. 1 TTL load + 100 pF.
6. NRZ only.
7. Abnormal end of transmission—CTS expires before RTS.
8. Normal end to transmission.
9. Programmable value:
   T71 = N_{IFS} • T36
   where: N_{IFS} = the IFS configuration value
   (if N_{IFS} is less than 12 then N_{IFS} is forced to 12).
10. Programmable value:
    T64 = (N_{CDF} • T36) + x • T36
    (If the collision occurs after the preamble)
    where:
    N_{CDF} = the collision detect filter configuration value, and
    x = 12, 13, 14, or 15
11. T68 = 32 • T36
12. Programmable value:
    T67 = (N_{CSF} • T36) + x • T36
    where: N_{CSF} = the Carrier Sense Filter configuration value, and
    x = 12, 13, 14, or 15
13. To guarantee recognition on the next clock.

82596DX/SX BUS OPERATION

The following figures show thae basic bus cycles for the 82596DX and 82596SX.

For more details refer to the *32-Bit LAN Components Manual.*

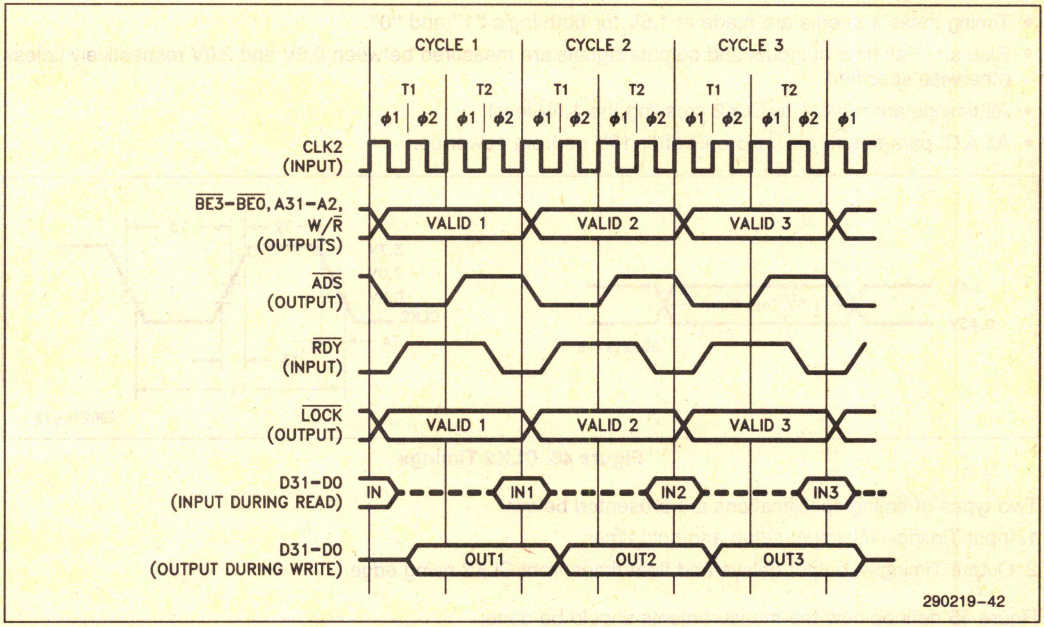


Figure 44. Basic 82596DX Bus Cycles

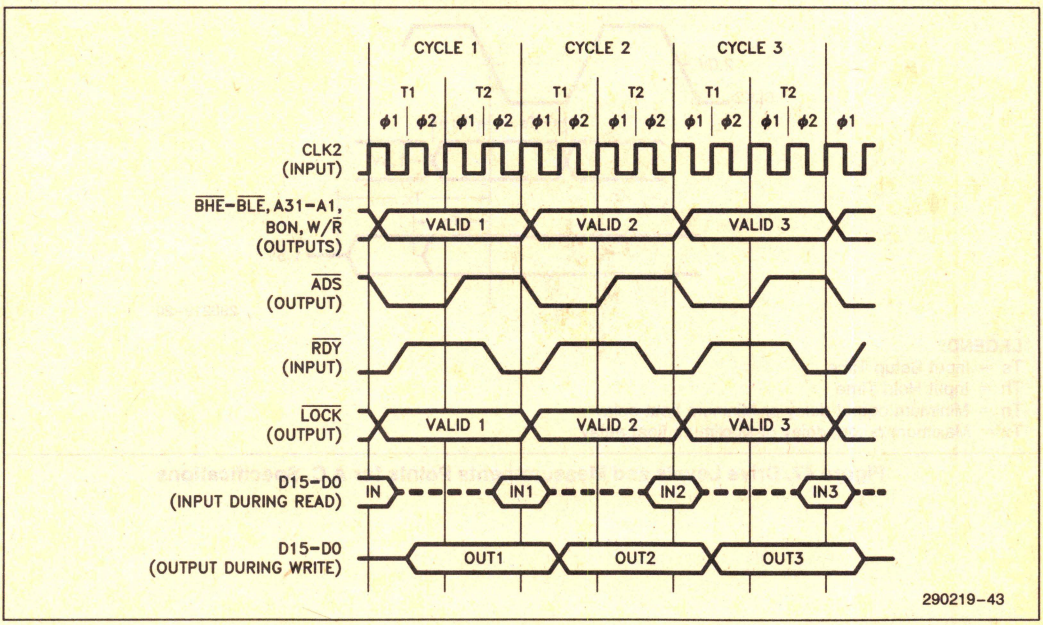
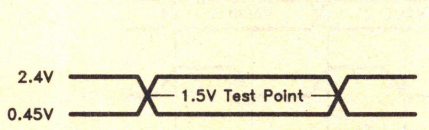


Figure 45. Basic 82596SX Bus Cycles

SYSTEM INTERFACE A.C. TIMING CHARACTERISTICS

The measurements should be done at:

- T_C = 0°C–85°C, V_{CC} = 5V ±10%, C = 50 pF unless otherwise specified.
- A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
- Timing measurements are made at 1.5V for both logic "1" and "0".
- Rise and Fall time of inputs and outputs signals are measured between 0.8V and 2.0V respectively unless otherwise specified.
- All timings are relative to CLK2 crossing the 1.5V level.
- All A.C. parameters are valid only after 100 μs from power up.



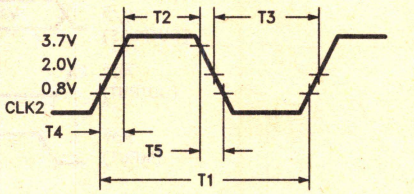
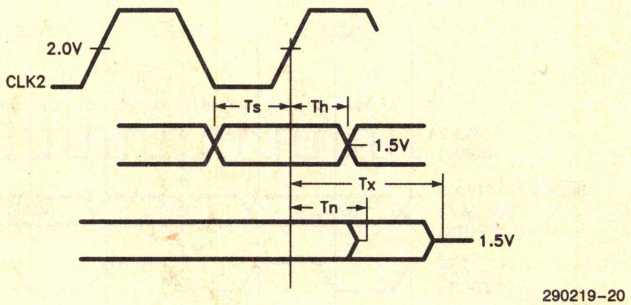


Figure 46. CLK2 Timings

Two types of timing specifications are presented below:

1. Input Timing—minimum setup and hold times.
2. Output Timings—output delays and float times from CLK2 rising edge.

Figure 45 defines how the measurements should be done:



LEGEND:
Ts = Input Setup Time
Th = Input Hold Time
Tn = Minimum output delay or Mininum float delay
Tx = Maximum output delay or Maximum float delay

Figure 47. Drive Levels and Measurements Points for A.C. Specifications

INPUT WAVEFORMS

Ts = T13, T15, T17, T19, T21, T23, T27, T29, T31
Th = T14, T16, T18, T20, T22, T22a, T24, T28, T30, T32

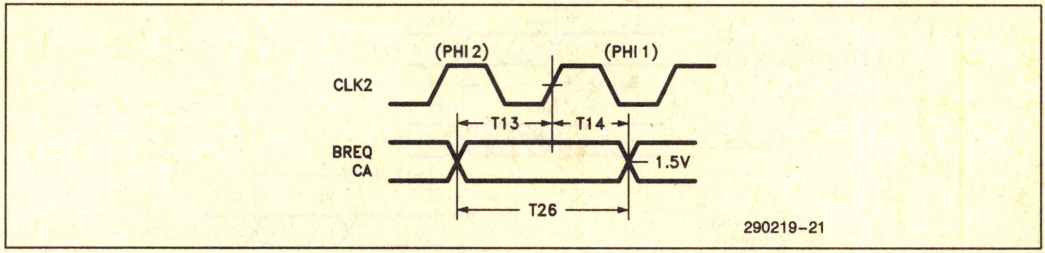


Figure 48. CA and BREQ Input Timing

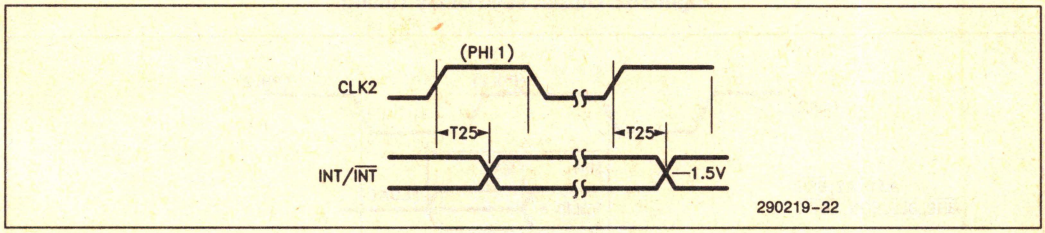


Figure 49. INT/$\overline{\text{INT}}$ Output Timing

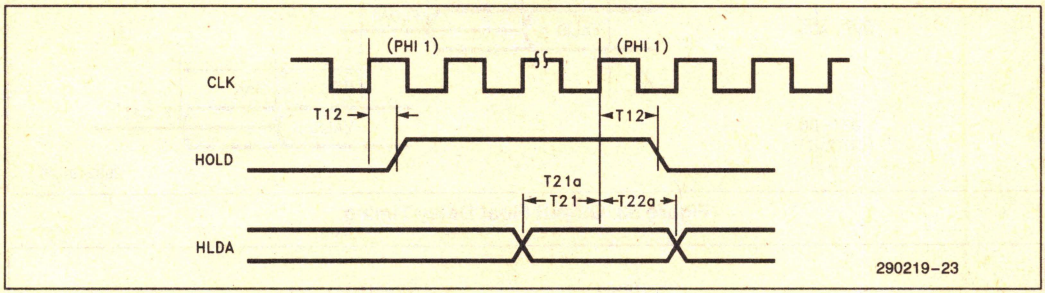


Figure 50. HOLD/HLDA Timings

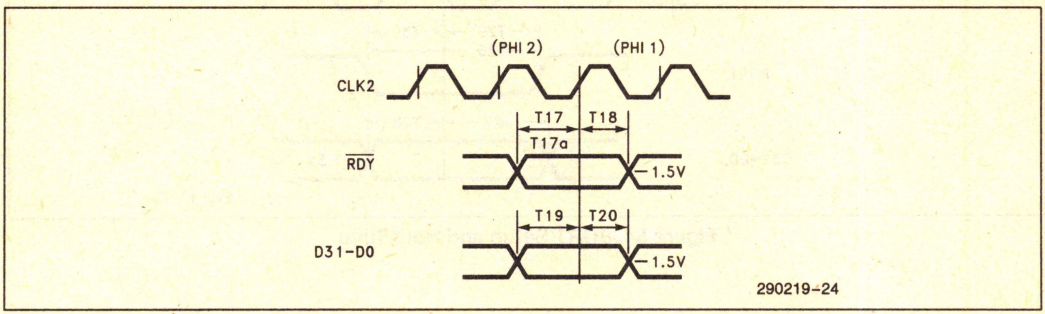


Figure 51. Input Setup and Hold Time

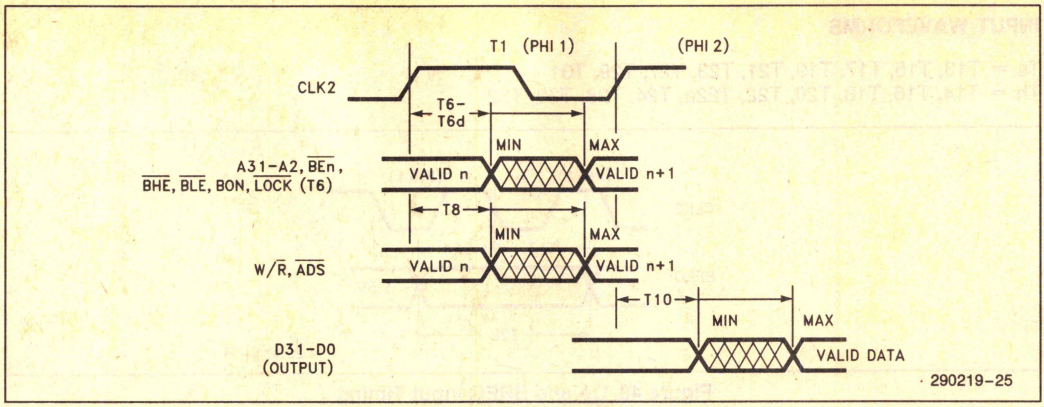


Figure 52. Output Valid Delay Timing

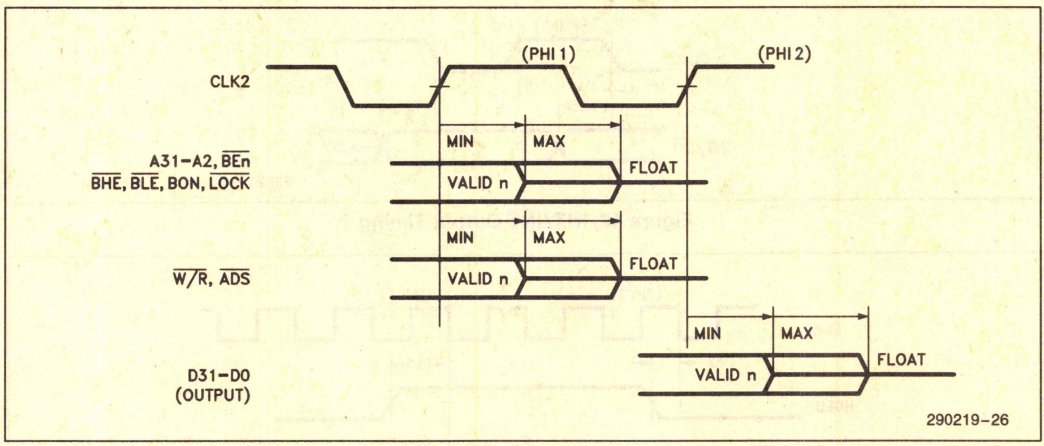


Figure 53. Output Float Delay Timing

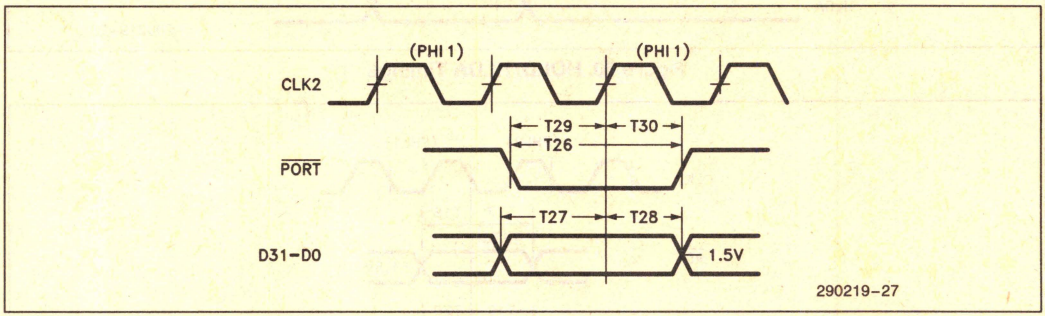


Figure 54. PORT Setup and Hold Time

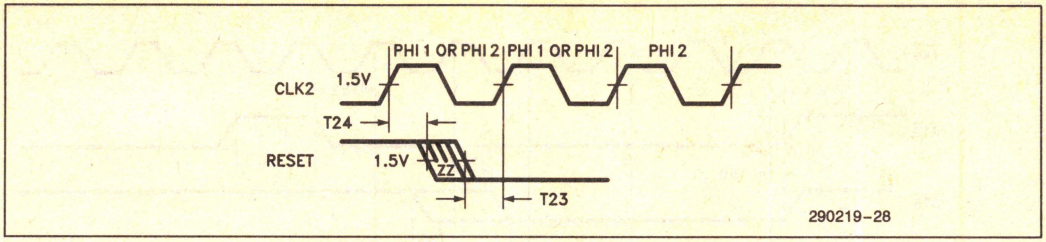


Figure 55. RESET Input Timing

SERIAL A.C. TIMING CHARACTERISTICS

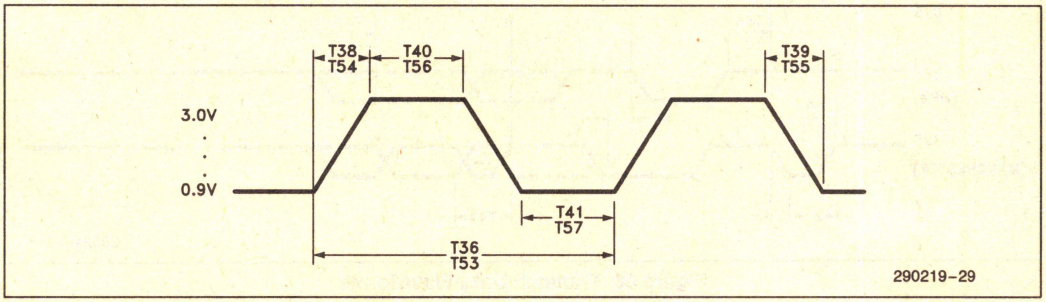


Figure 56. Serial Input Clock Timing

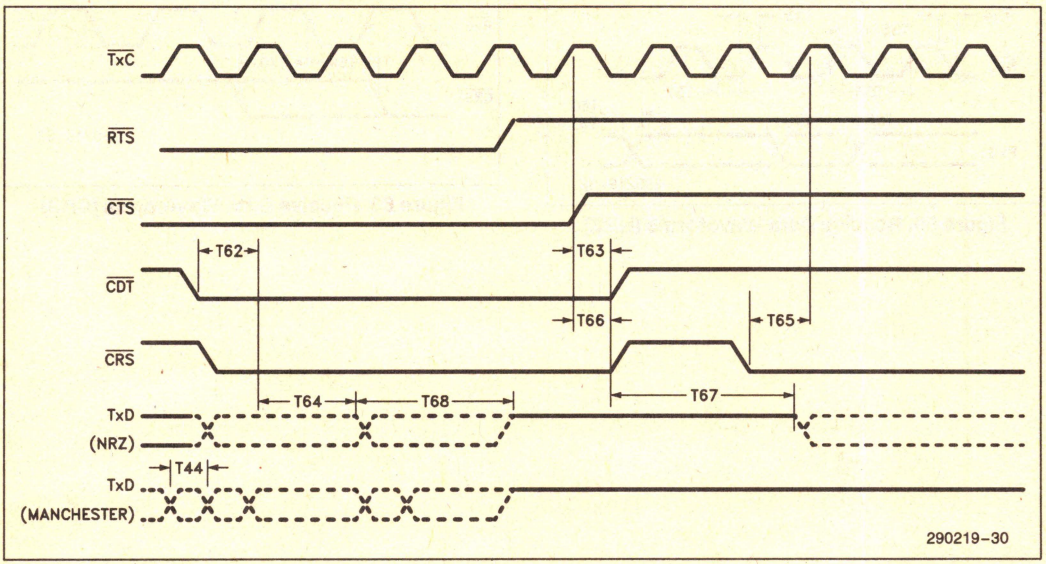


Figure 57. Transmit Data Waveforms

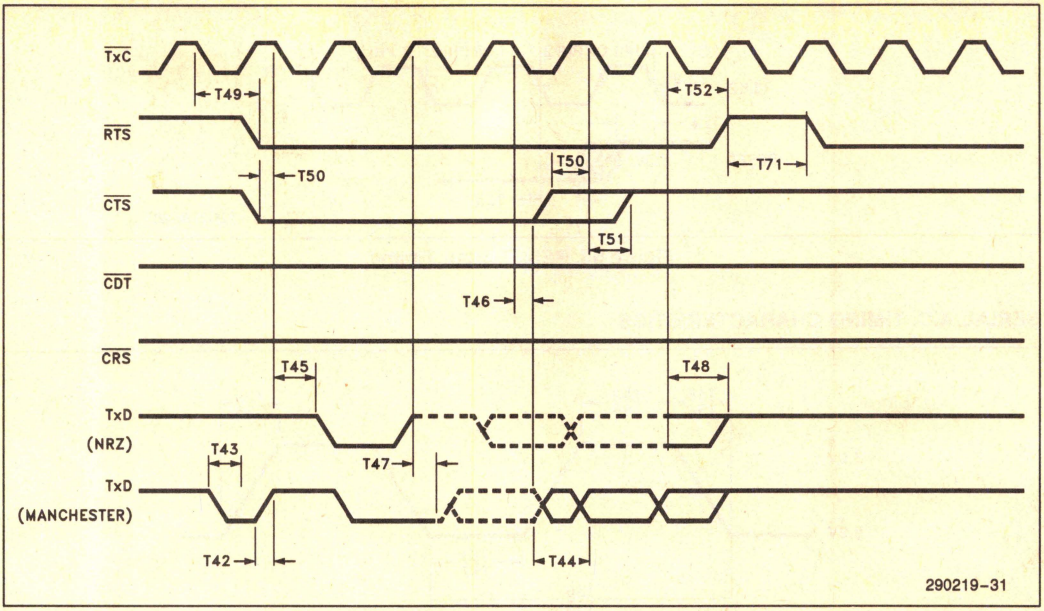


Figure 58. Transmit Data Waveforms

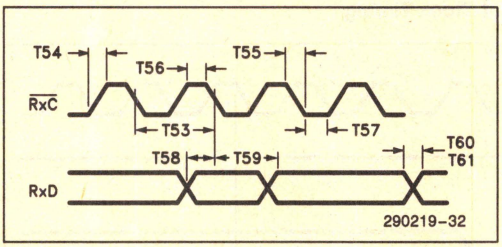


Figure 59. Receive Data Waveforms (NRZ)

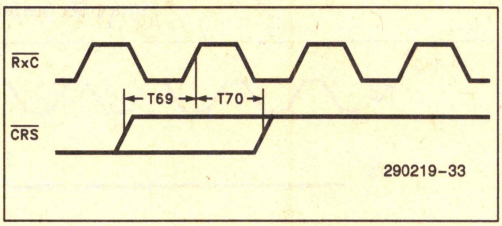
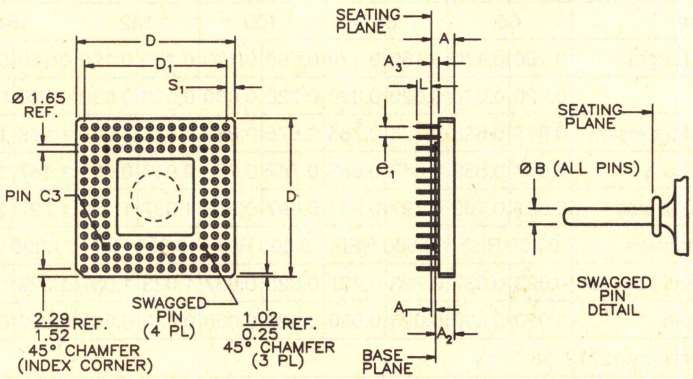


Figure 60. Receive Data Waveforms (CRS)

OUTLINE DIAGRAMS

132 LEAD CERAMIC PIN GRID ARRAY PACKAGE INTEL TYPE A



290219-36

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.76	1.27	Solid Lid	0.030	0.050	Solid Lid
A_2	2.67	3.43	Solid Lid	0.105	0.135	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	36.45	37.21		1.435	1.465	
D_1	32.89	33.15		1.295	1.305	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	132			132		
S_1	1.27	2.54		0.050	0.100	
ISSUE	IWS 10/12/88					

Intel Case Outline Drawings
Plastic Quad Flat Pack (PQFP)
0.025 Inch (0.635mm) Pitch

Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170	0.160	0.170
A1	Standoff	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
D, E	Terminal Dimension	0.675	0.685	0.775	0.785	0.875	0.885	1.075	1.085	1.275	1.285	1.475	1.485
D1, E1	Package Body	0.547	0.553	0.647	0.653	0.747	0.753	0.947	0.953	1.147	1.153	1.347	1.353
D2, E2	Bumper Distance	0.697	0.703	0.797	0.803	0.897	0.903	1.097	1.103	1.297	1.303	1.497	1.503
D3, E3	Lead Dimension	0.400 REF		0.500 REF		0.600 REF		0.800 REF		1.000 REF		1.200 REF	
D4, E4	Foot Radius Location	0.623	0.637	0.723	0.737	0.823	0.837	1.023	1.037	1.223	1.237	1.423	1.437
L1	Foot Length	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030	0.020	0.030
Issue	IWS Preliminary 12/12/88												INCH

Symbol	Description	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
N	Leadcount	68		84		100		132		164		196	
A	Package Height	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32	4.06	4.32
A1	Standoff	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
D, E	Terminal Dimension	17.15	17.40	19.69	19.94	22.23	22.48	27.31	27.56	32.39	32.64	37.47	37.72
D1, E1	Package Body	13.89	14.05	16.43	16.59	18.97	19.13	24.05	24.21	29.13	29.29	34.21	34.37
D2, E2	Bumper Distance	17.70	17.85	20.24	20.39	22.78	22.93	27.86	28.01	32.94	33.09	38.02	38.18
D3, E3	Lead Dimension	10.16 REF		12.70 REF		15.24 REF		20.32 REF		25.40 REF		30.48 REF	
D4, E4	Foot Radius Location	15.82	16.17	18.36	18.71	21.25	21.25	25.89	26.33	31.06	31.41	36.14	36.49
L1	Foot Length	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76	0.51	0.76
Issue	IWS Preliminary 12/12/88												mm

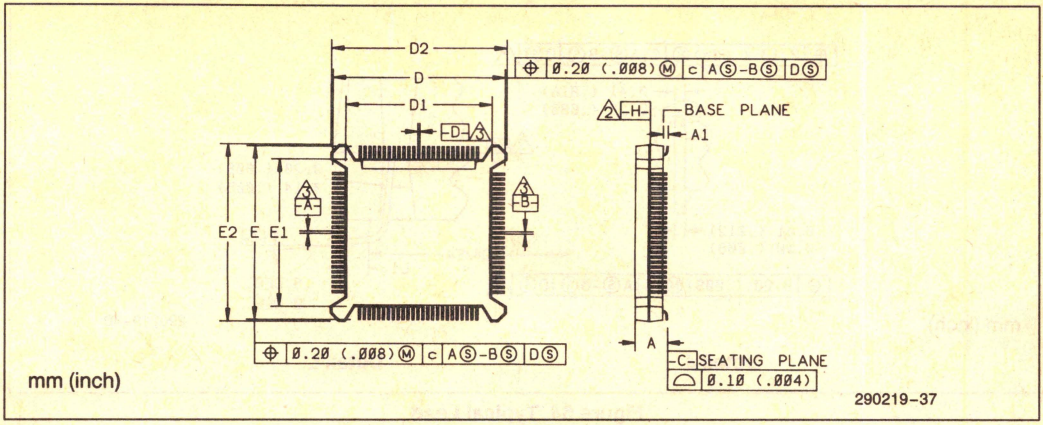


Figure 61. Principal Dimensions and Datums

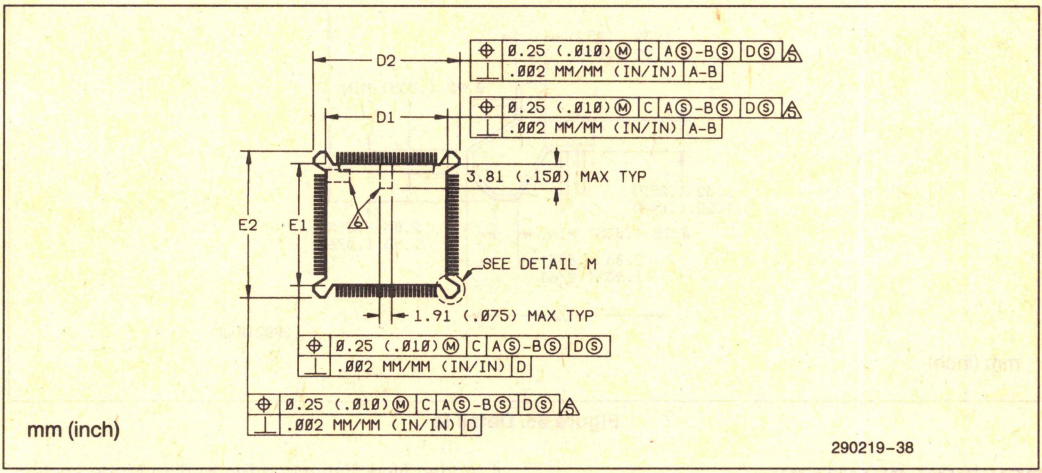


Figure 62. Molded Details

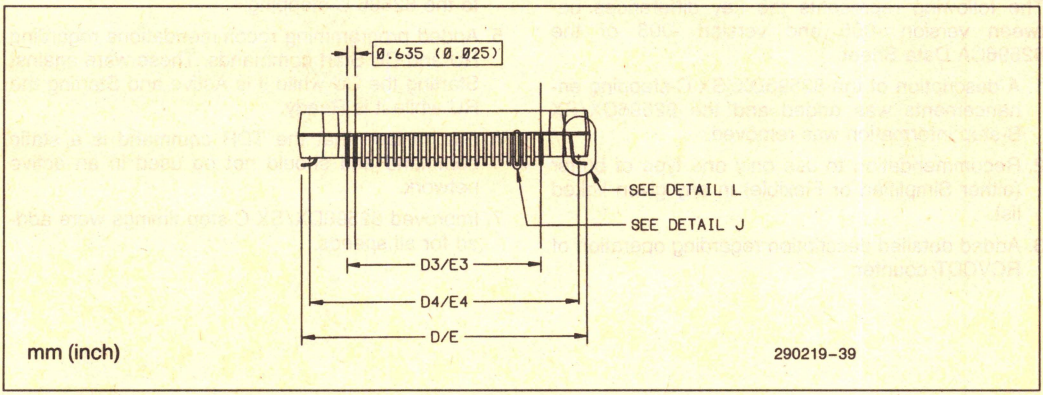


Figure 63. Terminal Details

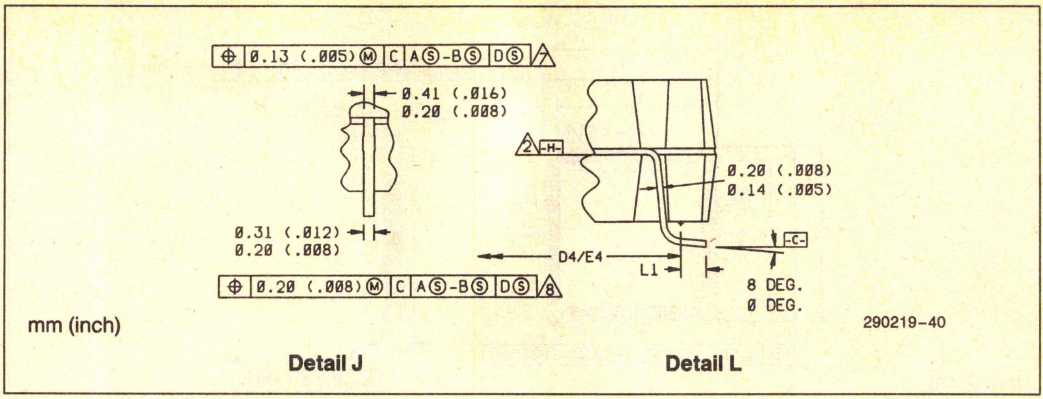


Figure 64. Typical Lead

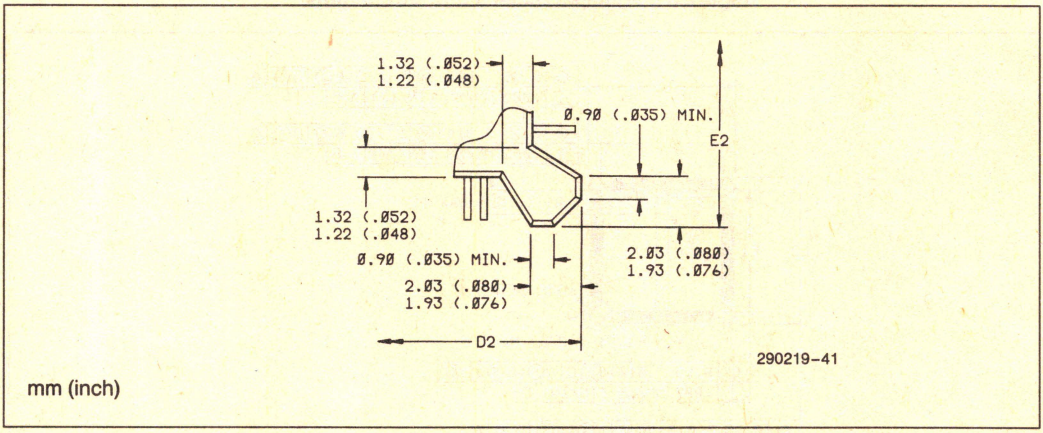


Figure 65. Detail M

REVISION SUMMARY

The following represents the key differences between version -005 and version -006 of the 82596CA Data Sheet.

1. A description of the 82596DX/SX C-stepping enhancements was added and the 82596DX/SX B-step information was removed.
2. Recommendation to use only one type of buffer (either Simplified or Flexible) in any given linked list.
3. Added detailed description regarding operation of RCVCDT counter.
4. Added New Enhanced Big Endian Mode section. The New Enhanced Big Endian Mode applies only to the 82596 C-stepping.
5. Added programming recommendations regarding RU and CU Start commands. These warn against Starting the CU while it is Active and Starting the RU while it is Ready.
6. Emphasized that the TDR command is a static command and should not be used in an active network.
7. Improved 82596DX/SX C-step timings were added for all speeds.

82C501AD
ETHERNET SERIAL INTERFACE

- **CHMOS Replacement for Intel 82C501, 82501, or SEEQ 8023A**
- **Conforms to IEEE 802.3 10BASE5 (Ethernet) and 10BASE2 (Cheapernet) Specifications**
- **Direct Interface to Intel LAN Controllers and the Attachment Unit Interface (Transceiver) Cable**
- **10-Mb/s Operation**
- **Manchester Encoding/Decoding and Receive Clock Recovery**
- **10-MHz Transmit Clock Generator**
- **Drives/Receives 802.3 AUI Cables**
- **Defeatable Watchdog Timer Circuit to Prevent Continuous Transmission**
- **Diagnostic Loopback for Network Node Fault Detection and Isolation**

1

The 82C501AD Ethernet Serial Interface (ESI) chip is designed to work directly with Intel LAN Controllers (82586, 82590, and 82596) in IEEE 802.3 (10BASE5 and 10BASE2), 10-Mb/s, Local Area Network applications. The major functions of the 82C501AD are to generate the 10-MHz transmit clock for the Intel LAN Controller, perform Manchester encoding/decoding of the transmitted/received frames, and provide the electrical interface to the Ethernet transceiver cable (AUI). Diagnostic loopback control enables the 82C501AD to route the signal to be transmitted from the Intel LAN Controller through its Manchester encoding and decoding circuitry and back to the Intel LAN Controller. The combined loopback capabilities of the Intel LAN Controller and 82C501AD result in highly effective fault detection and isolation through sequential testing of the communications interface. A (defeatable) on-chip watchdog timer circuit prevents the station from locking up in a continuous transmit mode. The 82C501AD is pin compatible with the 82C501 and functionally compatible with the 82501 and SEEQ 8023A.

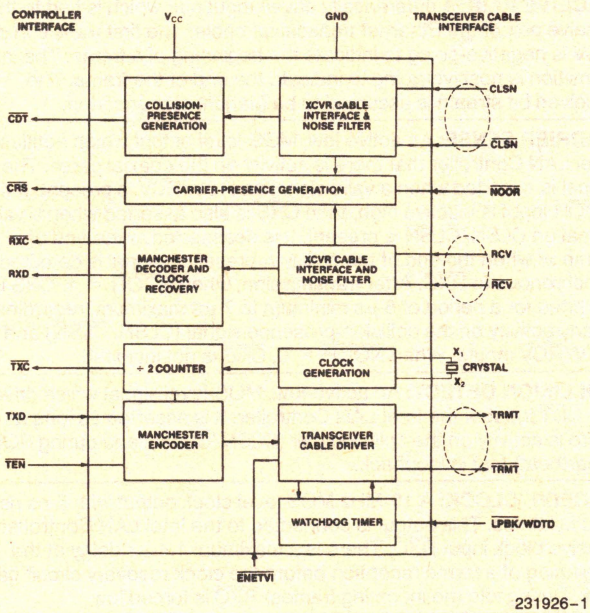
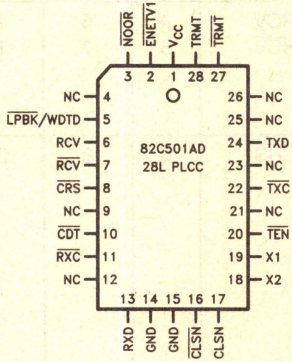


Figure 1. 82C501AD Functional Block Diagram

PLCC



DIP

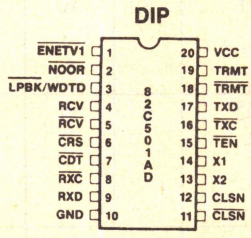


Figure 2. Pin Configurations (PLCC and DIP)

Table 1. Pin Description

Symbol	DIP Pin No.	PLCC Pin No.	Type	Name and Function
$\overline{\text{ENETV1}}$	1	2	I	**ETHERNET VERSION 1.0:** An active low, MOS-level input intended for use as a strapping option. When $\overline{\text{ENETV1}}$ is asserted, the TRMT/$\overline{\text{TRMT}}$ pair remains at high differential voltage at the end of transmission. This operation is compatible with the Ethernet Version 1.0 specification. If the $\overline{\text{ENETV1}}$ pin is left floating, an internal pull-up resistor biases the input inactive high. When $\overline{\text{ENETV1}}$ is high, the TRMT/$\overline{\text{TRMT}}$ differential voltage gradually approaches 0V at the end of transmission.
$\overline{\text{NOOR}}$	2	3	I	**CRS 'OR':** An active low, MOS-level input intended for use as a strapping option. When $\overline{\text{NOOR}}$ is low, only the presence of a valid signal on the RCV/$\overline{\text{RCV}}$ pair will force $\overline{\text{CRS}}$ active. If the $\overline{\text{NOOR}}$ pin is floating, an internal pull-up resistor biases the input inactive high. When $\overline{\text{NOOR}}$ is inactive high, either the presence of a valid signal on CLSN/$\overline{\text{CLSN}}$ or on RCV/$\overline{\text{RCV}}$ will force $\overline{\text{CRS}}$ active.
$\overline{\text{LPBK}}$/ WDTD	3	5	I	**LOOPBACK/WATCHDOG TIMER DISABLE:** An active low, TTL-level control signal that enables the loopback mode. In loopback mode serial data on the TXD input is routed through the 82C501AD internal circuits and back to the RXD output without driving the TRMT/$\overline{\text{TRMT}}$ output pair to the transceiver cable. During loopback $\overline{\text{CDT}}$ is asserted at the end of each transmission to simulate the SQE test. The $\overline{\text{LPBK}}$ signal should be driven high once V_{CC} is stabilized. **WATCHDOG TIMER DISABLE:** An input voltage of 10 to 16 V through a 1 kΩ resistor will disable the on-chip watchdog timer.
RCV $\overline{\text{RCV}}$	4 5	6 7	I I	**RECEIVE PAIR:** A differentially driven input pair which is tied to the receive pair of the Ethernet transceiver cable. The first transition on RCV is negative-going to indicate the beginning of a frame. The last transition is positive-going to indicate the end of the frame. The received bit stream is assumed to be Manchester encoded.
$\overline{\text{CRS}}$	6	8	O	**CARRIER SENSE:** An active low, MOS-level output which notifies the Intel LAN Controller that there is activity on the coaxial cable. The signal is asserted when a valid signal on RCV/$\overline{\text{RCV}}$ is present. If the $\overline{\text{NOOR}}$ input is inactive high, then $\overline{\text{CRS}}$ is also asserted when a valid signal on CLSN/$\overline{\text{CLSN}}$ is present. It is deasserted at the end of a frame or when the end of the collision-presence signal is detected, synchronous to $\overline{\text{RXC}}$. After transmission, when $\overline{\text{NOOR}}$ = 1, $\overline{\text{CRS}}$ is inhibited for a period of 5 μs minimum to 7 μs maximum, regardless of any activity on the collision-presence signal (CLSN/$\overline{\text{CLSN}}$) and RCV/$\overline{\text{RCV}}$ inputs. When $\overline{\text{NOOR}}$ = 0, $\overline{\text{CRS}}$ is not inhibited.
$\overline{\text{CDT}}$	7	10	O	**COLLISION DETECT:** An active-low, MOS-level signal which drives the $\overline{\text{CDT}}$ input of the Intel LAN Controller. It is asserted as long as there is activity on the collision pair (CLSN/$\overline{\text{CLSN}}$), and during SQE (heartbeat) test in loopback.
$\overline{\text{RXC}}$	8	11	O	**RECEIVE CLOCK:** A 10-MHz MOS level clock output with 5-ns rise and fall times. This output is connected to the Intel LAN Controller receive clock input $\overline{\text{RXC}}$. There is a maximum 1.4-μs delay at the beginning of a frame reception before the clock recovery circuit gains lock. During idle (no incoming frames) $\overline{\text{RXC}}$ is forced low.
RXD	9	13	O	**RECEIVE DATA:** A MOS-level output tied directly to the RXD input of the Intel LAN Controller and sampled by the Intel LAN Controller at the negative edge of $\overline{\text{RXC}}$. The bit stream received from the transceiver cable is Manchester decoded prior to being transferred to the controller. This output remains high during idle.

Table 1. Pin Description (Continued)

Symbol	DIP Pin No.	PLCC Pin No.	Type	Name and Function
GND	10	14 15		**GROUND**
CLSN $\overline{CLSN}$	12 11	17 16	I I	**COLLISION PAIR:** A differentially driven input pair tied to the collision-presence pair of the Ethernet transceiver cable. The collision-presence signal is a 10-MHz square wave. The first transition at CLSN is negative-going to indicate the beginning of the signal; the last transition is positive-going.
X_1 X_2	14 13	19 18	I I	**CLOCK CRYSTAL:** 20-MHz crystal inputs. When X_2 is floated, X_1 can be driven by an external MOS level input clock.
$\overline{TEN}$	15	20	I	**TRANSMIT ENABLE:** An active low, TTL level signal synchronous to $\overline{TXC}$ that enables data transmission to the transceiver cable and starts the watchdog timer. $\overline{TEN}$ can be driven by the $\overline{RTS}$ signal from the Intel LAN Controller.
$\overline{TXC}$	16	22	O	**TRANSMIT CLOCK:** A 10-MHz MOS level clock output with 5-ns rise and fall times. This clock is connected directly to the $\overline{TXC}$ input of the Intel LAN Controller.
TXD	17	24	I	**TRANSMIT DATA:** A TTL-level input signal that is directly connected to the serial data output, TXD, of the Intel LAN Controller.
TRMT $\overline{TRMT}$	19 18	28 27	O O	**TRANSMIT PAIR:** A differential output driver pair that drives the transmit pair of the transceiver cable. The output bit stream is Manchester encoded. Following the last transmission, which is always positive at TRMT, the differential voltage is slowly reduced to zero volts in a series of steps. If $\overline{ENETV1}$ is asserted this voltage stepping is disabled.
V_{CC}	20	1		**POWER:** 5V ±10%.

FUNCTIONAL DESCRIPTION

Clock Generation

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ± 0.01% clock required by the IEEE 802.3 specification.

It is recommended that a crystal meeting the following specifications be used:

- Quartz Crystal
- 20.00 MHz ± 0.002% at 25°C
- Accuracy ±0.005% Over Full Operating Temperature, 0 to 70°C
- Parallel Resonant with 20-pF Load Fundamental Mode

Several vendors have these crystals available; either off the shelf or custom made. Two possible vendors are:

1. M-Tron Industries, Inc
   Yankton, SD 57078
2. Crystek Corporation
   100 Crystal Drive
   Ft Myers, FL 33907

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics, therefore it is advised to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 and 35 pF.

An external, 20 MHz, MOS-level clock may be applied to pin X_1 while pin X_2 is left floating.

TRANSMIT SECTION

Manchester Encoder and Transceiver Cable Driver

The 20-MHz clock is used to Manchester encode data on the TXD input line. The clock is also divided by two to produce the 10-MHz clock required by the

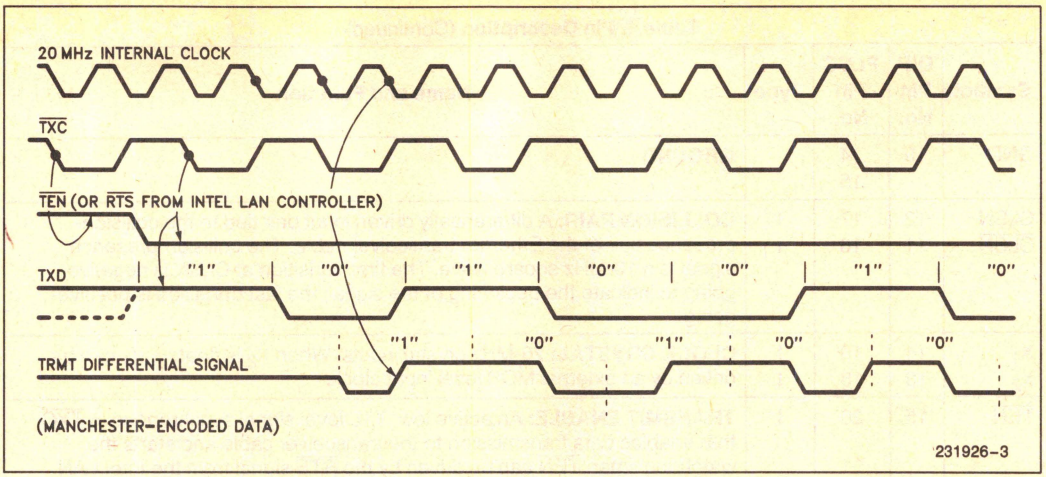


Figure 3. Start of Transmission and Manchester Encoding

Intel LAN Controller for synchronizing its $\overline{RTS}$ and TXD signals. See Figure 3. (Note that the Intel LAN Controller $\overline{RTS}$ is tied to the 82C501AD $\overline{TEN}$ input as shown in Figure 4.)

Data encoding and transmission begins with $\overline{TEN}$ going low. Since the first bit is a '1', the first transition on the transmit output TRMT is always negative. Transmission ends with the $\overline{TEN}$ going high. The last transition is always positive at TRMT and can occur at the center of the bit cell (last bit = 1) or at the boundary of the bit cell (last bit = 0). A 1.5-bit delay is introduced by the 82C501AD between its TXD input and TRMT/$\overline{TRMT}$ output as shown in Figure 3. If the signal applied to the $\overline{ENETV1}$ input is inactive high, the TRMT differential output is kept at high differential for 200 ns, after the last transmit data transition, then it is gradually reduced. The TRMT/$\overline{TRMT}$ differential voltage will become less than 40 mV within t_{18} after the last positive transition. The undershoot for return to idle is less than 100 mV differentially. This mode of operation is compatible with the IEEE 802.3 transceiver specifications.

If an active signal is present at the $\overline{ENETV1}$ input at the end of transmission, the TRMT/$\overline{TRMT}$ pair output will remain at a high differential voltage. As a result there is a positive differential voltage during the entire transmit idle time. This mode of operation is compatible with the Ethernet Version 1.0 specification.

Immediately after the end of a transmission all signals on the receive pair are inhibited for 5 μs minimum to 7 μs maximum (when $\overline{NOOR}$ = 1). This dead time is required for proper operation of the SQE (heartbeat) test.

An internal watchdog timer is started when $\overline{TEN}$ is asserted low at the beginning of the frame. The duration of the watchdog timer is 25 ms ± 15%. If the transmission terminates (by deasserting the $\overline{TEN}$) before the timer expires, the timer is reset (and ready for the next transmission). If the timer expires before the transmission ends, the frame is aborted. The frame is aborted by disabling the output driver for the TRMT/$\overline{TRMT}$ pair. RXD and $\overline{RXC}$ are not affected. The watchdog timer is reset only when the $\overline{TEN}$ is deasserted.

The cable driver is a differential circuit requiring external pulldown resistors of 240Ω ±5%. In addition, high-voltage protection to +10V maximum, and short circuit protection to ground is provided.

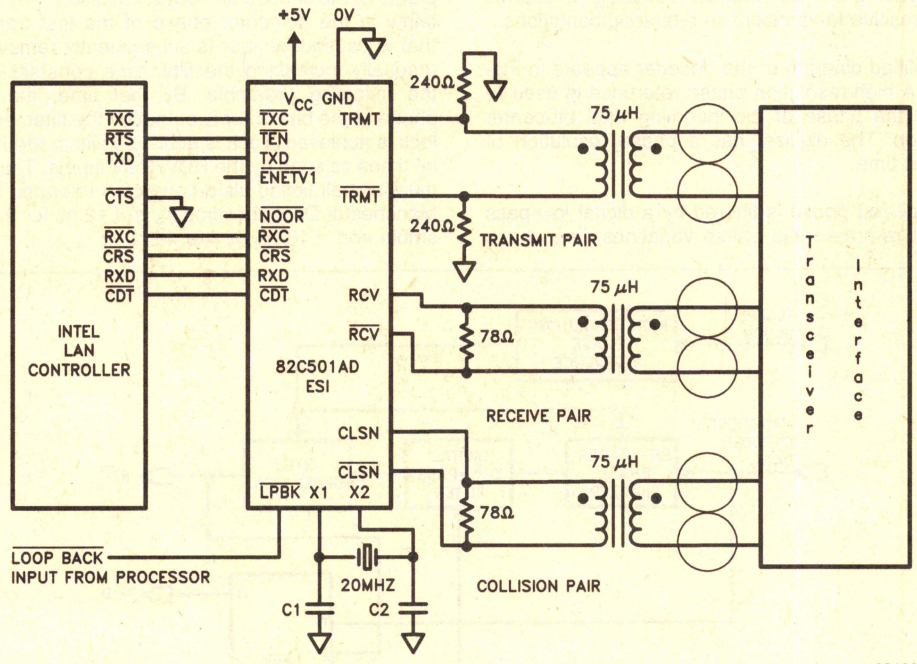
To provide additional high voltage protection if the cable is shorted, an isolation transformer can be used to isolate the TRMT and $\overline{\text{TRMT}}$ outputs from the transceiver cable. Transmit circuit inductance (including the IEEE 802.3 transceiver transformers) should be a minimum of 27 μH. We recommend that the transformer at the 82C501AD end have a minimum inductance of 75 μH.

RECEIVE SECTION

Cable Interface

The 82C501AD input circuits can be driven directly from the Ethernet transceiver cable receive pair. In this case the cable is terminated with a resistor of 78Ω ±6% for proper impedance matching. See Figure 4.

The signal received on the RCV/$\overline{\text{RCV}}$ pair from the transceiver defines both the $\overline{\text{RXC}}$ and RXD outputs to the Intel LAN Controller. The $\overline{\text{RXC}}$ and RXD signals are recovered from the encoded RCV/$\overline{\text{RCV}}$ pair signal by the Manchester decode circuitry.



NOTE:
$C_1 = C_2 = 22$ pF to 35 pF.
For best operation, a decoupling capacitor should be used between V_{CC} and GND.

Figure 4. LAN Controller/82C501AD/Transceiver Interface

The input circuits can also be driven with ECL voltage levels. In either case, the input common mode voltage must be in the range of 0-V_{CC} volts to allow for wide driver supply variation at the transceiver. To provide additional high voltage protection, if the cable is shorted, an isolation transformer can be used to isolate the RCV and $\overline{RCV}$ inputs from the cable.

Manchester Decoder and Clock Recovery

The Manchester-encoded data stream is decoded to separate the Receive Clock ($\overline{RXC}$) and the Receive Data ($\overline{RXD}$) from the stream. The 82C501AD uses an advanced digital technique to perform the decoding function. The use of digital circuitry instead of analog circuitry (e.g., a phase-lock loop) to perform the decoding ensures that the decoding function is less sensitive to variations in operating conditions.

A simplified diagram of the decoder appears in Figure 5. A high-resolution phase reference is used to digitize the phase of the incoming data bit-center transition. The digitizer has a phase resolution of 1/32 bit time.

The digitized phase is filtered by a digital low-pass filter to remove rapid phase variations; i.e., phase jitter. Slow phase variations, such as those caused by small differences between the data frequency and the clock frequency, are passed unfiltered by the low-pass filter.

The $\overline{RXC}$ generator digitally sets the phases of the two $\overline{RXC}$ transitions to respectively lead and lag the bit-center transition by 1/4 bit time. $\overline{RXC}$ is used to recover RXD by sampling the incoming data with an edge-triggered flip-flop.

The Frame_Detect signal informs the decoder that the first valid negative transition of a new frame has been detected. This signal is used to initiate the lock-on sequence of the decoder. Lock is achieved by reducing the time constant of the digital filter to zero at the start of a new frame. With a time constant of zero, the filter immediately outputs the phase of the second bit-center transition. Any uncertainty in the bit-center phase of the first transition that is caused by jitter is subsequently removed by gradually increasing the filter time constant during the following preamble. By that time, the exact phase of the bit center is output by the filter, and the lock is achieved. Lock is achieved within the first 14 bit times as seen by the RCV/$\overline{RCV}$ inputs. The maximum bit-cell timing distortion (jitter) tolerated by the Manchester Decoder Circuitry is ±12 ns for the preamble and ±18 ns for the data.

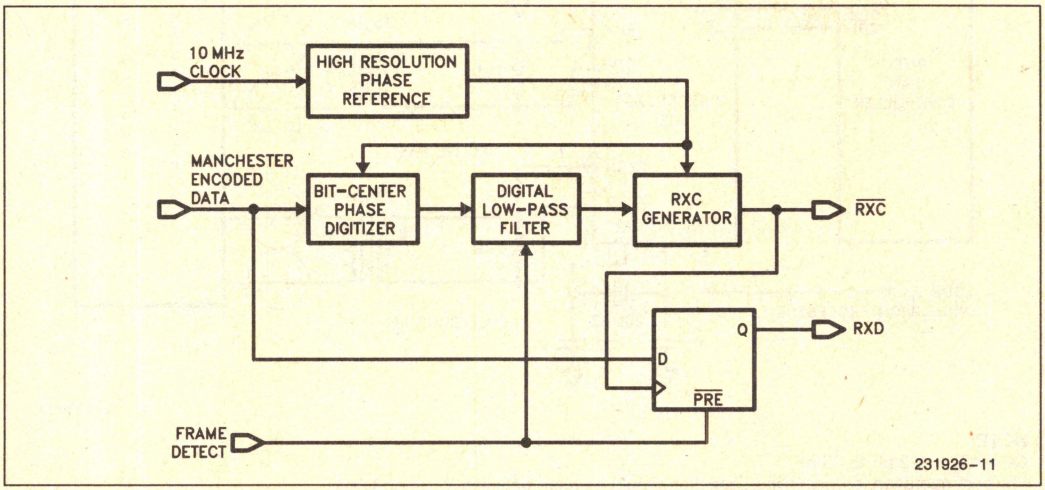


Figure 5. Manchester Decoder

COLLISION-PRESENCE SECTION

The CLSN/$\overline{\text{CLSN}}$ input signal is a 10 MHz +25%/−15% square-wave generated by the transceiver whenever two or more data frames are superimposed on the coaxial cable. The pulse width of the CLSN/$\overline{\text{CLSN}}$ signal can be no less than 35 ns and no greater than 70 ns measured at the 0-V crossing.

The common-mode voltage and external termination are identical to the RCV/$\overline{\text{RCV}}$ input. (See Figure 4.)

A valid collision presence signal will assert the 82C501AD $\overline{\text{CDT}}$ output, which can be directly tied to the $\overline{\text{CDT}}$ input of the Intel LAN Controller. During normal operation the 82C501AD logically "ORs" the collision presence signal with an internal signal, indicating valid data reception on the RCV/$\overline{\text{RCV}}$ pair, to generate $\overline{\text{CRS}}$ output. If, however, the $\overline{\text{NOOR}}$ input is asserted low, this "OR" function is removed and $\overline{\text{CRS}}$ is only asserted by the presence of valid data on the RCV/$\overline{\text{RCV}}$ pair. This mode of operation is required for repeater design.

During the time that valid collision-presence transitions are present on the CLSN/$\overline{\text{CLSN}}$ input, invalid data transitions may be present on the receive data pair due to the superposition of signals from two or more stations transmitting simultaneously. It is possible for RCV/$\overline{\text{RCV}}$ to lose transitions for a few bit times due to perfect cancellation of the signals; this may cause the 82C501AD to abort the reception.

The $\overline{\text{CRS}}$ signal is asserted low (along with $\overline{\text{CDT}}$) whenever a valid collision-presence signal is present and $\overline{\text{NOOR}}$ = 1. If this collision-presence signal arrives within 5 μs to 7 μs after the last transmission, only $\overline{\text{CDT}}$ is generated. This ensures that the LAN Controller recognizes the active $\overline{\text{CDT}}$ as a valid SQE (heartbeat) test signal.

NOISE FILTERING ON RCV AND CLSN PAIRS

Both the receive and collision pairs have the following characteristics.

- At idle, the noise filter is turned on.
- A pulse is rejected if:

a. Its peak voltage is more positive than −150 mV, with no restriction on width, or:

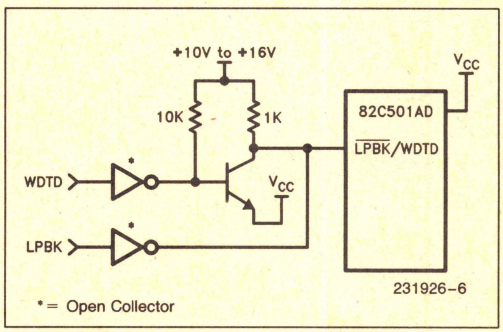
b. Its peak voltage is more positive than −600 mV and its width is less than 5 ns (measured at a reference level of −285 mV).

- The filter is turned off by the first valid negative pulse on the RCV or CLSN pair. A pulse whose peak voltage is more negative than −300 mV and whose width is greater than 30 ns (measured at −285 mV) is considered valid.
- The filter is turned on again when no positive transition is observed on the RCV or CLSN pair for 160 ns.

Internal Loopback

When asserted, $\overline{\text{LPBK}}$ causes the 82C501AD to route serial data from its TXD input through its transmit logic (retiming and Manchester encoding); returning it through the receive logic (Manchester decoding and receive clock generation) to RXD output. The internal routing prevents the data from passing through the output drivers and onto the transmit output pair TRMT/$\overline{\text{TRMT}}$. When in loopback mode all of the transmit and receive circuits, are tested except for the transceiver cable output driver and input receivers. Also, at the end of each frame transmitted in loopback mode the 82C501AD generates the SQE test (heartbeat) signal within 1 μs after the end of the frame. Thus, the collision circuits are also tested in loopback mode. During loopback, as in any normal reception, the 82C501AD receive circuitry uses 14 bit times while the Manchester Decoder locks on the data. As a result, the first 14 bits are lost and $\overline{\text{RXC}}$ is held low during that time.

The watchdog timer remains enabled in loopback mode, terminating test frames that exceed its timeout period. The watchdog timer can be inhibited by connecting $\overline{\text{LPBK}}$ to a 1 kΩ resistor connected to 10 to 16V. The loopback feature can still be used to test the integrity of the 82C501AD by using the circuit shown in Figure 6.



LPBK	WDTD	Function
1	X	LPBK mode
0	0	Normal mode
0	1	Normal mode with watchdog timer disabled

Figure 6. Watchdog Timer Disable

The 82C501AD operates as a full-duplex device, being able to transmit and receive simultaneously. By

combining the internal and external loopback modes of the Intel LAN Controller, and the internal loopback and normal modes of the 82C501AD, incremental testing of an Intel LAN Controller/82C501AD-based interface can be performed under program control for systematic fault detection and fault isolation.

Interface Example

The 82C501AD is designed to work directly with the Intel LAN Controller in IEEE 802.3 10 Mb/s, as well as other 10 Mb/s LAN applications. The control and data signals connect directly between the two devices without the need for additional external logic. The complete Intel LAN Controller/82C501AD Ethernet Transceiver interface is shown in Figure 4. The 82C501AD provides the driver and receivers needed to directly connect to the transceiver cable or requiring only terminating resistors on each input signal pair and 240Ω pull-down resistors.

It is recommended that a decoupling capacitor be used between V_{CC} and GND.

The Transmit, Receive, and Collision pairs have a maximum 10V overvoltage protection.

If additional high voltage protection is desired, a pulse transformer should be included for Ethernet applications. IEEE 802.3 10BASE5 (Ethernet) specifications require at least 16V protection for the Transmit, Receive, and Collision pairs. In 10BASE2 (Cheapernet) a pulse transformer is required to be inserted between the DTE (Intel LAN Controller/82C501AD) and the transceiver. In an Ethernet/Cheapernet design, a single transformer can be used for both connections at minimal additional cost.

The pulse transformer should have the following characteristics:

1. A minimum inductance of 75 μH.
2. 2000V isolation between primary and secondary windings.
3. 2000V isolation between primaries of separate transformers.

Since Ethernet Version 1.0 transceivers can require a positive differential on the TRMT pair during idle, check with the transceiver vendor before including the pulse transformer.

ABSOLUTE MAXIMUM RATING*

Case Temperature Under Bias . . . . . 0°C to +85°C
Storage Temperature . . . . . −65°C to +140°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +6.0V(1)
Operating Power Dissipation 0.75W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS T_C = 0°C to +85°C, V_{CC} = 5V ±10%

Symbol	Parameter		Min	Max
V_{IL}	Input Low Voltage	TTL MOS	−0.5V −0.5V	0.8V 0.6V
V_{IH}	Input High Voltage	TTL MOS	2.0V 3.9V	V_{CC} + 0.5V V_{CC} + 0.5V
V_{ACCEPT}	Differential Input Accept Voltage		±285 mV	
V_{REJECT}	Differential Input Reject Voltage			±150 mV
V_{CM}	Input Common Mode Voltage		0V	V_{CC}
V_{OCM}	Common Mode Output Voltage(2)		0.5V	5.0V
V_{OL}	Output Low Voltage @ I_{OL} = 4 mA			0.45V
V_{OH}	Output High Voltage (MOS) @ I_{OH} = −500 µA		3.9V	
V_{ODF}	Differential Output Voltage(2)		±0.45V	±1.2V
V_U	TRMT Pair Differential Return to Zero Undershoot(2)			−100 mV
V_{DI}	TRMT Pair Differential Idle Voltage(2)			±40 mV(5)
I_{LI}	Input Leakage Current @ V_{IN} = 0V to V_{CC}(3)			±10 µA
I_{CC}	Power Supply Current @ T_C = 85°C(4)			135 mA
I_{SP}	Short Protection Activation Current		60 mA	150 mA
I_L	Input Load Current(6)			±1 mA
C_{IN}	Input Capacitance @ fc = 1 MHz(7)			10 pF

NOTES:
1. The voltage levels for CLSN/$\overline{\text{CLSN}}$, RCV/$\overline{\text{RCV}}$ inputs are −0.75V to +10V.
2. The testing load is a 78Ω ±1% resistor in parallel with a 27 µH ±1% inductor and two 240Ω ±5% pulldown resistors.
3. Applies to TXD and $\overline{\text{TEN}}$ pins.
4. Part of the power is dissipated through the pulldown resistors connected to the TRMT/$\overline{\text{TRMT}}$ outputs.
5. Measured after t_{18} has expired.
6. Applies to RCV/$\overline{\text{RCV}}$, X_1, CLSN/$\overline{\text{CLSN}}$, $\overline{\text{LPBK}}$/WDTD, $\overline{\text{NOOR}}$, and $\overline{\text{ENETV1}}$ inputs for input voltages from 0V to V_{CC}.
7. Characterized, not tested.

A.C. MEASUREMENT CONDITIONS

1. T_C = 0°C to +85°C, V_{CC} = 5V ±10%.
2. The AC MOS, TTL and differential signals are referred to in Figures 7, 8, 9, 10 and 10A.
3. AC Loads:
   a) MOS: a 20 pF total capacitance to ground.
   b) Differential: a 10 pF total capacitance from each terminal to ground, two 240Ω ±5% pull down resistors, and a load resistor of 78Ω ±1% in parallel with a 27 μH ±1% inductor between terminals.
4. All AC Parameters become valid 100 μs after the supply voltage has stabilized.

Clock Timing(1)

Symbol	Parameter	Min	Max	Unit
t_1	X_1 Cycle Time	49.995	50.005	ns
t_2	X_1 Fall Time(2)		5	ns
t_3	X_1 Rise Time(2)		5	ns
t_4	X_1 Low Time(2)	15		ns
t_5	X_1 High Time(2)	15		ns

NOTES:
1. Refer to Figure 9.
2. Applies to external clock inputs.

TRANSMIT TIMING(1)

Symbol	Parameter	Min	Max	Unit
t_6	$\overline{TXC}$ Cycle Time(2)	99.99	100.01	ns
t_7	$\overline{TXC}$ Rise/Fall Time		5	ns
t_8	TXD Rise/Fall Time		10	ns
t_9	$\overline{TXC}$ Low Time	40		ns
t_{10}	$\overline{TXC}$ High Time	40		ns
t_{11}	Transmit Enable/Disable to $\overline{TXC}$ Low	45		ns
t_{12}	TXD Stable to $\overline{TXC}$ Low	45		ns
t_{13}	Bit Cell Center to Bit Cell Center of Transmit Pair Data(3)	99.5	100.5	ns
t_{14}	$\overline{TEN}$ Rise/Fall Time		10	ns
t_{15}	Transmit Differential Signal Rise/Fall Time		5.0	ns
t_{16}	Bit Cell Center to Bit Cell Boundary of Transmit Pair Data(3)	49.5	50.5	ns
t_{17}	$\overline{TRMT}$ held low from Last Positive Transition of the Transmit Pair at the End of Frame	200		ns
t_{18}	From Last Positive Transition of Transmit Pair Differential Output Approaches Within 40 mV of zero volts.		8000	ns

NOTES:
1. Refer to Figure 11.
2. This parameter is exactly twice t_1.
3. Characterized, not tested.

RECEIVE TIMING(1)

Symbol	Parameter	Min	Max	Unit
t_{19}	Duration which the $\overline{RXC}$ is held at Low State at the Start of a Packet		1400	ns
t_{20}	Receive Pair Signal Rise/Fall Time(5)		10	ns
t_{21}	Receive Pair Bit Cell Center Jitter in Preamble(2)		±12	ns
t_{22}	Receive Pair Bit Cell Center Jitter in Data(2)		±18	ns
t_{23}	Receive Idle Time after Transmission in a Transmitting Station	8		µs
t_{24}	Receive Pair Signal Return to Zero Level from Last Valid Positive Transition	160		ns
t_{25}	$\overline{CRS}$ Assertion Delay from the First Received Valid Negative Transition of Receive Pair Signal		100	ns
t_{26}	$\overline{CRS}$ Deassertion Delay from the Last Valid Positive Transition Received (when no Collision-Presence Signal Exists on the Transceiver Cable)(3)		300	ns
t_{27}	$\overline{RXC}$ Cycle Time	96	104	ns
t_{28}	$\overline{RXC}$ Rise/Fall Time		5.0	ns
t_{29}	$\overline{RXC}$ Low Time	40		ns
t_{30}	$\overline{RXC}$ High Time	36		ns
t_{31}	Receive Data Stable Before the Negative Edge of $\overline{RXC}$	30		ns
t_{32}	Receive Data Held Valid Past the Negative Edge of $\overline{RXC}$	30		ns
t_{33}	Carrier Sense Active → Inactive Hold Time from $\overline{RXC}$ High	10	40	ns
t_{34}	Receive Data Rise/Fall Time(5)		10	ns
t_{35}	$\overline{CRS}$ Inhibit Time After Frame Transmission(4)	5	7	µs

NOTES:
1. Refer to Figures 12 and 13.
2. Measured per 802.3 Para B1.1.4.2 recommendations.
3. $\overline{CRS}$ is deasserted synchronously with the $\overline{RXC}$. This condition is not specified in the IEEE 802.3 specification.
4. Required for SQE test. Applies when $\overline{NOOR}$ = 1. For $\overline{NOOR}$ = 0 there is no inhibit of $\overline{CRS}$.
5. Characterized, not tested.

COLLISION TIMING(1)

Symbol	Parameter	Min	Max	Unit
t_{36}	CLSN/$\overline{\text{CLSN}}$ Cycle Time	80	118	ns
t_{37}	CLSN/$\overline{\text{CLSN}}$ Rise/Fall Time(2)		10	ns
t_{38}	CLSN/$\overline{\text{CLSN}}$ High/Low Time	35	70	ns
t_{39}	CLSN Pair Return to Zero from Last Positive Transition	160		ns
t_{40}	$\overline{\text{CDT}}$ Assertion from the First Valid Negative Edge of Collision Pair Signal		75	ns
t_{41}	$\overline{\text{CDT}}$ Deassertion from the Last Positive Edge of CLSN/$\overline{\text{CLSN}}$ Signal		300	ns
t_{42}	$\overline{\text{CRS}}$ Deassertion from the Last Positive Edge of CLSN/$\overline{\text{CLSN}}$ Signal (if no Post-Collision Signal Remains on the Receive Pair)		450	ns

NOTE:
1. Refer to Figure 14.
2. Characterized, not tested.

LOOPBACK TIMING(1)

Symbol	Parameter	Min	Max	Unit
t_{43}	$\overline{\text{LPBK}}$ asserted before the first attempted transmission (2)	500		ns
t_{44}	Simulated collision test delay from the end of each attempted transmission	0.5	1.5	µs
t_{45}	Simulated collision test duration(3)	0.6	1.6	µs
t_{46}	$\overline{\text{LPBK}}$ deasserted after the last attempted transmission	5		µs

NOTES:
1. Refer to Figure 15.
2. In Loopback mode, $\overline{\text{RXC}}$ and $\overline{\text{CRS}}$ function in the same manner as a normal Receive.
3. SQE test (heartbeat) signal

NOISE FILTER(1)

Symbol	Parameter	Min	Max	Unit
t_{47}	RCV/$\overline{\text{RCV}}$ Noise Filter Pulse Width Rejected		5	ns
t_{48}	RCV/$\overline{\text{RCV}}$ Noise Filter Pulse Width Accepted	30		ns
t_{49}	CLSN/$\overline{\text{CLSN}}$ Noise Filter Pulse Width Rejected		5	ns
t_{50}	CLSN/$\overline{\text{CLSN}}$ Noise Filter Pulse Width Accepted	25		ns

NOTE:
1. Refer to Figure 16.

A.C. TIMING CHARACTERISTICS

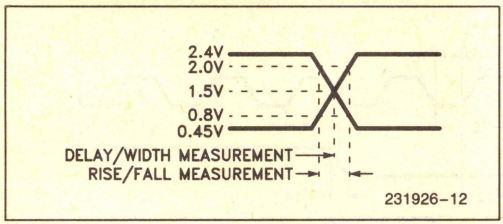


Figure 7. TTL Input Voltage Levels for Timing Measurements ($\overline{TEN}$, TXD, $\overline{LPBK}$/WDTD).

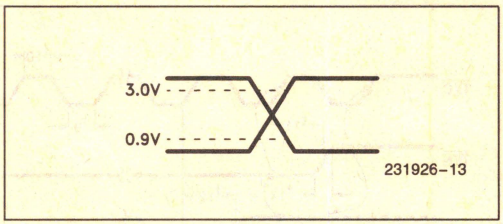


Figure 8. Voltage Levels for MOS Level Output-Timing Measurements ($\overline{TXC}$, $\overline{RXC}$, $\overline{CRS}$, $\overline{CDT}$, and RXD).

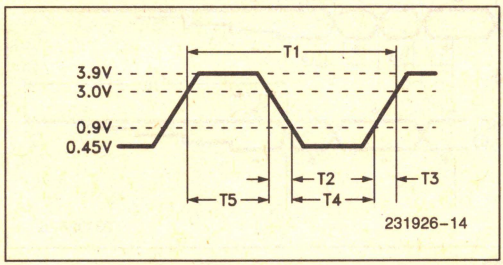


Figure 9. X1 Input Voltage Levels for Timing Measurements

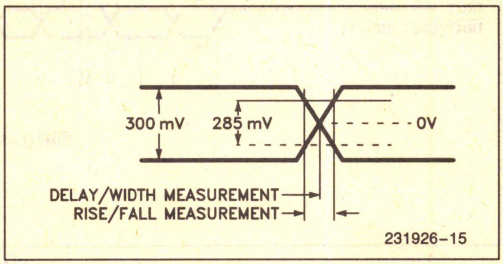


Figure 10. Voltage Levels for Differential-Input Timing Measurements (RCV/$\overline{RCV}$ and CLSN/$\overline{CLSN}$).

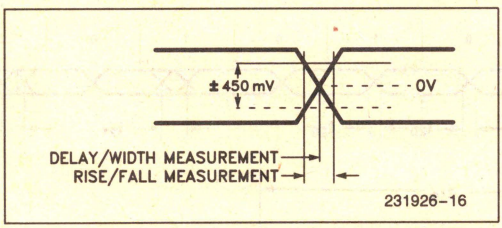


Figure 10A. Voltage Levels for TRMT/$\overline{TRMT}$ Output-Timing Measurements

TRANSMIT TIMING

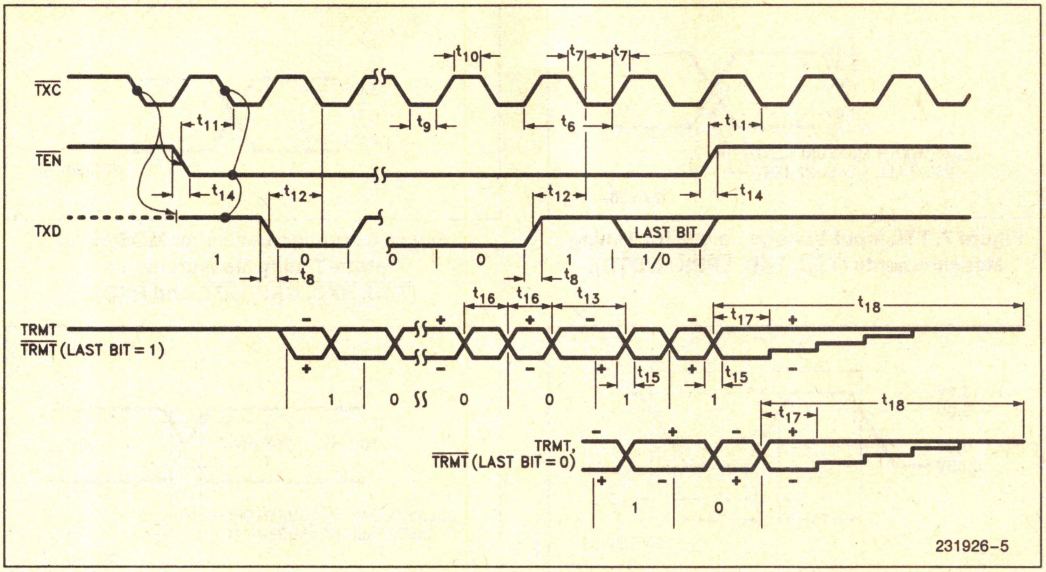


Figure 11

RECEIVE TIMING: START OF FRAME

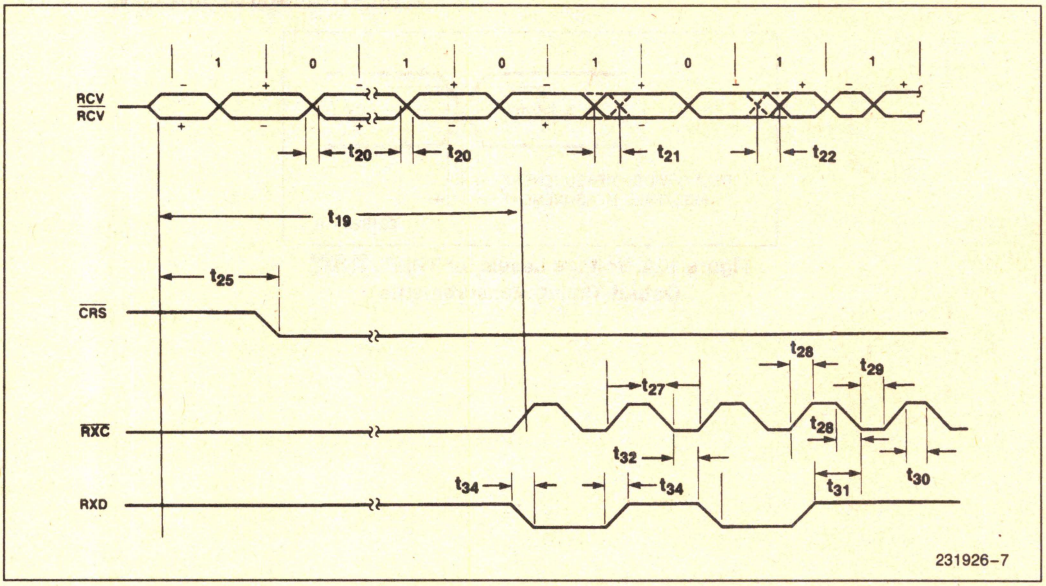


Figure 12

RECEIVE TIMING: END OF FRAME

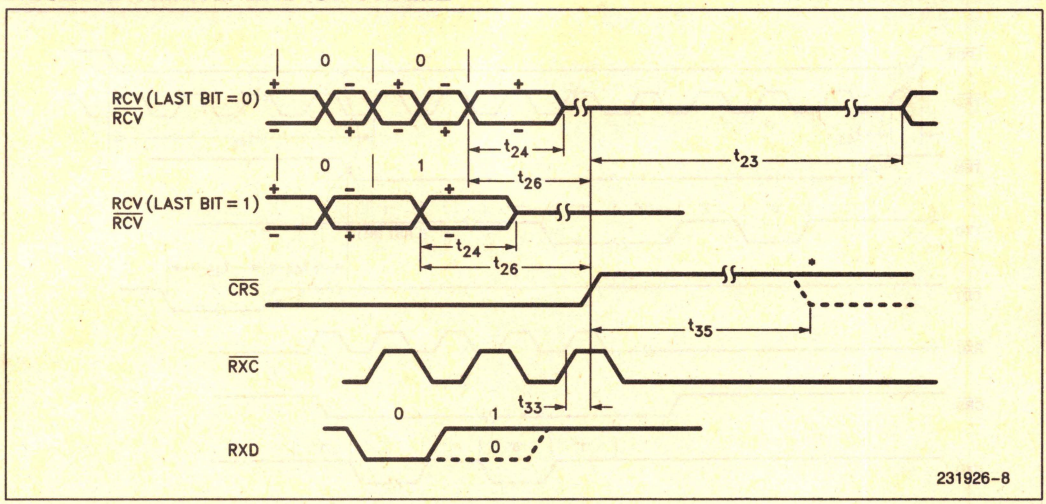


Figure 13

COLLISION TIMING

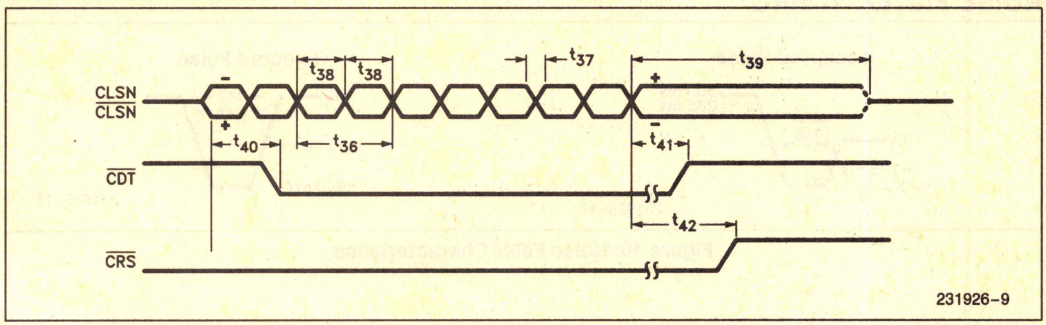


Figure 14

LOOPBACK TIMING

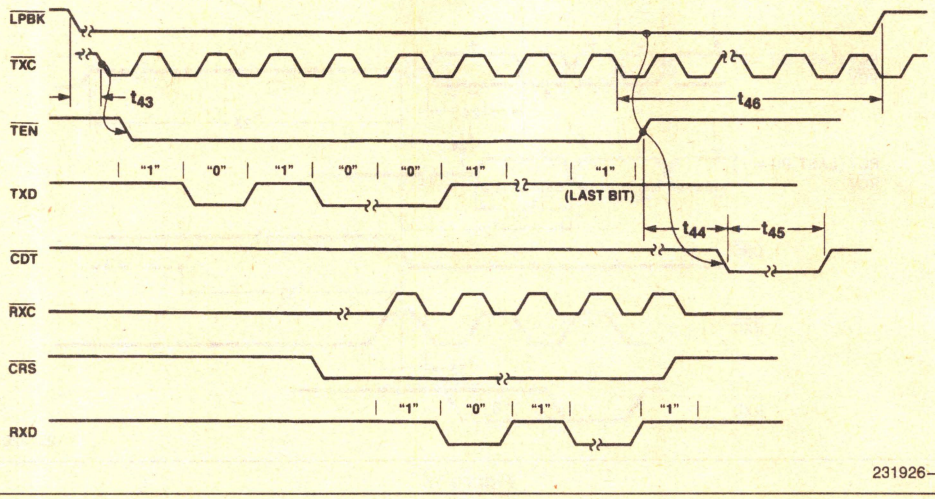
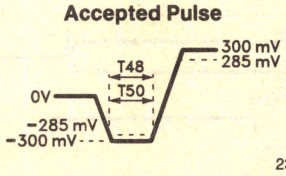


Figure 15

NOISE FILTER TIMING



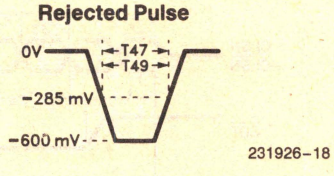
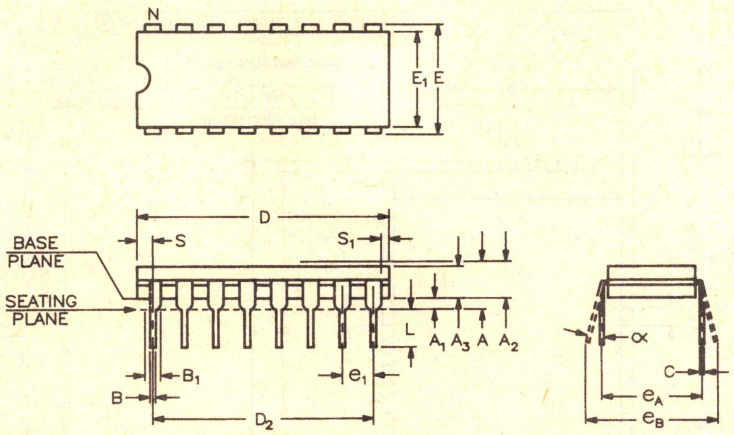


Figure 16. Noise Filter Characteristics

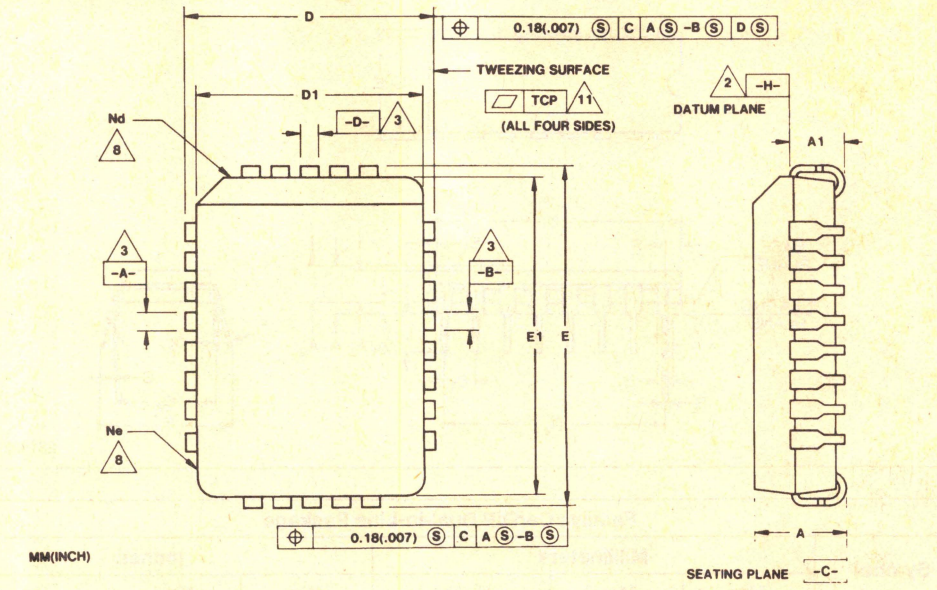
20 LEAD CERDIP DUAL IN-LINE PACKAGE INTEL TYPE D



231926-20

Family : CerDIP Dual-In-Line Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A		5.08			0.200	
A_1	0.38			0.015		
A_2	3.56	4.24		0.140	0.167	
A_3	3.56	4.24		0.140	0.167	
B	0.41	0.51		0.016	0.020	
B_1	1.52		Typical	0.060		Typical
C	0.23	0.30	Typical	0.009	0.012	Typical
D	24.38	25.27	Reference	0.960	0.995	
D_2	22.86		Reference	0.900		Reference
E	7.62	8.13		0.300	0.320	
E_1	7.11	7.90		0.280	0.31	
e_1	2.29	2.79		0.090	0.110	
e_A	7.87		Reference	0.310		Reference
e_B	8.13	10.16		0.320	0.400	
L	3.18	3.81		0.125	0.150	
N	20		½ Leads	20		½ Leads
S	0.38	1.78		0.015	0.070	
S_1	0.13			0.005		
ISSUE	IWS 1/15/87					

PLASTIC LEADED CHIP CARRIER RECTANGULAR



Dimension	28 Lead (Inch)		28 Lead (mm)	
	Min	Max	Min	Max
Overall Height (A)	0.126	0.140	3.20	3.56
Shoulder to Board Height (A_1)	0.076	0.090	1.93	2.29
Outside Dimension (D)	0.385	0.396	9.78	10.0
Plastic Body Dimension (D_1)	0.347	0.353	8.81	8.97
Foot Print (D_2)	0.290	0.330	7.37	8.38
Foot Print (D_3)	0.200 Ref.		5.08 Ref.	
Outside Dimension (E)	0.585	0.595	14.9	15.1
Platic Body Dimension (E_1)	0.547	0.553	13.9	14.0
Foot Print (E_2)	0.490	0.530	12.4	13.5
Foot Print (E_3)	0.400 Ref.		10.2 Ref.	
# of Leads (N)	28		28	
# of Leads on Short Side (N_d)	5		5	
# of Leads on Long Side (N_e)	9		9	
Seating Plane Coplanarity (CP)	0.000	0.004	0.00	0.10
Tweezing Coplanarity (TCP)	0.000	0.004	0.000	0.10
Lead Thickness (LT)	0.009	0.015	0.23	0.38
Issue	IWS 1/15/87			

82503
DUAL SERIAL TRANSCEIVER (DST)

82503 PRODUCT FEATURE SET OVERVIEW

- Single Component Ethernet* Interface to Both 802.3 10BASE-T and AUI
- Automatic or Manual Port Selection
- Manchester Encoder/Decoder and Clock Recovery
- No Glue Interface to Industry-Standard LAN Controllers
  - — Intel 82586, 82590, 82593 and 82596
  - — AMD 7990 (LANCE*)
  - — National Semiconductor 8390 and 83932 (SONIC*)
  - — Western Digital 83C690
  - — Fujitsu 86950 (Etherstar*)
- Diagnostic Loopback
- Reset, Low Power Modes
- Network Status Indicators
- Defeatable Jabber Timer
- User Test Modes
- 10 MHz Transmit Clock Generator
- One Micron CHMOS** IV (Px48) Technology
- Single 5-V Supply

1

INTERFACE FEATURES

TPE

- Complies with 10BASE-T, IEEE Std. 802.3i-1990 for Twisted Pair Ethernet
- Selectable Polarity Switching
- Direct Interface to TPE Analog Filters
- On-Chip TPE Squelch
- Defeatable Link Integrity (LI)
- Support of Cable Lengths $>$ 100m

AUI

- Complies with IEEE 802.3 AUI Standard
- Direct Interface to AUI Transformers
- On-Chip AUI Squelch

A block diagram of a typical application is shown in Figure 1. The 82503 Dual Serial Transceiver is a high-integration CMOS device designed to simplify interfacing industry standard Ethernet LAN Controllers to IEEE 802.3 local area network applications (10BASE5, 10BASE2, and 10BASE-T). The component supports both an attachment unit interface (AUI) and a Twisted Pair Ethernet interface (TPE). It allows OEMs to design a state-of-the-art media interface that is jumperless and fully automatic. The 82503 includes on-chip AUI and TPE drivers and receivers; it offers designers a cost-effective, integrated solution for interfacing LAN controllers to the wire medium.

**CHMOS is a patented process of Intel Corporation.
*Ethernet is a registered trademark of Xerox Corporation.
LANCE is a registered trademark of Advanced Micro Devices.
Etherstar is a registered trademark of Fujitsu Electronics.
Sonic is a registered trademark of National Semiconductor Corporation.

November 1992
Order Number: 290421-003

82503 Dual Serial Transceiver (DST)

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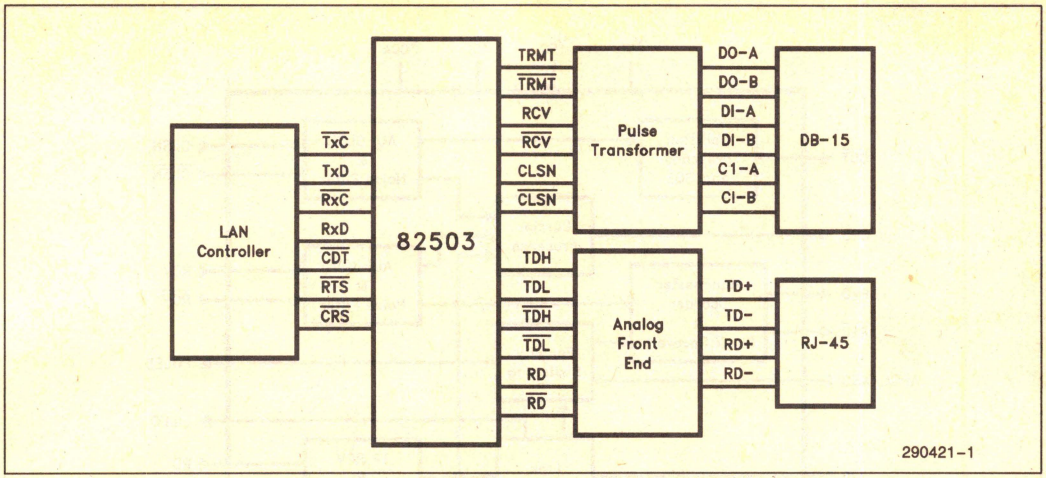


Figure 1. Application Block Diagram

1.0 82503 PRODUCT FEATURES

The 82503 incorporates all the active circuitry required to interface Ethernet controllers to 10BASE-T networks or the attachment unit interface (AUI). It supports a direct no-glue interface to Intel's family of high-performance LAN controllers (82586, 82590, 82593, and 82596). The 82503 also provides a direct no-glue interface to the National Semiconductor 8390 and 83932 (SONIC), the Western Digital 83C690, the Advanced Micro Devices 7990 (LANCE) and 79C900 (ILACC), and the Fujitsu 86950 (Etherstar) controllers.

This component includes three advanced features: jumperless two-port design capability, automatic port selection, and polarity switching. The jumperless TPE or AUI port selection capability allows designers maximum ease-of-use and network flexibility. Automatic port selection ensures complete software compatibility with existing 10BASE2 and 10BASE5 software drivers. The 82503's polarity switching feature will detect and correct polarity errors on the twisted pair—the most common wiring fault in twisted pair networks.

The 82503 contains all the circuitry needed to meet the 10BASE-T specification, including link integrity, a jabber timer and internal predistortion. Deselecting link integrity allows the component to be used in some prestandard networks. The 82503's jabber timer prevents the station from continuously transmitting and is defeatable for simple design characterization. The predistortion circuitry eliminates line overcharge and reduces jitter on 10BASE-T links.

The 82503 can also support twisted pair cable lengths of up to 200m when placed in TPE Extended Squelch Mode (XSQ).

This component incorporates six LED drivers to display transmit data, receive data, collision, link integrity, polarity faults and port selections, allowing for complete network monitoring by the user. The transmit, receive and collision LEDs indicate the rate of activity by the frequency of flashing. The 82503 also has a low power mode. During low power, many of the 82503's pins are in a high-impedance state to facilitate board-level testing.

The 82503's diagnostic loopback control enables it to route a transmission signal from the LAN controller through its Manchester encoder-decoder circuitry and back to the LAN controller. This provides effective network node fault detection and isolation capabilities. In addition, the 82503 supports diagnostic test modes that generate continuous tranmission of data through the twisted pair port, allowing designers to measure the analog performance of their design.

The 82503 is available in 44-lead PLCC and 44-lead QFP packages and is fabricated with Intel's low-power, high-speed, CHMOS IV technology using a single 5-V supply.

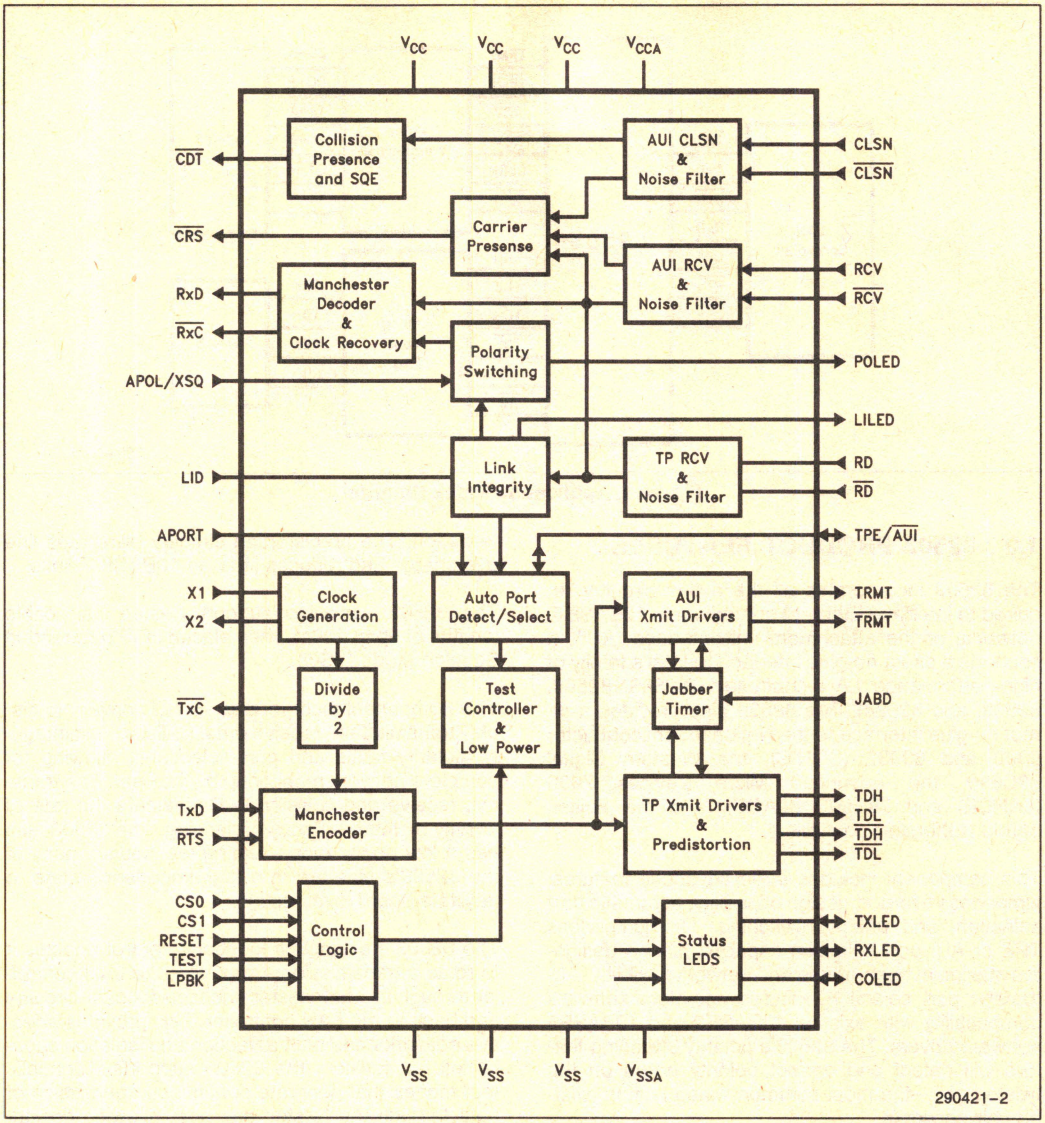


Figure 2. 82503 Functional Block Diagram

2.0 PIN DEFINITION

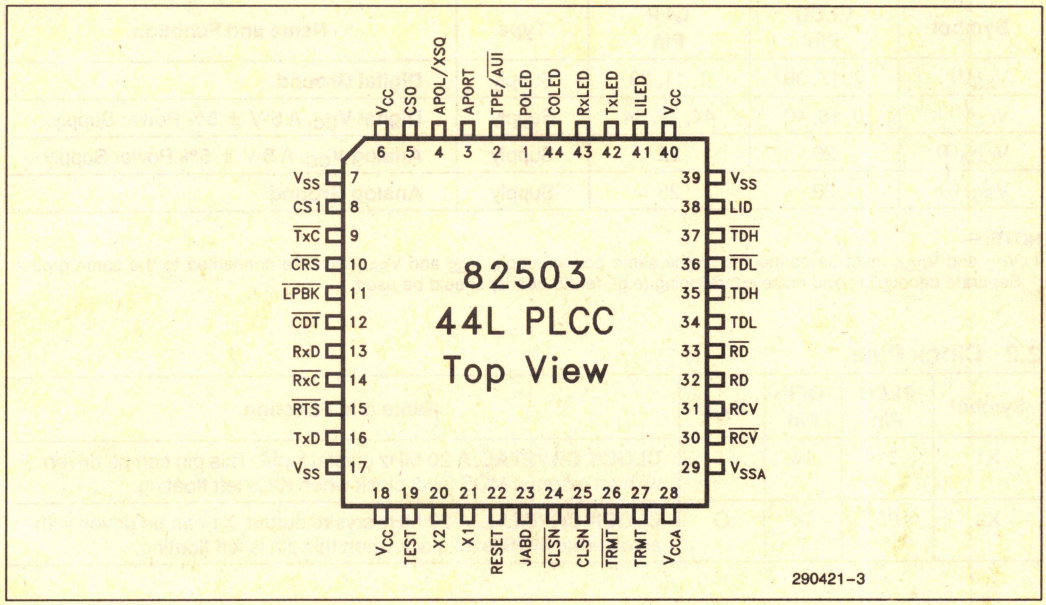


Figure 3. 44-Lead PLCC Pin Configuration

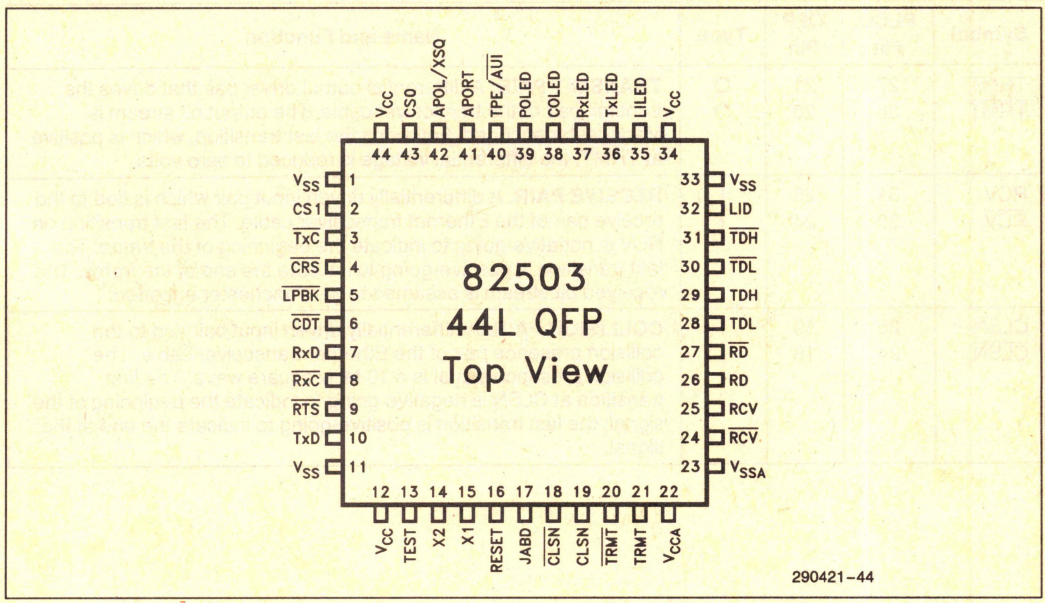


Figure 4. 44-Lead QFP Pin Configuration

2.1 Power Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
V_{SS}(1)	7, 17, 39	1, 11, 33	Supply	**Digital Ground.**
V_{CC}(1)	6, 18, 40	44, 12, 34	Supply	**Digital V_{CC}.** A 5-V ± 5% Power Supply.
V_{CCA}(1)	28	22	Supply	**Analog V_{CC}.** A 5-V ± 5% Power Supply.
V_{SSA}(1)	29	23	Supply	**Analog Ground.**

NOTE:
1. V_{CC} and V_{CCA} must be connected to the same power supply. V_{SS} and V_{SSA} must be connected to the same ground. Separate decoupling and noise conditioning (e.g., ferrite beads) should be used.

2.2 Clock Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
X1	21	15	I	**CLOCK CRYSTAL.** A 20 MHz crystal input. This pin can be driven with an external MOS level clock when X2 is left floating.
X2	20	14	O	**CLOCK CRYSTAL.** A 20 MHz crystal output. X1 can be driven with an external MOS level clock when this pin is left floating.

2.3 AUI Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TRMT $\overline{\text{TRMT}}$	27 26	21 20	O O	**TRANSMIT PAIR.** A differential output driver pair that drives the transmit pair of the transceiver cable. The output bit stream is Manchester encoded. Following the last transition, which is positive at TRMT, the differential voltage is reduced to zero volts.
RCV $\overline{\text{RCV}}$	31 30	25 24	I I	**RECEIVE PAIR.** A differentially driven input pair which is tied to the receive pair of the Ethernet transceiver cable. The first transition on RCV is negative-going to indicate the beginning of the frame. The last transition is positive-going to indicate the end of the frame. The received bit stream is assumed to be Manchester encoded.
CLSN $\overline{\text{CLSN}}$	25 24	19 18	I I	**COLLISION PAIR.** A differentially driven input pair tied to the collision presence pair of the Ethernet transceiver cable. The collision presence signal is a 10 MHz square wave. The first transition at CLSN is negative-going to indicate the beginning of the signal; the last transition is positive-going to indicate the end of the signal.

2.4 TPE Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TDH $\overline{\text{TDH}}$ TDL $\overline{\text{TDL}}$	35 37 34 36	29 31 28 30	O O O O	**TP TRANSMIT PAIR DRIVERS.** These four outputs constitute the twisted-pair drivers, which have predistortion capabilities. The TDH/$\overline{\text{TDH}}$ outputs generate the 10 Mb/s Manchester Encoded data. The TDL/$\overline{\text{TDL}}$ outputs mirror the TDH/$\overline{\text{TDH}}$ outputs except for fat bit occurrences (100 ns pulses). During the second half of a fat bit (either high or low), the TDL/$\overline{\text{TDL}}$ outputs are inverted with respect to TDH/$\overline{\text{TDH}}$ outputs. This signal behavior reduces the amount of jitter by preventing overcharge on the twisted pair medium.
RD $\overline{\text{RD}}$	32 33	26 27	I I	**TP RECEIVE PAIR.** The differential twisted pair receiver. The receiver pair is connected to the twisted pair medium and is driven with 10 Mb/s Manchester encoded data.

1

2.5 Controller Interface Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
$\overline{\text{TxC}}$	9	3	O	**TRANSMIT CLOCK.** A 10 MHz clock output tied directly to the transmit clock pin of the Ethernet controller. Changes sense depending on controller selected. Active low for Intel and Fujitsu controller interfaces, active high for National and AMD interfaces. Can drive one TTL load.
TxD	16	10	I	**TRANSMIT DATA.** TTL input. NRZ serial data is clocked in on TxD from the Ethernet controller. Connects directly to the transmit data pin of the Ethernet controller.
$\overline{\text{RTS}}$	15	9	I	**REQUEST TO SEND.** TTL input. An active low input signal synchronous to $\overline{\text{TxC}}$ which enables data transmission on the active port. Changes sense depending on controller selected. Active low for the Intel controller interface, active high for National, AMD, and Fujitsu interfaces.
$\overline{\text{RxC}}$	14	8	O	**RECEIVE CLOCK.** A 10 MHz clock output tied directly to the receive clock pin of the Ethernet controller. This clock is the recovered clock from incoming data on the active port. Changes sense depending on controller selected. Active low for Intel and Fujitsu controller interfaces, active high for National and AMD interfaces. Can drive one TTL load.
RxD	13	7	O	**RECEIVE DATA.** Received NRZ data (synchronous to $\overline{\text{RxC}}$) passed to the Ethernet controller. Connect directly to the receive data pin of the controller. Can drive one TTL load.
$\overline{\text{CRS}}$	10	4	O	**CARRIER SENSE.** Output that alerts the Ethernet controller that data is present on the active port. Connects directly to the carrier sense pin of the Ethernet controller. Changes sense depending on controller mode selected. Active low for Intel controller interface, active high for National, AMD, and Fujitsu interfaces. Can drive one TTL load.
$\overline{\text{CDT}}$	12	6	O	**COLLISION DETECT.** Output that indicates presence of a collision. Connects directly to the collision detect pin of the Ethernet controller. Changes sense depending on controller selected. Active low for Intel and Fujitsu controller interfaces, active high for National and AMD interfaces. Can drive one TTL load.

2.6 Mode Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TPE/$\overline{\text{AUI}}$	2	40	I/O	**PORT SELECT.** TTL input/LED output. If APORT is low, TPE/$\overline{\text{AUI}}$ is an input and selects either the TPE port (TPE/$\overline{\text{AUI}}$ high) or AUI port (TPE/$\overline{\text{AUI}}$ low). If APORT is high, the 82503 will indicate the port selected by driving TPE/$\overline{\text{AUI}}$ high (TPE) or low (AUI). TPE/$\overline{\text{AUI}}$ can drive an LED pull-up.
APORT	3	41	I	**AUTOMATIC PORT SELECTION.** TTL input. When high, 82503 will automatically select TPE or AUI port based on presence of valid link beats or frames on the TPE receive input. Mode selected will be indicated on TPE/$\overline{\text{AUI}}$.
APOL/XSQ	4	42	I	**AUTOMATIC POLARITY CORRECTION/EXTENDED SQUELCH ENABLE.** TTL input. When high, the extended squelch mode is disabled and automatic polarity correction is enabled. Both junctions (APOL and XSQ) are enabled when this pin is at a high impedance state. When low, both functions become disabled. The presence of a polarity fault on the TPE receive pair is indicated on POLED regardless of the state of APOL.
LID	38	32	I	**LINK INTEGRITY DISABLE.** TTL input. If high, link integrity function is disabled. If low, link integrity function is enabled.
CS0 CS1	5 8	43 2	I I	**CONTROLLER SELECT.** Selects the appropriate interface for the desired Ethernet controller. When CS0/1 = 0/0, supports Intel controllers. When CS0/1 = 0/1, supports Fujitsu controllers. When CS0/1 = 1/0, supports Western Digital and National controllers. When CS0/1 = 1/1, supports AMD controllers. (See Table 2.)
$\overline{\text{LPBK}}$	11	5	I	**LOOPBACK.** TTL input. An active low input signal that causes the 82503 to enter diagnostic loopback mode. The twisted pair or AUI medium will be removed from the circuit, thus isolating the node from the network. When not connected, this pin assumes the inactive (high) state. Diagnostic loopback does not disable the operation of the link integrity processor, link beat generator, or automatic port selection.
JABD	23	17	I	**JABBER DISABLE.** TTL input. When high, this pin disables the jabber function. When low, the jabber function is enabled and the device performs AUI or TP jabber protection for the active port. If this pin and TEST are asserted during a falling edge of RESET, the 82503 enters its low power mode; when either this pin or TEST deasserts, then the 82503 transitions to its normal operating mode.
TEST	19	13	I	**TEST MODE ENABLE.** TTL input. When TEST is high and RESET is deasserted, a customer test mode is directly accessed. When driven low, test mode is disabled. If this pin and JABD are asserted during a falling edge of RESET, the 82503 enters its low power mode; when either this pin or JABD deasserts, then the 82503 transitions to its normal operating mode.
RESET	22	16	I	**RESET.** TTL input. When high, resets internal circuitry. On the falling edge of RESET, either test mode or low power mode can be entered depending on the state of JABD and TEST.

2.7 LED Pins

Symbol	PLCC Pin	QFP Pin	Type	Name and Function
TxLED	42	36	I/O	**TRANSMIT LED.** LED output. Indicates transmit status of the AUI or TPE port. Normally off (high) output. Turns on to indicate transmission. Flashes at a rate dependent on the level of transmit activity. Upon entering a customer test mode, this pin must be driven high either through an LED, or a resistor.
RxLED	43	37	I/O	**RECEIVE LED.** LED output. Indicates receive status of the AUI or TPE port. Normally off (high) output. Turns on to indicate reception. Flashes at a rate dependent on the level of receive activity. Upon entering a customer test mode, this pin must be driven high either through an LED, or a resistor.
COLED	44	38	I/O	**COLLISION LED.** LED output. Indicates collision status of the AUI or TPE port. Normally off (high) output. Turns on to indicate collision. Flashes at a rate dependent on the level of collision activity. This pin is also used to determine which customer test modes are entered.
LILED	41	35	O	**LINK INTEGRITY LED.** LED output. Normally on (low) output which indicates good link integrity on the TPE port during TPE mode. Remains on when link integrity function has been disabled. Turns off during AUI mode or when link integrity fails in TPE mode. Minimum off time is 100 ms, minimum on time is set by the link integrity function.
POLED	1	39	O	**POLARITY INDICATION.** LED output. If the 82503 detects that the receive TPE wires are reversed, POLED will turn on (low) to indicate the fault. POLED remains on even if APOL/XSQ is high and the 82503 has automatically corrected for the reversed wires.

NOTE:

1. The LED outputs have a weak pull-up capable of sourcing 500 μA. They can sink 10 mA while still meeting TTL levels. All LEDs can be used as indication pins if no LED is needed. Some of these outputs include pulse width conditioning, which should be accounted for in software.

3.0 82503 ARCHITECTURE

3.1 Clock Generation

A 20 MHz parallel resonant crystal is used to control the clock generation oscillator, which provides the basic 20 MHz clock source. An internal divide-by-two counter generates the 10 MHz ±0.01% clock required by the IEEE 802.3 specification.

We recommend a crystal that meets the following specifications be used.

- Quartz Crystal
- 20 MHz ± 0.002% at 25°C
- Accuracy ± 0.005% over full operating temperature, 0°C to +70°C
- Parallel resonant with 20 pF Load Fundamental Mode
- Maximum Series Resistance: $R_{SERIES} = 30\Omega$

Several vendors have such crystals; either-off-the shelf or custom made. Two possible vendors are:

1. M-Tron Industries, Inc.
   Yankton, SD 57078

   Specifications;
   Part No. HC49 with 20 MHz, 50 PPM over 0°C to +70°C, and 20 pF fundamental load.
2. Crystek Corporation
   100 Crystal Drive
   Ft. Myers, FL 33907

   Part No. 013212

The accuracy of the Crystal Oscillator frequency depends on the PC board characteristics, therefore it is advisable to keep the X1 and X2 traces as short as possible. The optimum value of C1 and C2 should be determined experimentally under nominal operating conditions. The typical value of C1 and C2 is between 22 pF and 35 pF.

An external 20 MHz MOS-level clock may be applied to pin X1, if pin X2 is left floating.

3.2 Transmit Blocks

3.2.1 MANCHESTER ENCODER

The 20 MHz clock is used to Manchester-encode data on the TxD input. This clock is also divided by two to produce the 10 MHz clock the LAN controller needs for synchronizing its $\overline{RTS}$ and TxD signals.

Data encoding and transmission begins with $\overline{RTS}$ asserting. Since the first bit of a transmission is a 1, the first transition is always negative on the transmit outputs (TRMT or TD pins). Transmission ends when $\overline{RTS}$ deasserts. The last transition is always positive at the transmit outputs (TRMT or TD pins) and may occur at the center of the bit cell if the last data bit to be transmitted is a 1, or at the boundary of the bit cell if the last data bit to be sent is a 0.

Immediately after the end of a transmission, all signals on the RCV pair (when AUI mode is selected) are inhibited for 4 to 5 μs. This dead time is necessary for proper operation of the SQE (heartbeat) test.

3.2.2 AUI CABLE DRIVER

The AUI cable driver (TRMT pair) is a differential circuit, which interfaces to the AUI cable through a pulse transformer.

High voltage protection is achieved by using a transformer to isolate the transmit pins (TRMT pair) from the transceiver cable. The total transmit circuit inductance, including the 802.3 transceiver transformers, should be a minimum of 27 μH for Ethernet applications.

3.2.3 TWISTED PAIR CABLE DRIVER

The twisted pair line drivers (TD pairs) begin transmitting the serial Manchester bit stream 3 bit times after $\overline{RTS}$ is asserted. The line drivers use a predistortion algorithm to improve jitter performance for up to 100 meters of twisted pair cable. The line drivers reduce their drive level during the second half of "fat" (100 ns) Manchester pulses and maintain a full drive level during all "thin" (50 ns) pulses and during the first half of the "fat" pulses. This reduces line overcharging during "fat" pulses, a major source of jitter.

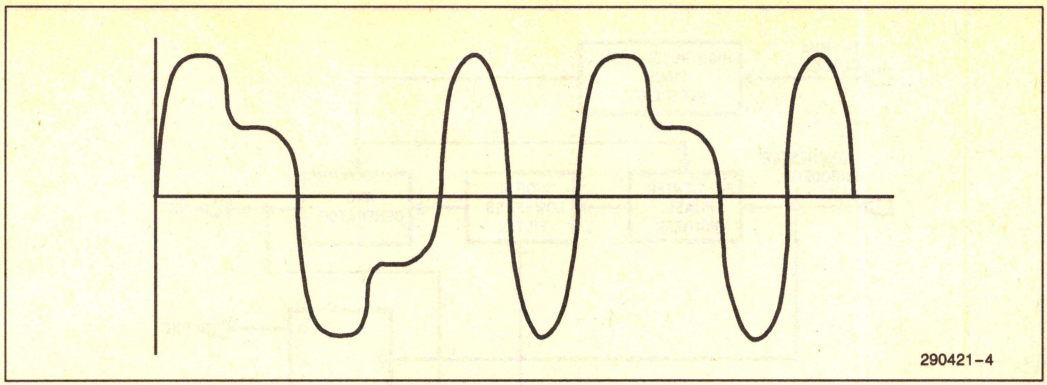


Figure 5. TPE Predistortion

3.3 Receive Blocks

3.3.1 MANCHESTER DECODER AND CLOCK RECOVERY

The 82503 performs Manchester decoding and timing recovery of the incoming data in AUI and TPE modes.

The Manchester-encoded data stream is decoded to separate the Receive Clock ($\overline{RxC}$) and the Receive Data (RxD) from the differential signal. The 82503 uses an advanced digital technique to perform the decoding function. The use of digital circuitry instead of analog circuitry (e.g., a phase-lock loop) to perform the decoding ensures that the decoding function is less sensitive to variations in operating conditions.

A high-resolution phase reference is used to digitize the phase of the incoming data bit-center transition. The digitizer has a phase resolution of 1/32 of a bit time.

The digitized phase is filtered by a digital low-pass filter to remove rapid phase variations, i.e., phase jitter. Slow phase variations, such as those caused by small differences between the data frequency and the clock frequency, are not filtered by the low-pass filter.

The $\overline{RxC}$ generator digitally sets the phases of the two $\overline{RxC}$ transitions to respectively lead and lag the bit-center transition by ¼ bit time. $\overline{RxC}$ is used to recover RxD by sampling the incoming data with an edge-triggered flip-flop.

Lock is achieved by reducing the time constant of the digital filter to zero at the start of a new frame. Any uncertainty in the bit-center phase of the first transition that is caused by jitter is subsequently removed by gradually increasing the filter time constant during the following preamble. By that time, the phase of the bit center is output by the filter, and lock is achieved. Lock is achieved within the first 14 bit times as seen by the AUI inputs. The maximum bit-cell timing distortion (jitter) tolerated by the Manchester decoder circuitry is ±12 ns (preamble), ±18 ns (data) for AUI, and ±13.5 ns for TPE (data and preamble).

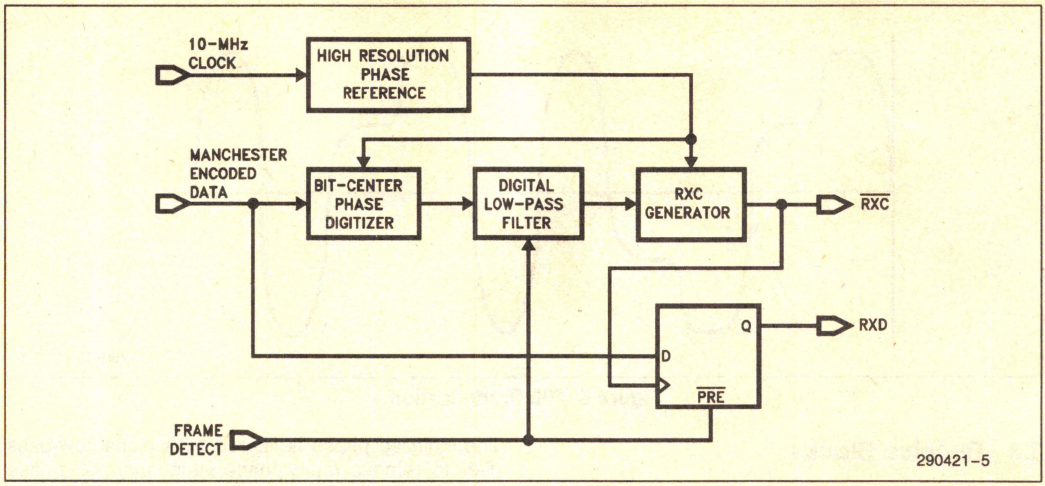


Figure 6. Manchester Decoder and Clock Recovery

3.3.2 AUI RECEIVE AND COLLISION BUFFERS

The AUI receive and collision inputs are driven through isolation transformers to provide high voltage protection and DC common mode voltage rejection. The incoming signals are converted to digital levels and passed to the Manchester decoder and collision detection circuitry.

3.3.3 AUI RECEIVE AND COLLISION SQUELCH CIRCUITS

Both the receive (RCV) and collision (CLSN) pairs have the following squelch characteristics.

- The squelch circuits are turned on at idle.
- A pulse is rejected if the peak differential voltage is more positive than −160 mV regardless of pulse width.
- A pulse is considered valid if its peak differential voltage is more negative than −300 mV and its width, measured at −285 mV, is greater than 25 ns.
- The squelch circuits are disabled by the first valid negative differential pulse on either the AUI receive (RCV) or the AUI collision (CLSN) pair.
- If a positive differential pulse occurs on either the AUI receive or collision pairs for greater than 160 ns, End of Frame (EOF) is assumed and the squelch circuitry is turned on.

3.3.4 TPE RECEIVE BUFFER

The TPE receive pins (RD and $\overline{RD}$) are connected to the twisted pair medium through an analog front end. The analog front end contains the line coupling devices and EMI filters necessary to conform to the 10BASE-T standards and local RF regulations. The input differential voltage range for the TPE receiver is greater than 500 mV and less than 3.1V differential.

3.3.5 TPE RECEIVE SQUELCH CIRCUITS

The TPE receive buffer distinguishes valid receive differential data, link test pulses, and the idle condition according to the requirements of the 10BASE-T standard. Signals at the output of the EMI filter (thus at the RD and $\overline{RD}$ pair) are rejected as follows:

- All differential pulses of peak magnitude less than 300 mV are rejected.
- All continuous sinusoids with a differential amplitude less than 6.2 V_{PP} and a frequency less than 2 MHz are rejected.
- All sine waves of single cycle duration starting with phase 0° or 180° that have an amplitude less than 6.2 V_{PP}, and a frequency of 2 MHz to 16 MHz are rejected, if the single cycle is preceeded and followed by 4 bit times of silence (i.e., a signal less than 300 mV).

3.3.6 TPE Extended Squelch Mode

By placing the 82503 into TPE extended squelch mode, the 82503 can support cable lengths greater than the 100m specified in the 10Base-T IEEE standard (802.3i-1990). The squelch thresholds for the signals at the RD/$\overline{RD}$ pair are typically reduced by 4.5 dB. This allows Grade 5 twisted-pair cable to be used to overcome attenuation and multipair crosstalk for cable lengths up to 200 meters.

TPE extended squelch mode is enabled by presenting a high-impedance (>100 KΩ) at the APOL/XSQ pin. This can be done by floating the APOL/XSQ pin, tying APOL/XSQ low through a 100 KΩ resistor, or driving APOL/XSQ with a three-state buffer. When driven high or low using a TTL driver or a low impedance pull-up or pull-down (<2 KΩ) extended squelch is disabled and the driven level at the APOL/XSQ pin determines the state of the polarity-correction function (APOL/XSQ = 1 enables polarity correction, APOL/XSQ = 0 disables polarity correction). The TPE extended squelch feature is transparent to previous steppings of the 82503. Polarity correction is always enabled when the TPE extended-squelch feature is enabled (APOL/XSQ = Z).

The APOL/XSQ pin senses a high-impedance state by an active-polling circuit implemented at the pin. Two small polling devices attempt to pull the APOL/XSQ pin up to V_{CC} and down to V_{SS}. If the pin is in a high-impedance state, the devices will be successful in pulling the APOL/XSQ pin high and low. If the pin is driven high or low, the polling devices will not be able to successfully pull the pin in the opposite direction. In this way, an internal state machine can correctly determine one of three states of the APOL/XSQ pin. The pin is polled every 25.6 μs.

3.4 Collision Detection

3.4.1 AUI COLLISION DETECTION

Collision detection in the AUI mode is performed by the attached transceiver, and signalled to the 82503 on the CLSN pair. A 10 MHz +25%, or −15%, square wave with transition times between 35 ns and 70 ns indicates the collision. The 82503 reports this to the LAN controller on the $\overline{CDT}$ pin.

3.4.2 TPE COLLISION DETECTION

Collision detection in the TPE mode is indicated by simultaneous transmission and reception on the twisted pair link segment. The $\overline{CDT}$ signal is asserted for the duration of both $\overline{RTS}$ and the presence of received data; $\overline{CRS}$ is asserted for the duration of either $\overline{RTS}$ or the presence of received data. During a collision, the source of RxD will be the received data. If the received data stream ends before the transmit data stream, the RxD source will be changed to transmit data stream until it ends.

3.5 Link Integrity

The 82503 supports the link integrity function as defined by 10BASE-T. During long periods of idle on the transmitter, link test pulses will be transmitted on to the twisted pair medium as an indication to the remote MAU that the link is good. These pulses will be transmitted 8 ms to 24 ms after the end of the last transmission or link test pulse.

The link integrity function continuously monitors activity on the receive circuit. If neither valid data nor link test pulses are received, the link integrity processor declares the link bad, and disables transmission and reception on the media, loopback, and the SQE test function. Transmission of link test pulses and monitoring receive activity are not affected. The idle time required for the link integrity processor to determine the link is bad is 50 ms to 150 ms.

Once a frame or a sequence of 2 to 10 valid consecutive link test pulses are detected, the Link Integrity Processor declares the link is good, and reconnects the transmitter and receiver.

The link integrity function can be disabled by driving the LID pin high or by disabling automatic port selection (APORT = 0) and selecting the AUI port. This option is intended primarily for use with pre-10BASE-T networks.

3.6 Jabber Function

The 82503 contains a jabber timer to implement the jabber function. If a transmission continues beyond the limits specified, the jabber function inhibits further transmission and asserts the collision indicator, $\overline{CDT}$. The limits for jabber transmission are 20 ms to 150 ms in TPE Mode, and 8 ms to 16 ms in AUI mode. For both AUI and TPE mode, the transmission inhibit period extends until the 82503 detects sufficient idle time (between 250 ms and 750 ns) on the $\overline{RTS}$ signal. The jabber function can be disabled by driving the JABD high.

In TPE mode the link integrity function continues to operate even if the jabber function is inhibiting transmission. Link test pulses continue to be sent and the receive circuit continues to be monitored. Additionally, the link integrity function reconnects to a restored link without waiting for the transmit input to go idle when the jabber function is inhibiting transmission.

3.7 TPE Loopback

In TPE mode the 82503 implements the transmit to receive loopback (DO to DI) mode specified in the 10BASE-T standard. This mode loops back transmitted data through the receive path.

This function is required to maintain full compatibility with coax MAUs where the data loopback is a natural result of the architecture.

The transmit to receive loopback function is disabled when the jabber function or link integrity function is inhibiting transmission.

3.8 SQE Test Function

The 82503 supports the SQE test function when in TPE mode or in Diagnostic Loopback mode. The 82503 will assert its $\overline{CDT}$ pin within 0.6 μs to 1.6 μs after the end of a transmission, and it will remain asserted for 5- to 15-bit times. If the 82503 is in the TPE mode and is not in diagnostic loopback mode, the link integrity function will disable the SQE test function when it detects a bad link.

3.9 Port Selection

The 82503 features both manual and automatic port selection. To enable automatic port selection, connect APORT to V_{CC}. The 82503 then starts in TPE mode and monitors link integrity. If the link is good, the 82503 stays in TPE mode and pulls TPE/$\overline{AUI}$ high to indicate that the TPE port was selected. If link integrity fails, the 82503 switches to AUI mode and pulls TPE/$\overline{AUI}$ low to indicate that the AUI port is now active. TPE/$\overline{AUI}$ can drive an LED to indicate port selection (on for AUI, off for TPE mode). Note that LILED will be on if TPE mode is selected and off if AUI mode is selected. If link integrity is disabled while automatic port selection is enabled, the 82503 defaults to TPE mode. If the 82503 changes ports while $\overline{RTS}$ is active, transmission is terminated with an End of Frame marker on the old port. Transmission of the remaining packet fragment is not allowed on the new port. Transmissions will begin with a complete data packet.

The port can be manually selected by driving APORT low. TPE/$\overline{AUI}$ = 0 selects AUI mode, and TPE/$\overline{AUI}$ = 1 TPE mode. When the port is manually selected, the circuitry for the unused port is powered down. Changing ports requires 100 μs to allow the circuitry for the new port to resume normal operation.

Table 1. Port Selection

Configuration			State
LID	APORT	TPE/$\overline{AUI}$	
X	0	0	AUI (TPE Port Powered Down)
X	0	1	TPE (AUI Port Powered Down)
0	1	X*	Automatic Port Selection
1	1	X*	TPE

NOTE:
*TPE/$\overline{AUI}$ is an output pin when APORT = 1.

3.10 LED Description

The 82503 supports six LED pins to indicate the status of important states; TPE/$\overline{AUI}$, TxLED, POLED, LILED, RxLED, COLED. Each pin is capable of directly driving an LED.

3.10.1 TPE/$\overline{AUI}$

When automatic port selection is enabled (APORT is high), TPE/$\overline{AUI}$ becomes an LED output and turns off if TPE mode is selected and on if AUI mode is selected.

3.10.2 TxLED

Transmit status. This LED is normally off and flashes at 2.5 Hz, 5 Hz, and 10 Hz to indicate respectively a low, medium, and high rate of transmit activity.

3.10.3 RxLED

Receive LED. This LED is normally off and flashes at 2.5 Hz, 5 Hz, and 10 Hz to indicate respectively a low, medium, and high rate of receive activity.

3.10.4 COLED

Collision LED. This LED is normally off and flashes at 2.5 Hz, 5 Hz, and 10 Hz to indicate respectively a low, medium, and high rate of collision activity.

3.10.5 POLED

Polarity Fault. This LED is normally off and turns on to indicate a polarity fault in the receive pair of the 10BASE-T link. Operation of this pin is not affected by the state of the polarity correction function (APOL/XSQ = X).

3.10.6 LILED

Link Integrity status. When Aport is enabled (APORT = 1), this LED is normally on (driven low) to indicate the presence of a valid 10BASE-T link when the TPE port is active. The LED will turn off (driven high) when the link fails. When link integrity is disabled (LID = 1) while APORT is enabled (APORT = 1) this LED is turned on (driven low). If APORT is disabled (APORT = 0) and the AUI port is manually selected (TPE/$\overline{AUI}$ = 0) the LED output is tristated.

3.11 Polarity Switching

In TPE mode, the 82503 monitors receive link beats and end-of-frame delimiters for a possible receiver

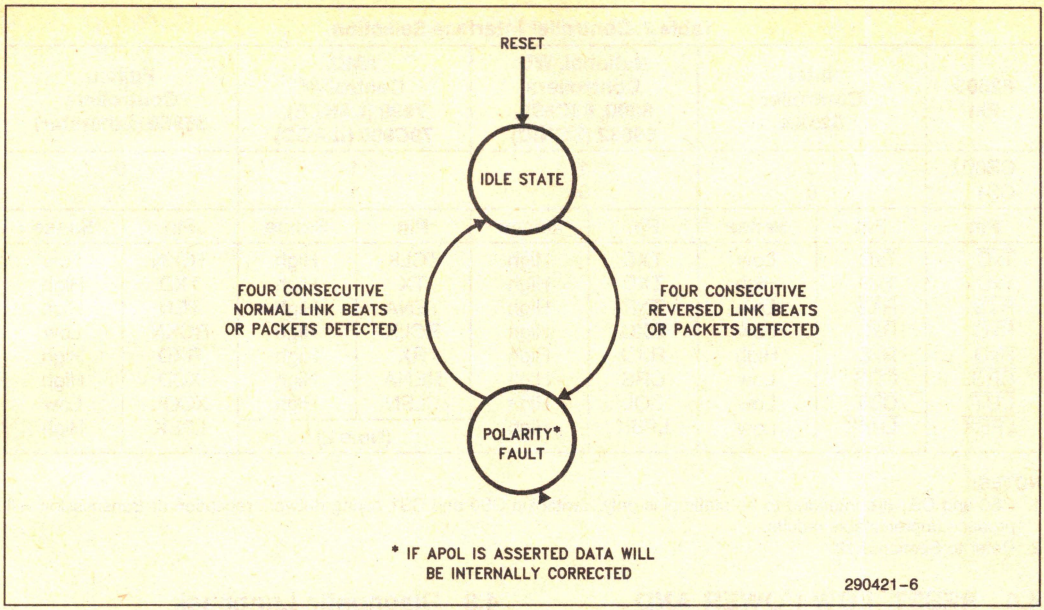


Figure 7. Polarity Fault State Diagram

polarity error due to crossed wires. If Pin 4 of the 82503 is high and the TPE receive pins are reversed, the 82503 will correct the error by reversing the signals internally, and turn POLED on (low) to indicate that the fault has been detected and corrected. The polarity correction function is defeatable by driving the APOL/XSQ input low. However, the polarity fault will continue to be indicated on the POLED.

3.12 Controller Interface

Connecting the 82503 to one of the Intel Ethernet controllers (82586, 82590, 82593, 82596) requires no additional components. Simply drive CS0 and CS1 both low, and connect $\overline{\text{TxC}}$, TxD, $\overline{\text{RTS}}$, $\overline{\text{RxC}}$, RxD, $\overline{\text{CRS}}$, $\overline{\text{CDT}}$, and $\overline{\text{LPBK}}$ to the corresponding controller pins.

The 82503 also works with other Ethernet controllers without additional components, including the National Semiconductor 8390 and 83932 (SONIC), Western Digital 83C690, Fujitsu 86950 (Etherstar), depending on the state of and CS0 and CS1 inputs.

The interface of the 82503 to the AMD 7990 (LANCE) requires external logic to control the $\overline{\text{LPBK}}$ pin of the 82503. Note that when an AMD LAN controller is used to interface to the 82503, the $\overline{\text{LPBK}}$ pin of the 82503 becomes active high. That is, the 82503 enters diagnostic loopback mode when $\overline{\text{LPBK}}$ pin is high and is in normal operation mode when $\overline{\text{LPBK}}$ pin is low.

The logic sense of the 82503 controller pins will change and should be connected to the controller pins according to the following table.

Table 2. Controller Interface Selection

82503 Pin	Intel Controller 825XX		National, WD Controllers 8390, 83C690, 83832 (SONIC)		AMD Controller 7990 (LANCE), 79C900 (ILACC)		Fujitsu Controllers 86950 (Etherstar)	
CS0(1)	0		1		1		0	
CS1	0		0		1		1	
Pin	**Pin**	**Sense**	**Pin**	**Sense**	**Pin**	**Sense**	**Pin**	**Sense**
$\overline{TxC}$	$\overline{TxC}$	Low	TXC	High	TCLK	High	TCKN	Low
TxD	TxD	High	TXD	High	TX	High	TXD	High
$\overline{RTS}$	$\overline{RTS}$	Low	TXE	High	TENA	High	TEN	High
$\overline{RxC}$	$\overline{RxC}$	Low	RXC	High	RCLK	High	RCKN	Low
RxD	RxD	High	RXD	High	RX	High	RXD	High
$\overline{CRS}$	$\overline{CRS}$	Low	CRS	High	RENA	High	XCD	High
$\overline{CDT}$	$\overline{CDT}$	Low	COL	High	CLSN	High	XCOL	Low
$\overline{LPBK}$	$\overline{LPBK}$	Low	LPBK	High	(Note 2)		LPBK	High

NOTES:
1. CS0 and CS1 are intended to be static pins only. Switching CS0 and CS1 during network reception or transmission will produce unpredictable results.
2. Refer to Section 3.12.

4.0 RESET, LOW-POWER AND TEST MODES

4.1 Reset

When RESET is asserted the device resets its internal circuits. RESET is required after power up, and before data can be transmitted or received. It is allowed any time thereafter, but any existing receive or transmit activity will be lost, and all state machines (Link integrity, Jabber, and Polarity Correction) return to their initial states. TEST must be held low for a device reset to prevent entering a test for low power mode. During RESET, $\overline{TxC}$ continues without interruption (in Fujitsu mode both $\overline{TxC}$ and $\overline{RxC}$ run continuously).

4.2 Low Power and High Impedance Modes

When RESET is deasserted while both TEST and JABD are held high, the 82503 enters its low power and high impedance modes. The majority of internal circuitry is powered down, and many inputs and outputs are three-stated. These pins are: APORT, APOL/XSQ, LID, TPE/$\overline{AUI}$, POLED, LILED, $\overline{RTS}$, $\overline{LPBK}$, RxD, TxD, $\overline{CRS}$ and $\overline{CDT}$. When either JABD or TEST is deasserted, the device begins a power on cycle which lasts less than 1 ms. During this cycle, all inputs are ignored and all transmissions are disabled. If $\overline{RTS}$ is active when the device returns to normal operation, the remainder of that packet fragment is not transmitted. Normal transmissions are resumed at the start of the first complete data packet.

4.3 Diagnostic Loopback

This is a diagnostic test mode to help in fault isolation and detection. Serial NRZ data input on TxD is Manchester encoded and then looped back through the Manchester decoder (TMD) appearing at the RxD output. Collision detect is asserted following each transmission to simulate the SQE test. Output cable drivers and input amplifiers are disconnected from the controller interface pins while in this mode. The link integrity and polarity fault detection functions are not inhibited by diagnostic loopback mode. If otherwise enabled, they continue to function.

4.4 Customer Test Mode (Continuous AUI/TPE Transmit)

In this mode, the 82503 continuously transmits data without the intervention of a LAN controller. Transmission is at 10 MHz (11-bit pattern), and can occur on either the TPE or AUI port. The jabber timer is disabled in this mode, allowing users to easily test the 10BASE-T harmonic content specification and the quality of their analog front end design without complex software exercisers.

Customer Test Mode—and Low Power Mode are selected at the deassertion of RESET as shown in the following table. (Note that the 82503 must be in non-loopback mode before it can enter the customer test mode.)

Table 3. Test and Low Power Mode Selection

RESET	TEST	JABD	TxLED(1)	RxLED(1)	COLED(1)	Mode Selected
↓	0	X	X	X	X	Normal Mode
↓	1	0	1	1	1	Cont Tx 10 MHz
↓	1	1	X	X	X	Low Power

NOTE:
1. A standard LED connection to these pins is sufficient to pull them to a logic 1.

The port on which the continuous transmit appears is determined by the APORT and TPE/$\overline{AUI}$ pins. If automatic port selection is enabled (APORT = 1) then the TPE port broadcasts the continuous transmit. If manual port selection is enabled (APORT = 0), then TPE/$\overline{AUI}$ selects the port (1 for TPE, 0 for AUI). Test mode is disabled when TEST is deasserted and the device is reset.

5.0 APPLICATION EXAMPLE

5.1 Introduction

The 82503 is designed to work directly with the Intel LAN controllers (82586, 82590, 82593, and 82596), as well as AMD's Am7990, National Semiconductor's 8390, Western Digital's 82C690, and Fujitsu's 86950. The serial interface signals connect directly between one of the aforementioned LAN controllers and the 82503 without the need for external logic.

This example is targeted toward interfacing the 82503 to the Intel 82596 in a two-port (TPE/AUI) application.

5.2 Design Guidelines

AUI Pulse Transformer

In order to meet the 16V fault tolerance specification of 802.3 a pulse transformer is recommended for the transmit, receive and collision pairs. The transformer should be placed between the TRMT, RCV, and CLSN pairs of the 503, and the DO, DI, and CI pairs respectively, of the AUI (DB-15 connector). The pulse transformer should have a parallel inductance of 75 μH minimum (100 μH recommended).

Several vendors stock such transformers. Two possible vendors are:

1. Pulse Engineering (P/N PE-64103)
2. Valor Electronics (P/N LT6003)

Terminating Resistors

The terminating resistors used across the receive and collision pairs are recommended to be 78.7 Ω ±1%.

Analog Front-End

The 82503 provides six TPE pins (TDH, $\overline{TDH}$, TDL, $\overline{TDL}$, RD, and $\overline{RD}$) that connect to the Analog Front End through a resistor summing network (Figure 7). AFE solutions can be made discretely or purchased from several manufacturers. Two different solutions are described in Application Note 356. The example shown here uses a Pulse Engineering AFE package PE65434 which includes EMI filter, isolation transformer, and common mode choke. The output of the AFE connects directly to the 10BASE-T connector (RJ-45).

Decoupling

It is recommended that 0.01 μF X7R and 0.001 μF NPO decoupling capacitors be placed between the V_{CCA} and V_{CCD} of the 82503 to V_{SSA} and V_{SSD}.

Clock Generation

The clock input to the 82503 can be from a clock oscillator or a crystal. If a clock oscillator is used, X1 should be driven, and X2 left floating. If a crystal oscillator is used, refer to Section 3.1 for crystal specifications.

A complete 82596/82503 TPE/AUI Ethernet Solution is shown at the end of this section.

5.3 Layout Guidelines

General

The analog section, as well as, the entire board itself should conform to good high-frequency practices and standards to minimize switching transients and parasitic interaction between various circuits. To achieve this, the following guidelines are presented.

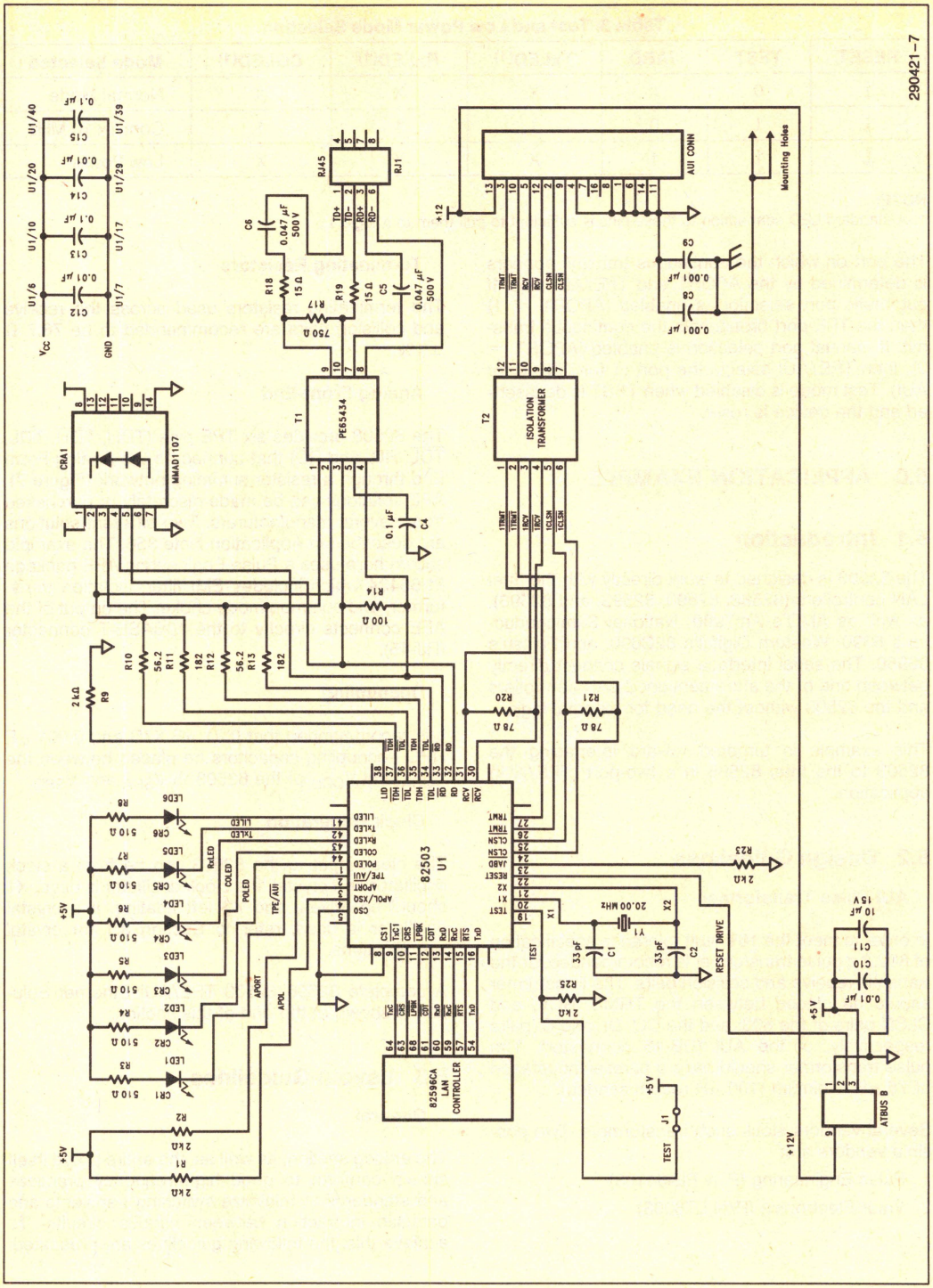


Figure 8. Application Example Schematic

Make power supply and ground traces as thick as possible. This will reduce high-frequency cross coupling caused by the inductance of thin traces.

Connect logic and chassis ground together.

Separate and decouple all of the analog and digital power supply lines.

Close signal paths to ground as close as possible to their sources to avoid ground loops and noise cross coupling.

Use high-loss magnetic beads on power supply distribution lines.

Crystal

The crystal should be adjacent to the 82503 and trace lengths should be as short as possible. The X1 and X2 traces should be symmetrical.

82503 Analog Differential Signals

The differential signals from the 82503 to the transformers, analog front end, and the connectors should be symmetrical for each pair and as short as possible. Differential signal layout should be performed to a characteristic impedance of 78Ω (for AUI) or 100Ω (for TPE).

As a general rule, the trace widths should be one to three times the distance between the PCB layers to eliminate excessive trace inductance.

The differential signals should also be isolated from the high speed logic signals on the same layer as well as on any sublayers of the PCB.

Group each of the circuits together, but keep them separate from each other. Separate their grounds.

In layout, the circuitry from the connectors to the filter network, should have the ground plane removed from beneath it. This will prevent ground noise from being induced into the analog front end.

All trace bends should not exceed 45 degrees.

6.0 PACKAGE THERMAL SPECIFICATIONS

The 82503 Dual Serial Transceiver is specified for operation when case temperature (T_C) is within the range of 0°C to +85°C. The case temperature can be measured in any environment, to determine if the 82503 is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The acceptable operating ambient temperature (T_A) is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from the θ_{ja} and θ_{jc} from the following equations:

$$T_J = T_C + P \times \theta_{jc}$$

$$T_J = T_A + P \times \theta_{ja}$$

$$T_A = T_C - P \times (\theta_{ja} - \theta_{jc})$$

Values for θ_{ja} and θ_{jc} are given in Table 4 for the 44-lead PLCC and 44-lead QFP packages. Various values for θ_{ja} at different airflows. Table 5 shows the maximum T_A allowable (without exceeding T_C) at various airflows.

Table 4. Thermal Resistance (°C/Watt) θ_{jc} and θ_{ja}

Package	θ_{jc}	θ_{ja} vs Airflow—ft/min (m/s)					
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
44-Lead PLCC	19	57	48	43	41	39	37
44-Lead QFP	26	98	94	78	70	66	64

Table 5. Maximum T_A at Various Airflows

Package	θ_{ja} vs Airflow—ft/min (m/s)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
44-Lead PLCC	66	71	73	74	75	76
44-Lead QFP	49	51	59	63	65	66

7.0 ELECTRICAL SPECIFICATIONS AND TIMINGS

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

ABSOLUTE MAXIMUM RATINGS

Case Temperature Under Bias . . . . . 0°C to +85°C
Storage Temperature . . . . . −65°C to +140°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +6.0V(1)

DC CHARACTERISTICS (T_C = 0°C to +85°C, V_{CC} = 5V ±5%, V_{CCA} = 5V ±5%)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}(TTL)(2)	Input Low Voltage	−0.3	0.8	V	
V_{IH}(TTL)(2)	Input High Voltage	2.0	V_{CC}	V	
I_{LI}(2)	Input Leakage Current		±10	μA	0.0V ≤ V_I ≤ V_{CC}, RESET = 1
V_{OL}(MOS)(3)	Output Low Voltage		0.45	V	I_{OL} = 4 mA
V_{OH}(MOS)	Output High Voltage	3.9		V	I_{OH} = −500 μA
V_{OL}(LED)(4)	Output Low Voltage		0.45	V	I_{OL} = 10 mA
V_{OH}(LED)	Output High Voltage	3.9		V	I_{OH} = −500 μA
I_{LP}	Leakage Current, Low Power Mode(5)		±10	μA	0.0V ≤ V_I ≤ V_{CC}
R_{DIFF}	Input Differential Resistance(6)	10		kΩ	dc
V_{IDF}(TPE)(7)	Input Differential Accept Input Differential Reject Input Differential Accept (XSQ) Input Differential Reject (XSQ)	±0.500 (Note 8) 	±3.1 ±0.300 ±3.1 ±0.180	V_P V_P V_P V_P	5 MHz ≤ f ≤ 10 MHz
R_S(TPE)(8)	Output Source Resistance	6	13	Ω	$\|I_{LOAD}\|$ = 25 mA
V_{IDF}(AUI)(9)	Input Differential Accept Input Differential Reject	±0.300	±1.5 ±0.160	V_P V_P	
V_{ODF}(AUI)(10)	Output Differential Voltage	±0.450	±1.20	V	

NOTES:
1. The voltage levels for RCV, CLSN, and RD pairs are −0.75V to +8.5V.
2. TTL Input Pins: TxD, $\overline{RTS}$, TPE/$\overline{AUI}$, APORT, APOL/XSQ, LID, CS0, CS1, $\overline{LPBK}$, JABD, TEST, RESET.
3. MOS Output Pins: $\overline{TxC}$, RxD, $\overline{RxC}$, $\overline{CRS}$, $\overline{CDT}$.
4. LED Pins: TPE/$\overline{AUI}$, TxLED, RxLED, COLED, POLED, LILED. V_{OL} measured 10 ns after falling edge of $\overline{TxC}$.
5. Pins: APORT, APOL/XSQ, LID, TPE/$\overline{AUI}$, POLED, LILED, $\overline{RTS}$, $\overline{LPBK}$, RxD, TxD, $\overline{CRS}$, $\overline{CDT}$, CS0, CS1, JABD, TEST, and RESET.
6. Pins: RD to $\overline{RD}$, RCV to $\overline{RCV}$, and CLSN to $\overline{CLSN}$.
7. TPE Input Pins: RD, and $\overline{RD}$. See Section 3.3.4 and Section 3.3.5.
8. Typically it is −4.5 dB below normal squelch level.
9. TPE Output Pins: TDH, $\overline{TDH}$, TDL, and $\overline{TDL}$. R_S measures V_{CC} or V_{SS} to Pin.
10. AUI Input Pins: RCV, and CLSN pairs.
11. AUI Output Pins: TRMT pair.

DC CHARACTERISTICS (T_C = 0°C to +85°C, V_{CC} = 5V ±5%, V_{CCA} = 5V ±5%) (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{OSC}(AUI)	AUI Output Short Circuit Current		±150	mA	Short Circuit to V_{CC} or GND
V_U(AUI)	Output Differential Undershoot		−100	mV	
V_{ODI}(AUI)	Differential Idle Voltage(11)		±40	mV	
I_{CC}(HOT)	Power Supply Current(12)		65	mA	APORT = 1
I_{CC}	Power Supply Current		75	mA	APORT = 1
I_{CC}	Power Supply Current		60	mA	APORT = 0
I_{CCSB}	Standby Supply Current(13)		1	mA	Low Power Mode, 20 μA Typical
PD (HOT)	Power Dissipation(12)		0.38	W	APORT = 1, Continuous Transmission on AUI
PD	Power Dissipation		0.40	W	APORT = 1, Continuous Transmission on AUI
PD_{SB}	Standby Power Dissipation(13)		5.25	mW	Low Power Mode, 105 μW Typical
C_{IN}(14)	Input Capacitance		10	pF	at f = 1 MHz

NOTES:
11. Measured 8.0 μs after last positive transition of data packet.
12. I_{CC} HOT measurements made at T_C = +85°C. Additionally, TRMT, $\overline{\text{TRMT}}$, TDH, $\overline{\text{TDH}}$, TDL, $\overline{\text{TDL}}$ are loaded with 20 pF and load resistors removed.
13. Pins CS0 and CS1 connected to V_{CC} or V_{SS} through a 2.5 kΩ (or less) resistor. I_{CCSB} is typically at 20 μA after 30s from power down assertion—not tested.
14. Characterized, not tested. (Controller interface and mode pins only.)

AC TIMING CHARACTERISTICS

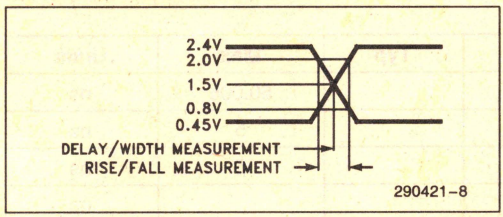


Figure 9. MOS Input Voltage Levels (TTL Compatible) for Timing Measurements (TxD, $\overline{\text{RTS}}$, TPE/$\overline{\text{AUI}}$, APORT, APOL/XSQ, LID, $\overline{\text{LPBK}}$, JABD, TEST, and RESET).

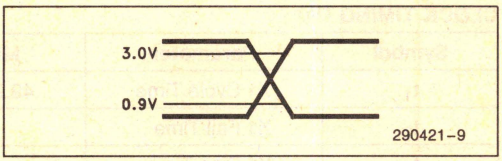


Figure 10. Voltage Levels for MOS Level Output Timing Measurements ($\overline{\text{TxC}}$, RxD, $\overline{\text{RxC}}$, $\overline{\text{CRS}}$, and $\overline{\text{CDT}}$).

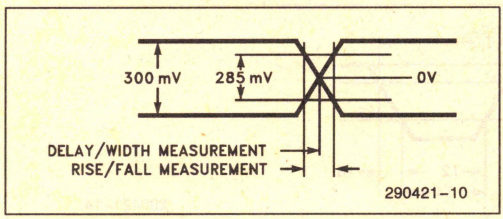


Figure 11. Voltage Levels for Differential Input Timing Measurements (RCV and CLSN Pairs).

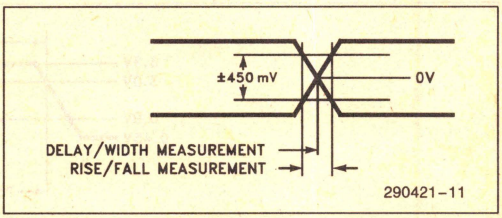


Figure 12. Voltage Levels for TRMT Pair Output Timing Measurements.

AC TIMING CHARACTERISTICS (Continued)

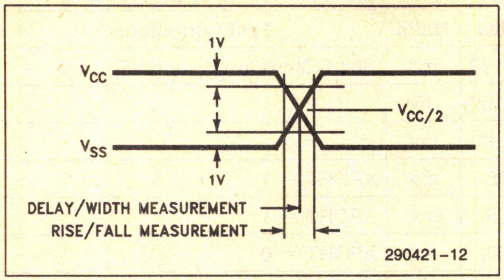


Figure 13. Voltage Levels for TDH, TDL, $\overline{TDH}$, and $\overline{TDL}$.

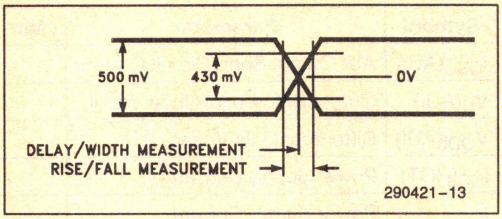


Figure 14. Voltage Levels for Differential Input Timing Measurements (RD Pair).

AC MEASUREMENT CONDITIONS

1. T_C = 0°C to +85°C, V_{CC} = 5V ±5%.
2. The AC MOS, TTL and differential signals are referred to in Figures, 8, 9, 10, 11, 12, and 13.
3. AC loads
   a. MOS: 20 pF total capacitance to ground.
   b. AUI Differential: a 10 pF total capacitance from each terminal to ground and a load resistor of 78Ω ±1% in parallel with a 27 μH ±1% inductor between terminals.
   c. TPE: 20 pF total capacitance to ground.
4. All parameters become valid 200 μs after the supply voltage and input clock has stabilized, or after RESET deasserts.

CLOCK TIMING (15)

Symbol	Parameter	Min	Typ	Max	Units
t_1	X1 Cycle Time	49.995		50.005	ns
t_2	X1 Fall Time			5	ns
t_3	X1 Rise Time			5	ns
t_4	X1 Low Time	15			ns
t_5	X1 High Time	15			ns

NOTE:
15. Refers to External Clock Input.

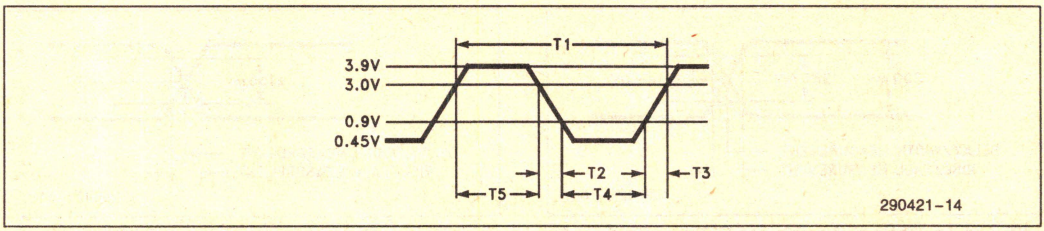


Figure 15. X1 Input Voltage Levels for Timing Measurements

Controller Interface Timings (Intel Mode)

TRANSMIT TIMINGS (Intel)

Symbol	Parameter	Min	Typ	Max	Units
t_{10}	$\overline{TxC}$ Cycle Time	99.99		100.01	ns
t_{11}	$\overline{TxC}$ High/Low Time	40			ns
t_{12}	$\overline{TxC}$ Rise/Fall Time			5	ns
t_{13}	TxD and $\overline{RTS}$ Rise/Fall Time			10	ns
t_{14}	TxD Setup Time to $\overline{TxC}$ ↓	45			ns
t_{15}	TxD Hold Time from $\overline{TxC}$ ↓	0			ns
t_{16}	$\overline{RTS}$ Setup Time to $\overline{TxC}$ ↓	45			ns
t_{17}	$\overline{RTS}$ Hold Time from $\overline{TxC}$ ↓	0			ns

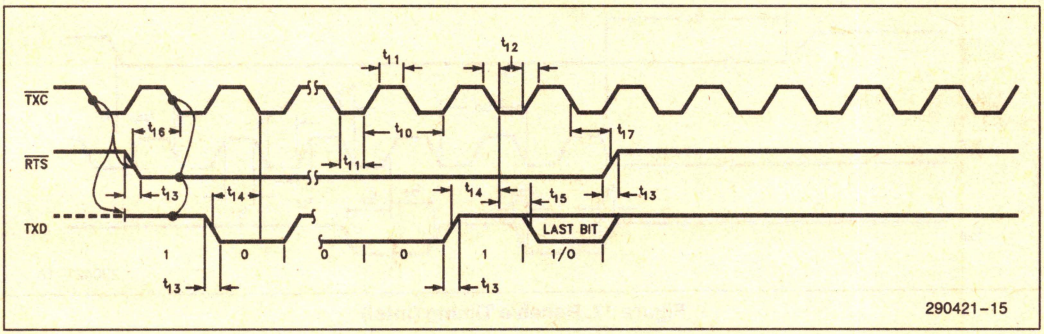


Figure 16. Transmit Timing (Intel)

RECEIVE TIMING (Intel)

Symbol	Parameter	Min	Typ	Max	Units
t_{20}	$\overline{RxC}$ Cycle Time	96	100		ns
t_{21}	$\overline{RxC}$ High Time	36			ns
t_{22}	$\overline{RxC}$ Low Time	40			ns
t_{23}	$\overline{RxC}$ Rise/Fall Time			5	ns
t_{24}	$\overline{RxC}$ Delay from $\overline{CRS}$ ↓		1100	1400	ns
t_{25}	RxD Rise/Fall Time			5	ns
t_{26}	RxD Setup from $\overline{RxC}$ ↓	30			ns
t_{27}	RxD Hold from $\overline{RxC}$ ↓	30			ns
t_{28}	$\overline{CRS}$ Deassertion Hold Time from $\overline{RxC}$ High	10		40	ns

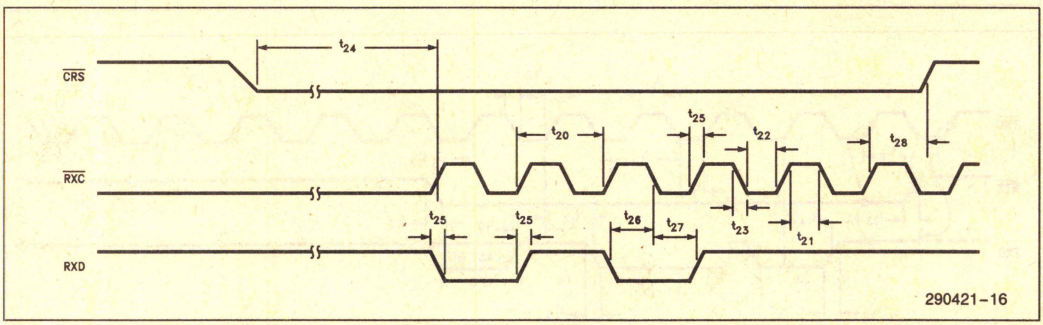


Figure 17. Receive Timing (Intel)

Controller Interface Timings (National Mode)

TRANSMIT TIMINGS (National)

Symbol	Parameter	Min	Typ	Max	Units
t_{30}	TXC Cycle Time(16)	99.99		100.01	ns
t_{31}	TXC High/Low Time	40	50		ns
t_{32}	TXC Rise/Fall Time at 20% to 80%			5	ns
t_{33}	TXD Setup Time to TXC ↑	20			ns
t_{34}	TXD Hold Time from TXC ↑	0			ns
t_{35}	TXE Setup Time to TXC ↑	20			ns
t_{36}	TXE Hold Time from TXC ↑	0			ns

NOTE:
16. All delay and width measurements on TxC are made at 1.5V.

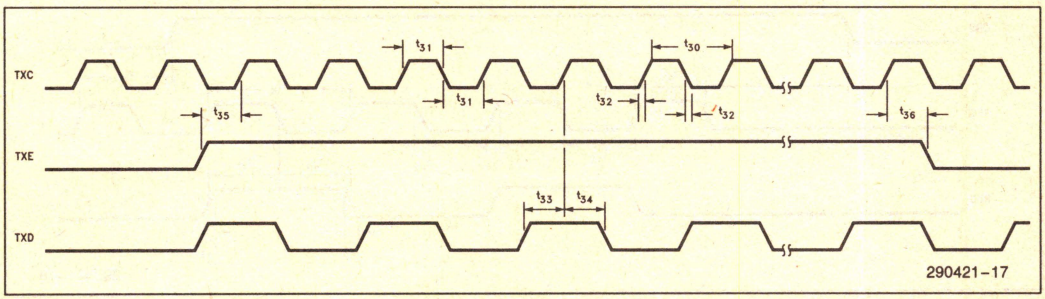


Figure 18. Transmit Timing (National)

RECEIVE TIMINGS (National)

Symbol	Parameter	Min	Typ	Max	Units
t_{40}	RxC Cycle Time	96	100		ns
t_{41}	RxC High/Low Time(17)	40	50	60	ns
t_{42}	RxC Rise/Fall Time at 20% to 80%			5	ns
t_{43}	RXD Rise/Fall Time at 20% to 80%			5	ns
t_{44}	RXD Setup Time to RxC ↑	30			ns
t_{45}	RXD Hold Time from RxC ↑	20			ns
t_{46}	RxC Delay from CRS ↑			1400	ns
t_{47}	RxC Continuing Beyond CRS ↓			5	cycles

NOTE:
17. All delay and width measurements on RXC are made at 1.5V.

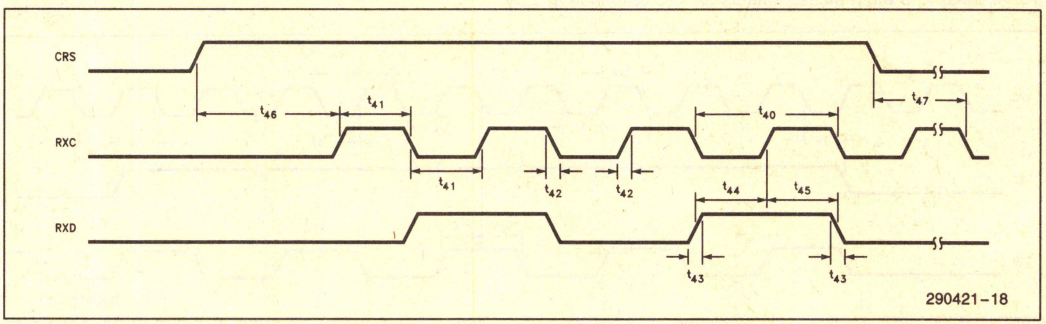


Figure 19. Receiving Timings (National)

Controller Interface Timing (AMD Mode)

TRANSMIT TIMINGS[18] (AMD)

Symbol	Parameter	Min	Typ	Max	Units
t_{50}	TCLK Cycle Time	99.99		100.01	ns
t_{51}	TCLK High Time (@ 0.8V to 2.0V)	45	50	58	ns
t_{52}	TCLK Low Time (@ 2.0V to 0.8V)	45	50	58	ns
t_{53}	TCLK Rise/Fall Time (@ 0.8V to 2.0V)		2.5	5	ns
t_{54}	TX Setup Time to TCLK ↑	20			ns
t_{55}	TX Hold Time from TCLK ↑	5			ns
t_{56}	TENA Setup Time to TCLK ↑	20			ns
t_{57}	TENA Hold Time from TCLK ↑	5			ns

NOTE:
18. Delay times for TX, TENA, and TCLK are measured from 0.8V for falling edges, and 2.0V for rising edges.

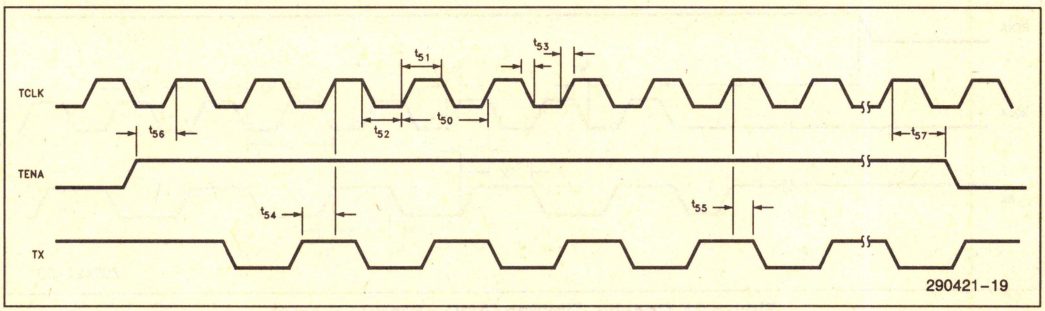


Figure 20. Transmit Timings (AMD)

RECEIVE TIMINGS[19] (AMD)

Symbol	Parameter	Min	Typ	Max	Units
t_{60}	RCLK Cycle Time	96	100		ns
t_{61}	RCLK High Time (@ 0.8V to 2.0V)	38	50		ns
t_{62}	RCLK Low Time (@ 2.0V to 0.8V)	38	50		ns
t_{63}	RCLK Rise/Fall Time (@ 0.8V to 2.0V)		2.5	5	ns
t_{64}	RX Rise/Fall Time (@ 0.8V to 2.0V)		2.5	5	ns
t_{65}	RX Hold time from RCLK ↑	10			ns
t_{66}	RX Setup Time to RCLK ↑	45			ns
t_{67}	RENA Deassertion Hold Time from RCLK ↑	40	50	80	ns
t_{68}	RCLK Delay from RENA ↑			450	ns

NOTE:
19. Delay times for RX, RENA, and RCLK are measured from 0.8V for falling edges and 2.0V for rising edges.

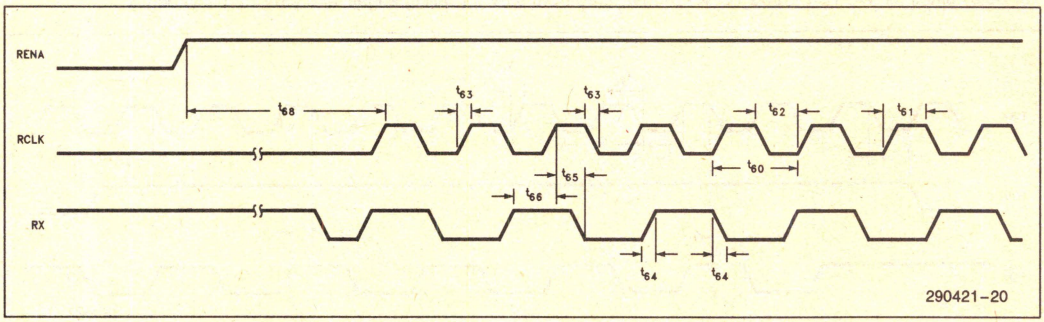


Figure 21. Receive Timings (AMD—Start of Frame)

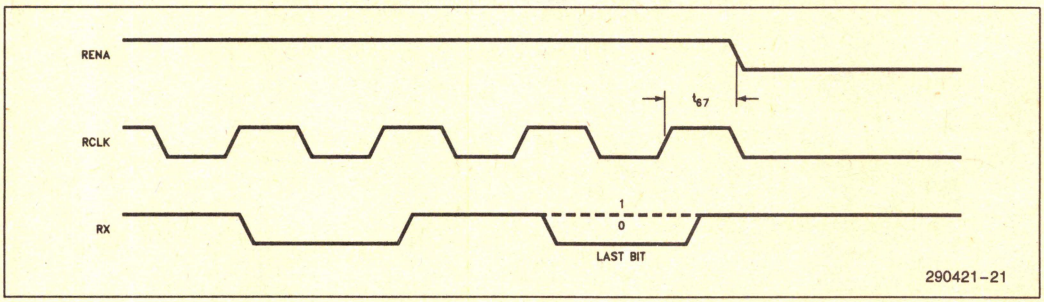


Figure 22. Receive Timings (AMD—End of Frame)

Controller Interface Timings (Fujitsu Mode)

TRANSMIT TIMINGS (Fujitsu)

Symbol	Parameter	Min	Typ	Max	Units
t_{70}	TCKN Cycle Time	99.99		100.01	ns
t_{71}	TCKN High/Low Time(20)	40	50		ns
t_{72}	TCKN Rise/Fall Time at 20% to 80%			5	ns
t_{73}	TXD Setup Time to TCKN ↓ (20)	20			ns
t_{74}	TXD Hold Time from TCKN ↓ (20)	0			ns
t_{75}	TEN Setup Time to TCKN ↓ (20)	20			ns
t_{76}	TEN Hold Time from TCKN ↓ (20)	0			ns

NOTE:
20. Timing measurements are referenced at 1.5V level.

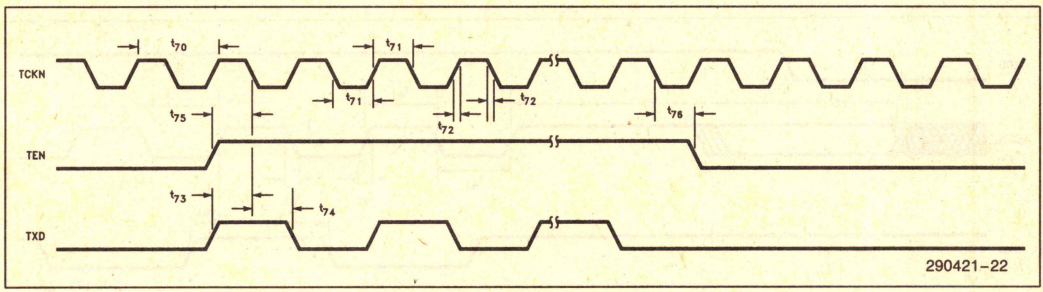


Figure 23. Transmit Timings (Fujitsu)

RECEIVE TIMINGS (Fujitsu)

Symbol	Parameter	Min	Typ	Max	Units
t_{80}	RCKN Cycle Time	96	100		ns
t_{81}	RCKN High/Low Time(21)	35	50	60	ns
t_{82}	RCKN Rise/Fall Time at 20% to 80%			5	ns
t_{83}	RXD Setup Time from RCKN ↓ (21)	20			ns
t_{84}	RXD Hold Time from RCKN ↓ (21)	10			ns
t_{85}	XCD Assertion Hold Time from RCKN ↓ (21)	0	10		ns
t_{86}	XCD Deassertion Hold Time from RCKN ↓ (21)		120		ns
t_{87}	XCD Deassertion Setup Time from RCKN ↓ (21)		80	130	ns
t_{88}	RCKN Delay from XCD ↑ (21)			1400	ns

NOTE:
21. Timing measurements are referenced at 1.5V.

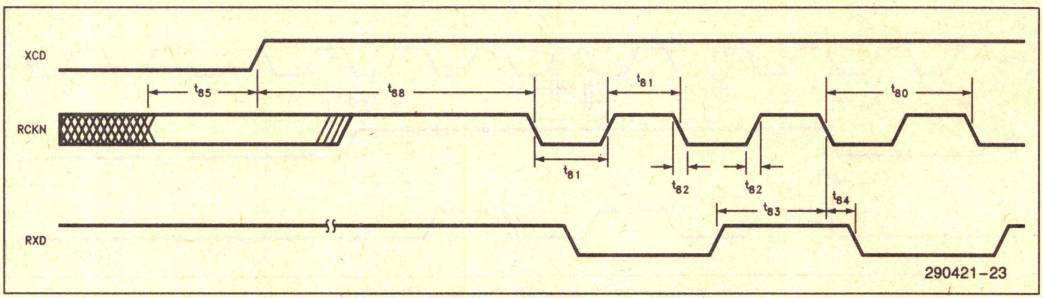


Figure 24. Receive Timings (Fujitsu—Start of Frame)

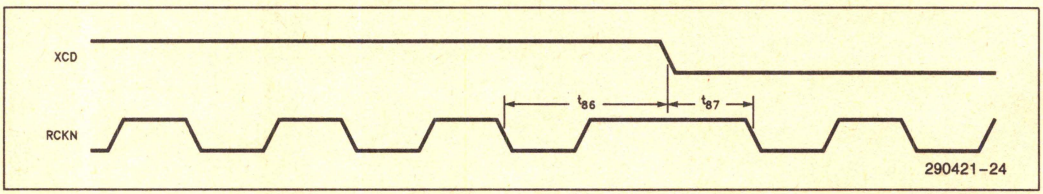


Figure 25. Receive Timings (Fujitsu—End of Frame)

TPE Timings

TPE TRANSMIT TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{90}	TxD to TD Bit Loss at Start of Packet			2	bits
t_{91}	TxD to TD Steady State Propagation Delay			400	ns
t_{92}	TxD to TD Startup Delay			600	ns
t_{93}	TDH and TDL Pairs Edge Skew (@ $V_{CC}/2$)		1.5	3	ns
t_{94}	TDH and TDL Pairs Rise/Fall Times (@ 0.5V to V_{CC} − 0.5V)		2	5	ns
t_{95}	TDH and TDL Pairs Bit Cell Center to Center	99	100	101	ns
t_{96}	TDH and TDL Pairs Bit Cell Center to Boundary	49	50	51	ns
t_{97}	TDH and TDL Pairs Return to Zero from Last TDH ↑	250		400	ns
t_{98}	Link Test Pulse Width	98	100	102	ns
t_{99}	Last TD Activity to Link Test Pulse	8	13	24	ms
t_{100}	Link Test Pulse to Data Separation	190	200		ns

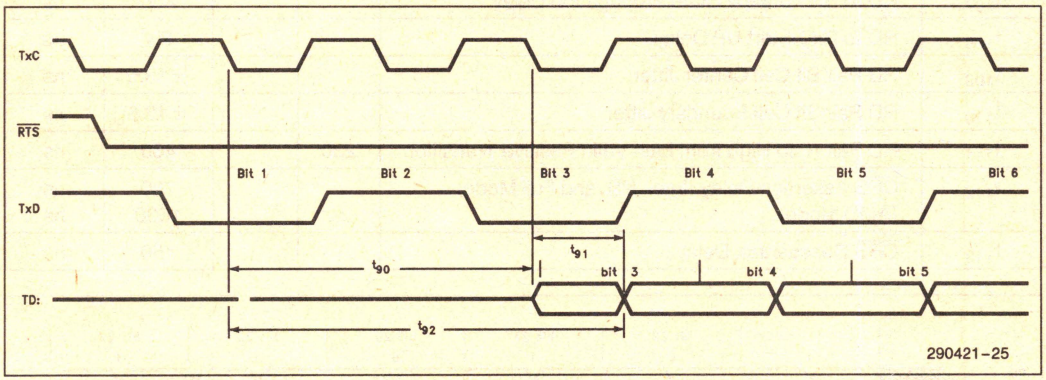


Figure 26. TPE Transmit Timings (Start of Frame)

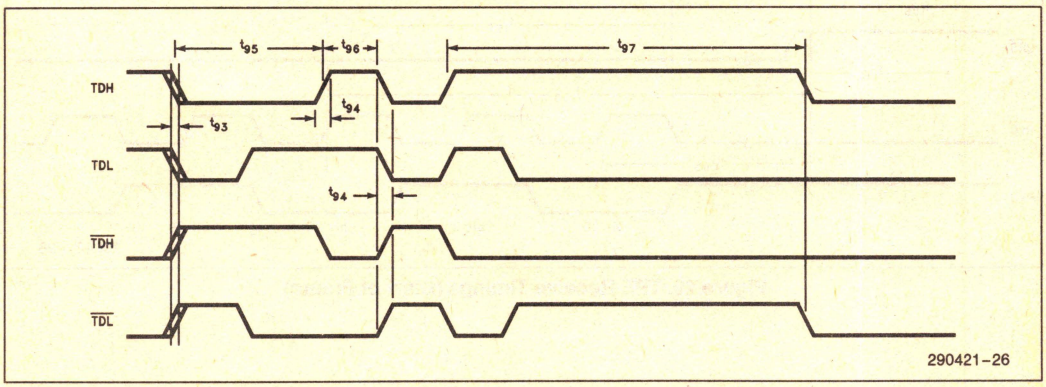


Figure 27. TPE Transmit Timings (End of Frame)

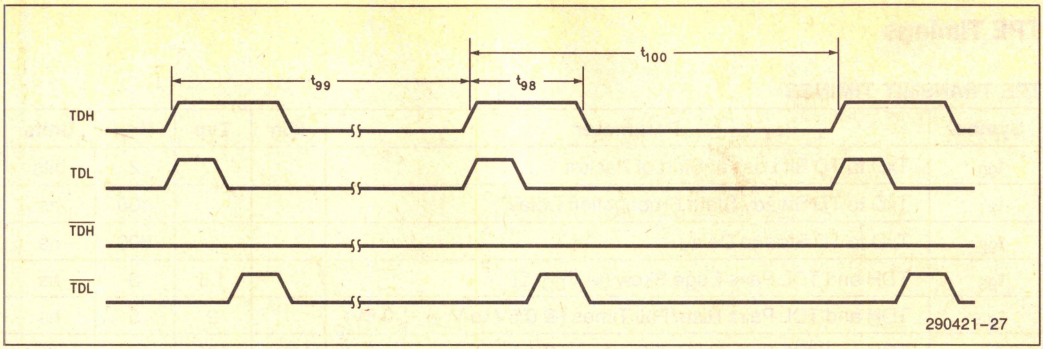


Figure 28. TPE Transmit Timings (Link Test Pulse)

TPE RECEIVE TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{105}	RD to RxD Bit Loss at Start of Packet	4		19	bits
t_{106}	RD to RxD Invalid Bits Allowed at Start of Packet			1	bits
t_{107}	RD to RxD Steady State Propagation Delay			400	ns
t_{108}	RD to RxD Start UP Delay			2.4	μs
t_{109}	RD Pair Bit Cell Center Jitter			±13.5	ns
t_{110}	RD Pair Bit Cell Boundary Jitter			±13.5	ns
t_{111}	RD Pair Held High from Last Valid Positive Transition	230		400	ns
t_{112}	$\overline{CRS}$ Assertion Delay (Intel, NS, and Fuji Mode) (AMD Mode)			700 1500	ns ns
t_{113}	$\overline{CRS}$ Deassertion Delay			450	ns

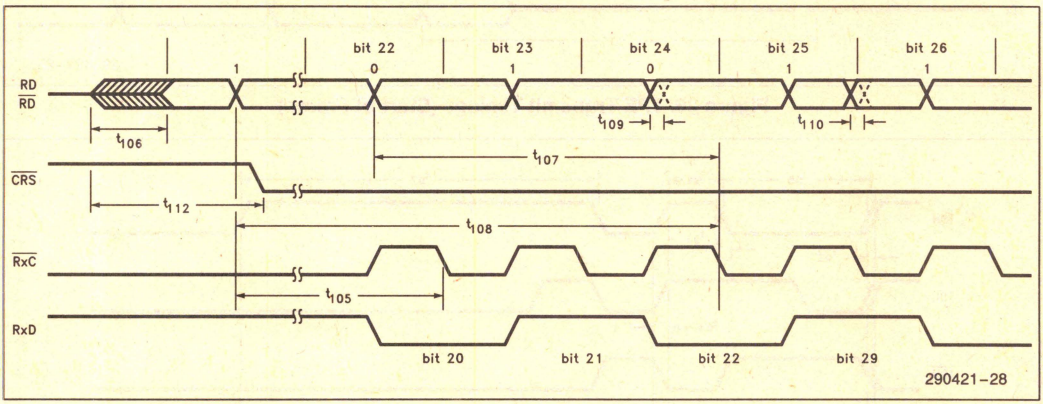


Figure 29. TPE Receive Timings (Start of Frame)

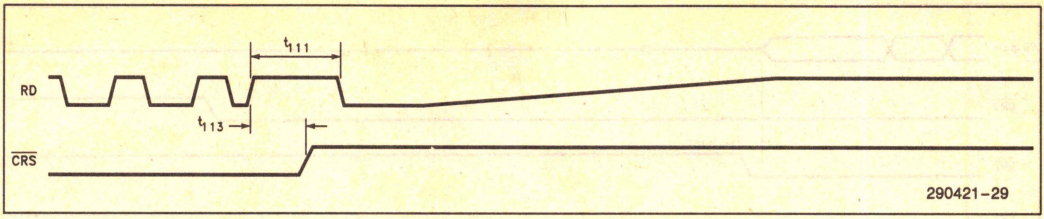


Figure 30. TPE Receive Timings (End of Frame)

TPE COLLISION TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{115}	Onset of Collision (RD Pair and $\overline{RTS}$ Active) to $\overline{CDT}$ Assert			900	ns
t_{116}	End of Collision (RD Pair or $\overline{RTS}$ Inactive) to $\overline{CDT}$ Deassert			900	ns
t_{117}	$\overline{CDT}$ Assert to RxD Sourced from RD Pair			900	ns
t_{118}	$\overline{CDT}$ Deassert (RD Pair Inactive) to RxD Sourced from TxD			900	ns

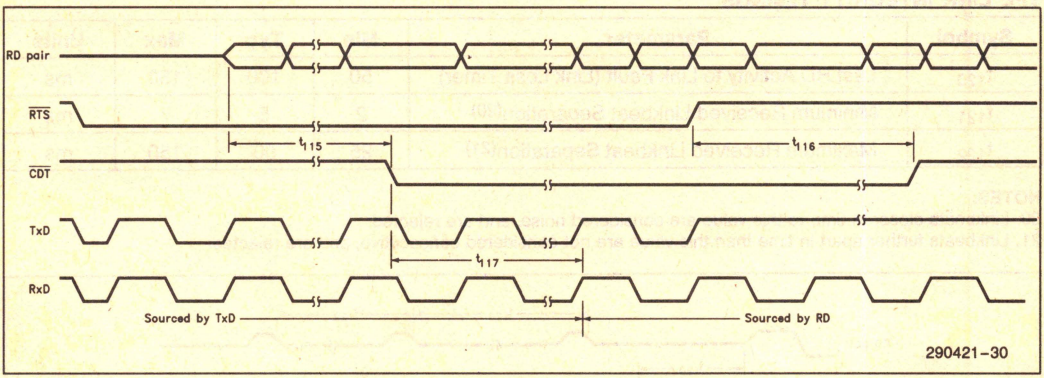


Figure 31. TPE Collision Timings (Start of Collision)

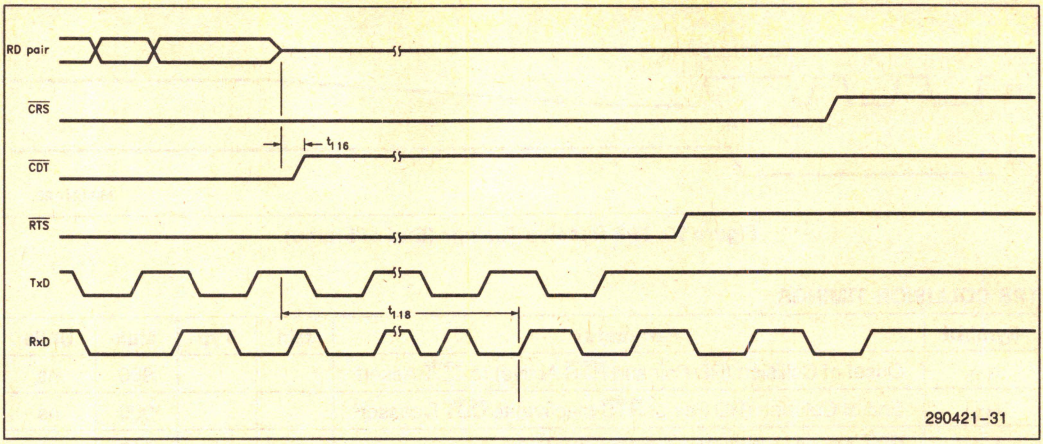


Figure 32. TPE Collision Timings (End of Collision)

TPE LINK INTEGRITY TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{120}	Last RD Activity to Link Fault (Link Loss Timer)	50	100	150	ms
t_{121}	Minimum Received Linkbeat Separation(20)	2	5	7	ms
t_{122}	Maximum Received Linkbeat Separation(21)	25	50	150	ms

NOTES:
20. Linkbeats closer in time to this value are considered noise, and are rejected.
21. Linkbeats further apart in time than this value are not considered consecutive, and are rejected.

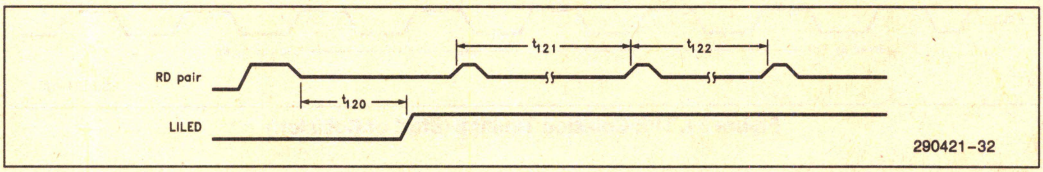


Figure 33. TPE Link Integrity Timings

AUI Timings

AUI TRANSMIT TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{125}	TxD to TRMT Pair Steady State Propagation Delay			200	ns
t_{126}	TRMT Pair Rise/Fall Times		3	5	ns
t_{127}	Bit Cell Center to Bit Cell Center of TRMT Pair	99.5	100	100.5	ns
t_{128}	Bit Cell Center to Bit Cell Boundary of TRMT Pair	49.5	50	50.5	ns
t_{129}	TRMT Pair Held at Positive Differential at Start of Idle	200			ns
t_{130}	TRMT Pair Return to ≤ 40 mV from Last Positive Transition			8.0	μs

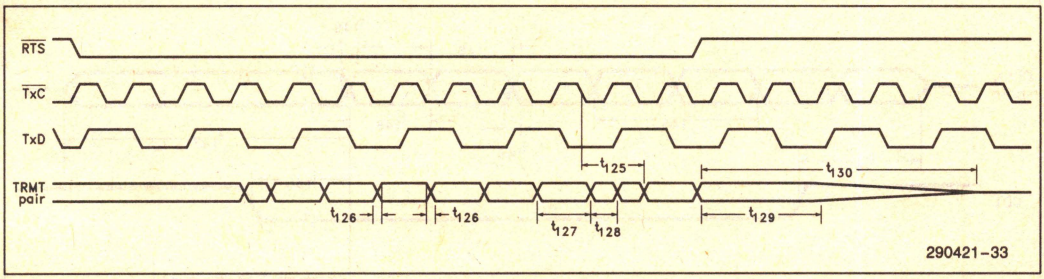


Figure 34. AUI Transmit Timings

AUI RECEIVE TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{135}	RCV Pair Rise/Fall Times			10	ns
t_{136}	RCV Pair Bit Cell Center Jitter in Preamble			±12	ns
t_{137}	RCV Pair Bit Cell Center/Boundary Jitter in Data			±18	ns
t_{138}	RCV Pair Idle Time after Transmission	8			μs
t_{139}	RCV Pair Return to Zero from Last Positive Transition	160			ns
t_{140}	$\overline{CRS}$ Assertion Delay (Intel, National, Fujitsu Modes) (AMD Mode)			100 1050	ns ns
t_{141}	$\overline{CRS}$ Deassertion Delay			350	ns
t_{142}	$\overline{CRS}$ Inhibited after Frame Transmission	4	4.3	5	μs

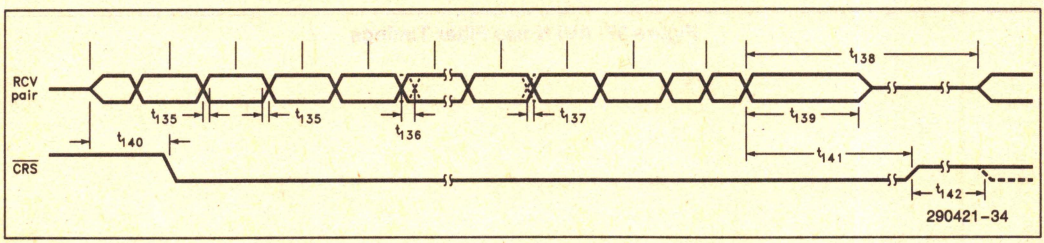


Figure 35. AUI Receive Timings

AUI COLLISION TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{145}	CLSN Pair Cycle Time	80		118	ns
t_{146}	CLSN Pair Rise/Fall Times			10	ns
t_{147}	CLSN Pair Return to Zero from Last Positive Transition	160			ns
t_{148}	CLSN Pair High/Low Times	35		70	ns
t_{149}	$\overline{CDT}$ Assertion Time			75	ns
t_{150}	$\overline{CDT}$ Deassertion Time			300	ns
t_{151}	$\overline{CRS}$ Deassertion Time (Intel Mode Only, RCV Pair Idle)			450	ns

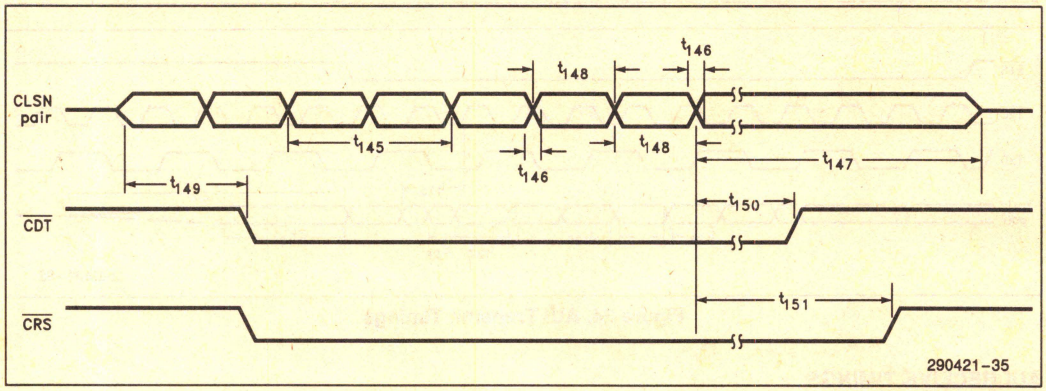


Figure 36. AUI Collision Timings

AUI NOISE FILTER TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{152}	RCV Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns
t_{153}	CLSN Pair Noise Filter Pulse Width Accept (@ −285 mV)	25			ns

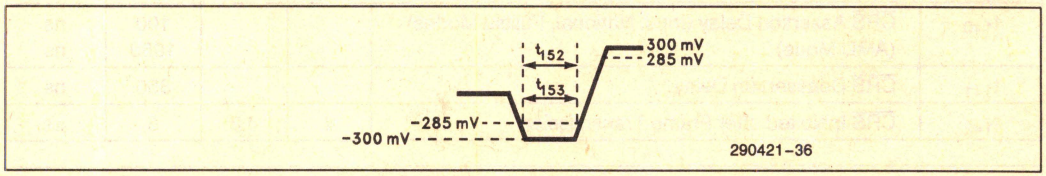


Figure 37. AUI Noise Filter Timings

LOOPBACK TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{155}	TxD to RxD Bit Loss at Start of Packet			16	bits
t_{156}	TxD to RxD Steady State Propagation Delay			600	ns
t_{157}	TxD to RxD Startup Delay			2.2	μs
t_{158}	SQE Test Wait Time	0.6	1.2	1.6	μs
t_{159}	SQE Test Duration	0.5	0.8	1.5	μs
t_{160}	$\overline{LPBK}$ Setup/Hold Times to $\overline{RTS}$(22)	1.0			μs

NOTE:
22. Guarantees proper processing of transmitted packets. Violation of this specification will not result in spurious data transmission. Incoming data packets occuring during transitions on $\overline{LPBK}$ will not be accepted.

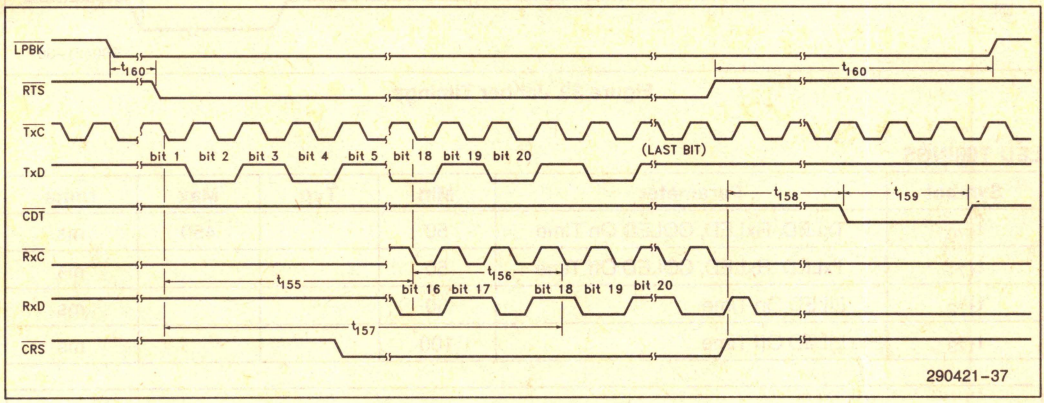


Figure 38. Loopback Timings

JABBER TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{165}	Maximum Length Transmission before Jabber Fault (TPE)	20	25	150	ms
t_{166}	Maximum Length Transmission before Jabber Fault (AUI)	10	13	18	ms
t_{167}	Minimum Idle Time to Clear Jabber Function	250	420	750	ms

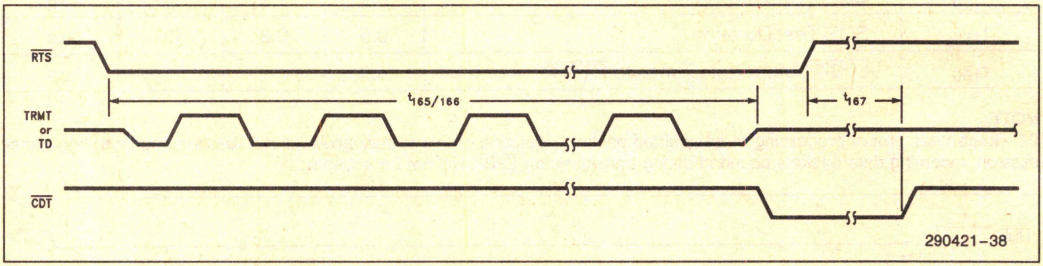


Figure 39. Jabber Timings

LED TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{170}	TxLED, RxLED, COLED On Time	50		450	ms
t_{171}	TxLED, RxLED, COLED Off Time	50			ms
t_{172}	LILED On Time	50			ms
t_{173}	LILED Off Time	100			ms

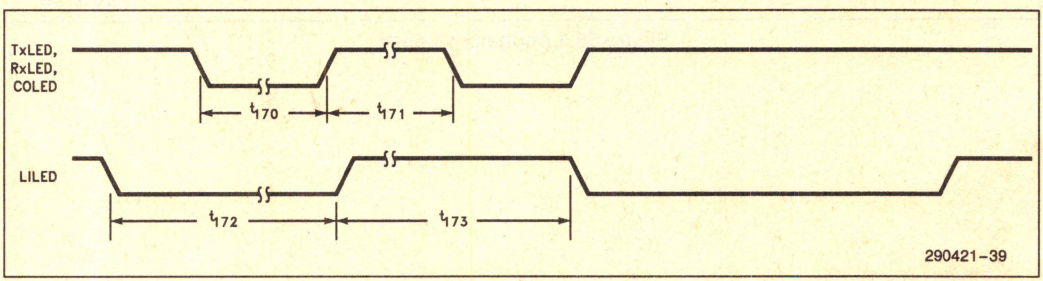


Figure 40. LED Timings

MODE TIMINGS(23, 24)

Symbol	Parameter	Min	Typ	Max	Units
t_{175}	Mode Pins Setup to $\overline{RTS}$ ↓	100			ms
t_{176}	Mode Pins Hold from $\overline{RTS}$ ↑	100			ms
t_{177}	Mode Pins Setup to RD Active(25)	100			ms
t_{178}	Mode Pins Hold from RD Active(25)	100			ms

NOTES:
23. Guarantees Proper processing of data packets. Violation of these specifications will not affect the integrity of the network.
24. Mode pins are: APORT, APOL/XSQ, LID, JABD, and TPE/$\overline{AUI}$.
25. Any data received within 100 ms of a mode transmission will be considered invalid.

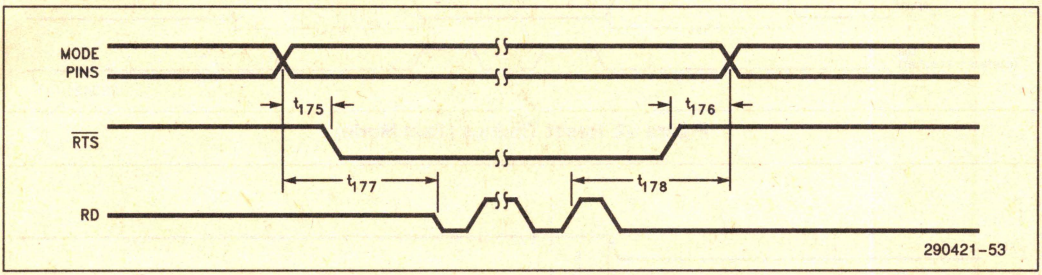


Figure 41. Mode Timings

RESET, TEST, AND LOW POWER MODE TIMINGS

Symbol	Parameter	Min	Typ	Max	Units
t_{180}	TEST and JABD Setup Time to RESET ↓	50			ns
t_{181}	RESET Pulse Width	300			ns
t_{182}	Low Power Mode Deactivation from TEST and JABD ↓			1	ms

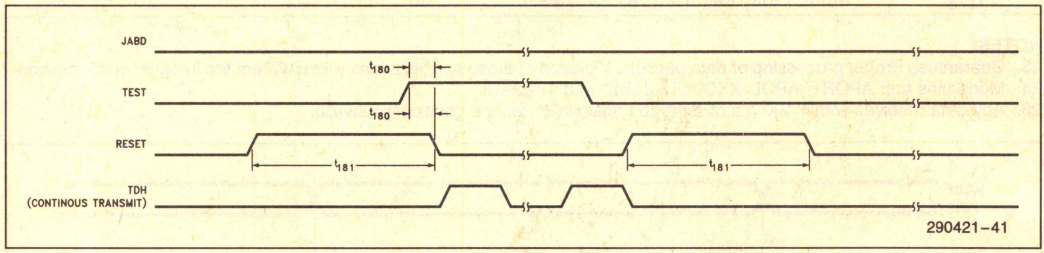


Figure 42. Reset Timings (Test Mode)

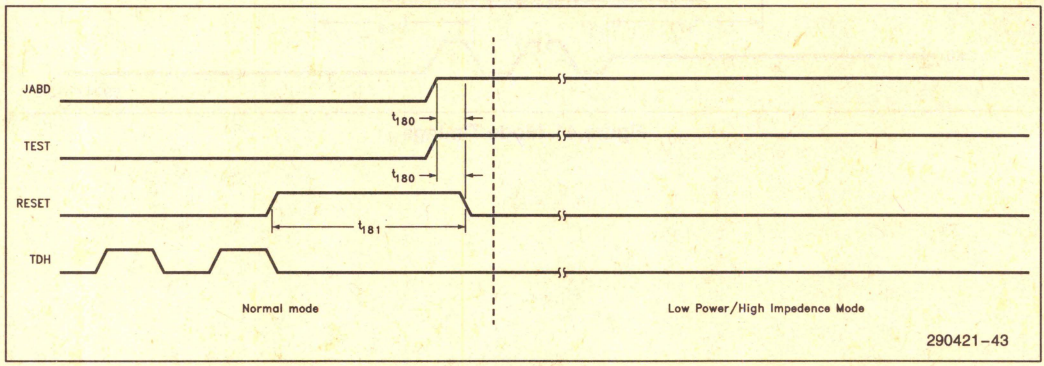


Figure 43. Reset Timings (Start of Low Power Mode)

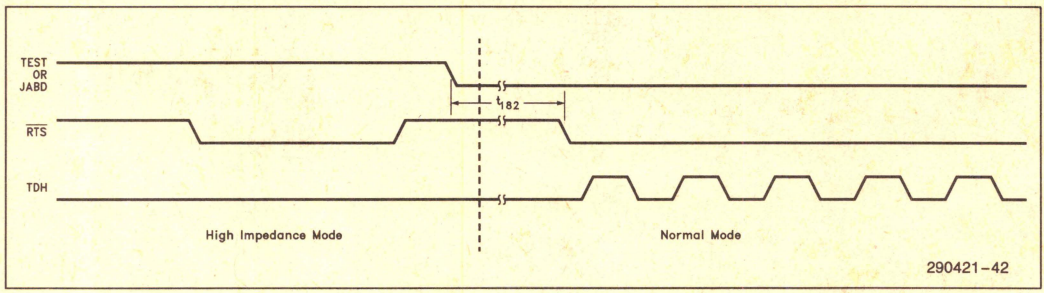


Figure 44. Reset Timings (End of Low Power Mode)

PACKAGE DIMENSIONS

PLASTIC LEADED CHIP CARRIER

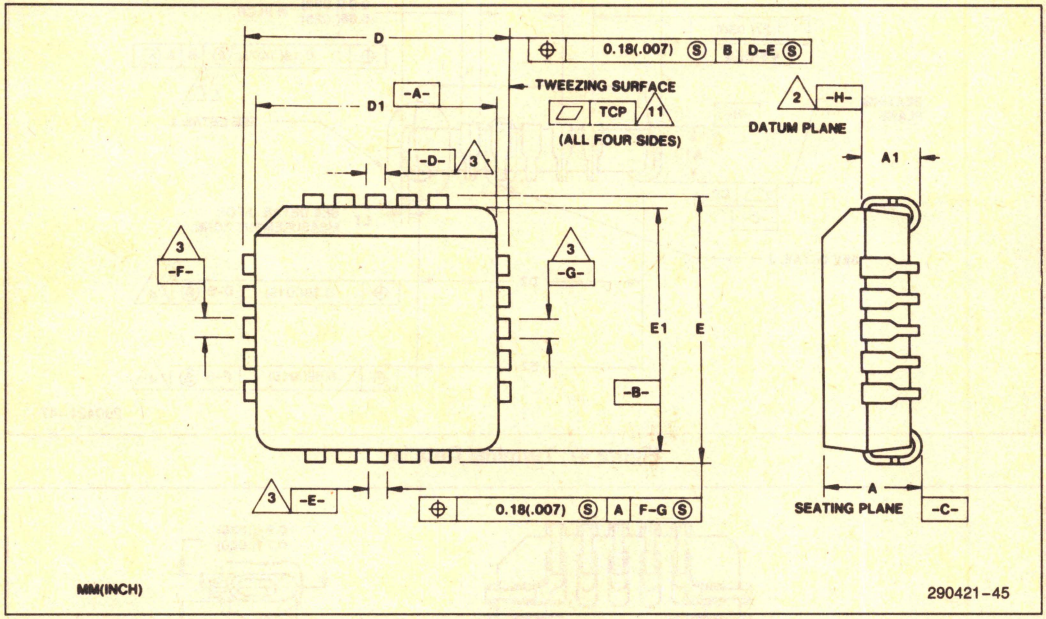


Figure 45. Principle Dimensions and Data

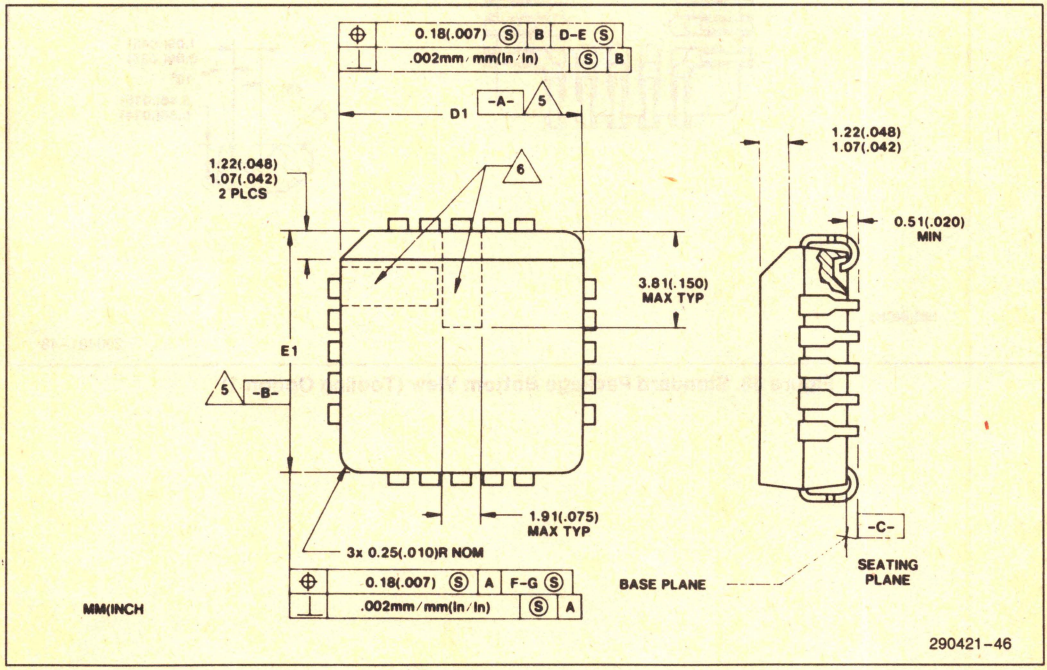


Figure 46. Molded Details

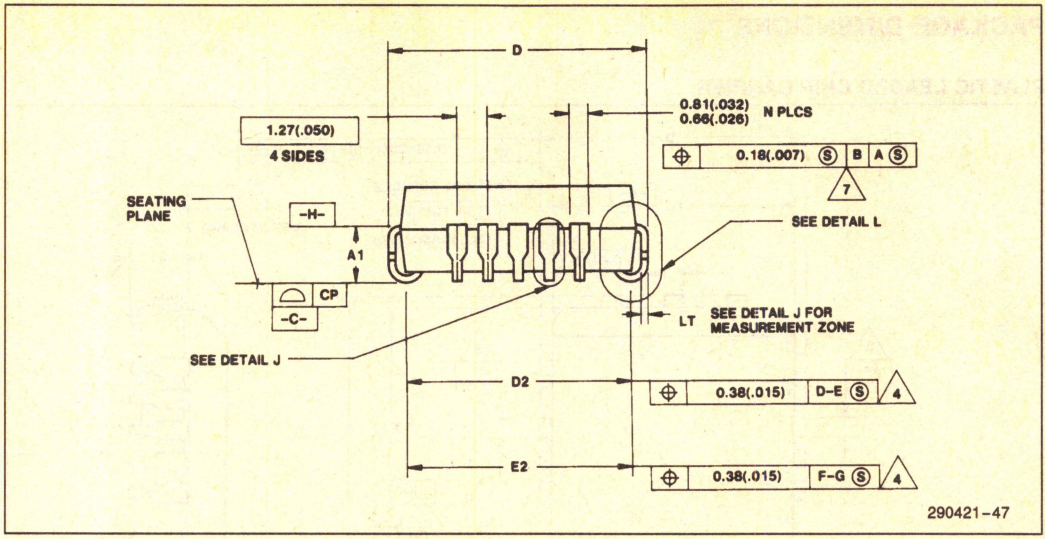


Figure 47. Terminal Details

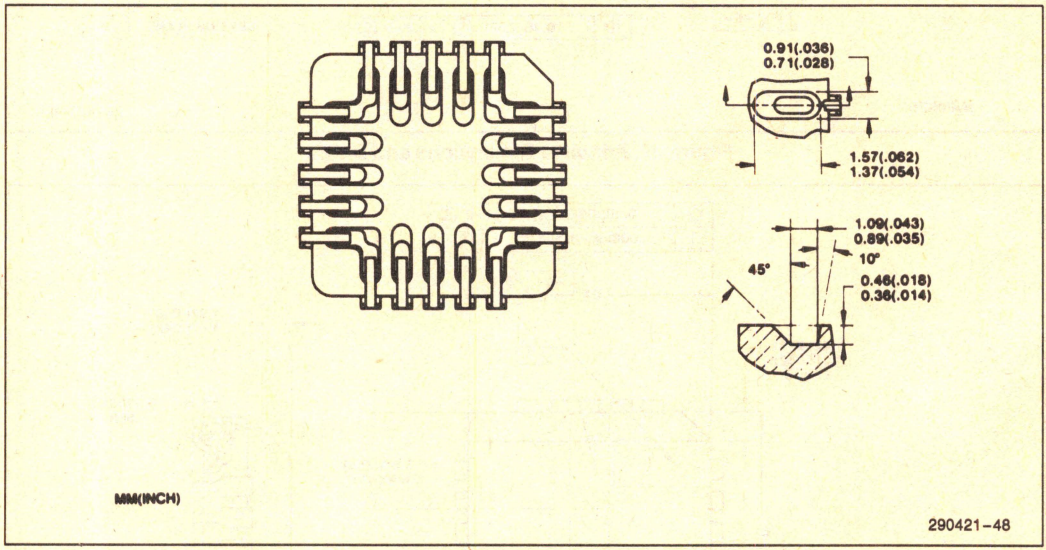


Figure 48. Standard Package Bottom View (Tooling Option 1)

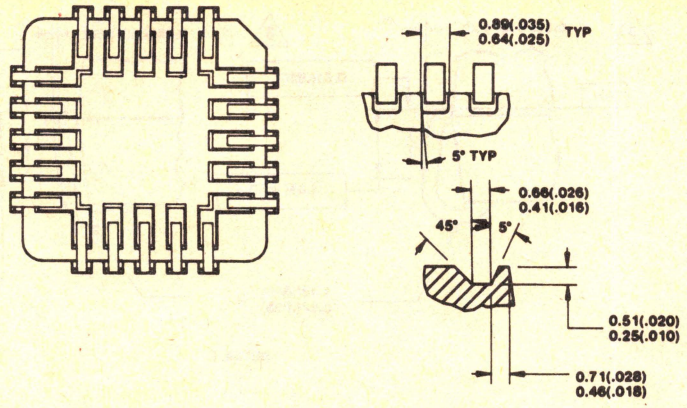


Figure 49. Standard Package Bottom View (Tooling Option II)

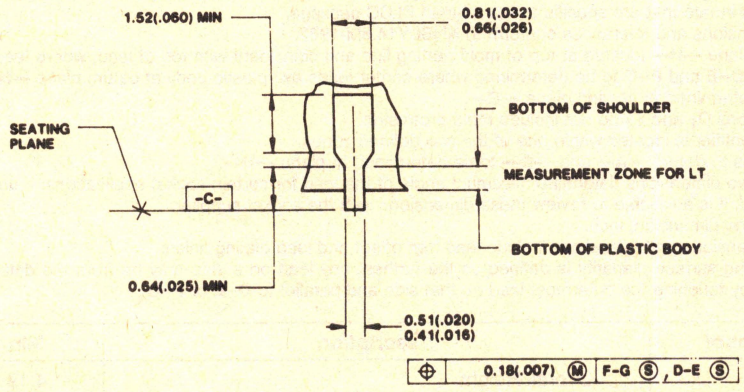


Figure 50. Detail J. Terminal Detail

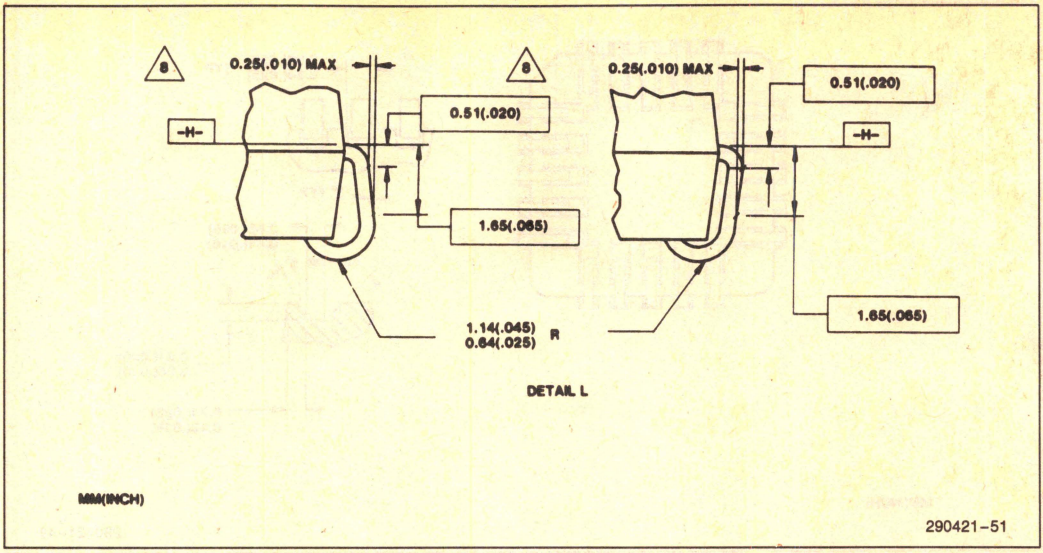


Figure 51. Detail L. Terminal Details

NOTES:
The above diagrams use a 20-lead PLCC package to show symbols for package dimensions. The table below indicates dimensions in mm that are specific to the 44-lead PLCC package.
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **—H—** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Datums **D–E** and **F–G** to be determined where center leads exit plastic body at datum plane **—H—**.
4. To be determined at seating plane **—C—**.
5. Dimensions D_1 and E_1 do not include mold protrusion.
6. Pin 1 identifier is located within one of the two defined zones.
7. Locations to datum **—A—** and **—B—** to be determined at plane **—H—**.
8. These two dimensions determine maximum angle of the lead for certain socket applications. If unit is intended to be socketed, it is advisable to review these dimensions with the socket supplier.
9. Controlling dimension, inch.
10. All dimensions and tolerances include lead trim offset and lead plating finish.
11. Tweezing surface planarity is defined as the furthest any lead on a side may be from the datum. The datum is established by touching the outermost lead on that side and parallel to **D–E** or **F–G**.

Symbol	Description	Min	Max
A	Overall Height	4.19	4.57
A_1	Distance from Lead Shoulder to Seating Plane	2.29	3.05
D	Overall Package Dimension	17.4	17.7
D_1	Plastic Body Dimension	16.5	16.7
D_2	Foot Print	15.0	16.0
E	Overall Package Dimension	17.4	17.7
E_1	Plastic Body Dimension	16.5	16.7
E_2	Foot Print	15.0	16.0
CP	Seating Plans Coplanarity	0.00	0.10
TCP	Tweezing Coplanarity	0.00	0.10
LT	Lead Thickness	0.23	0.38

44-LEAD QUAD FLATPACK PACKAGE

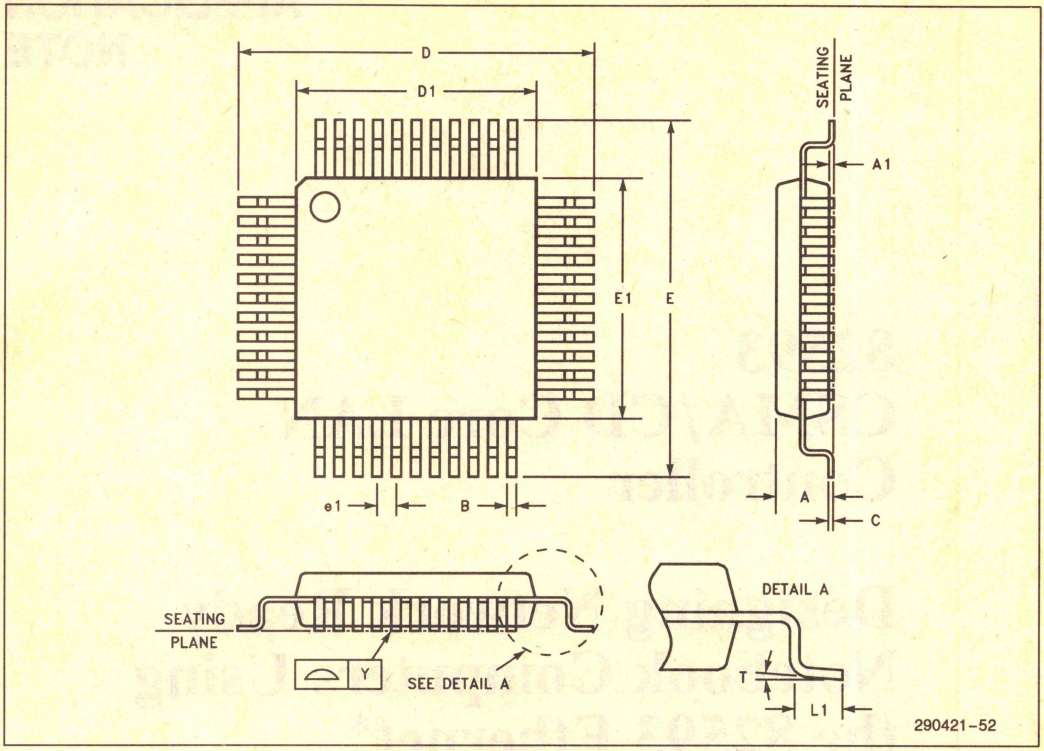


Figure 52. 44-Lead Quad Flatpack Package

Symbol	Description	Min	Nom	Max
A	Package Height			2.35
A1	Stand Off	0		0.60
B	Lead Width	0.2	0.3	0.4
C	Lead Thickness	0.1	0.15	0.2
D_1	Package Body		10	
E_1	Package Body		10	
e_1	Lead Pitch	0.65	0.8	0.95
D	Terminal Dimension	12.0	12.4	12.8
E	Terminal Dimension	12	12.4	12.8
L_1	Foot Length	0.38	0.58	0.78
Y	Coplanarity			0.1
T	Lead Angle	0		10°

NOTE:
Unless otherwise specified, all units are in millimeters.

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AP-367

APPLICATION NOTE

82593 CSMA/CD Core LAN Controller

Designing Network Ready Notebook Computers Using the 82593 Ethernet* Controller

RAYMOND SIT
TECHNICAL MARKETING ENGINEER

*Ethernet is a registered trademark of Xerox Corporation.

November 1992

Order Number: 292102-001

82593 CSMA/CD Core LAN Controller

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1

1.0 INTRODUCTION

This 82593 CMSA/CD Core LAN Controller Application Note provides applications and layout guidelines to build LAN solutions directly on the motherboard. The small form factor also allows easy integration into motherboard designs. LAN-On-Motherboard applications are becoming a market necessity for several reasons: Portable computing is on the rise, LAN Connectivity is fast becoming a real necessity and the installed base of LANs is growing daily. This Application Note is directed at all users interested in LAN-on-Motherboard (LOM) applications.

Portable Computing is on the Rise

Personal computers (PCs) have seen significant changes over the past several years. PCs have become firmly entrenched in the office. Their popularity, coupled with a highly competitive market, has compelled PC vendors to both reduce costs for their LAN solutions and to attempt to distinguish their product from the competition's. By the year 1995, 58% of all personal computer owners will own a portable computer. The requirement for LANs will grow accordingly.

LAN Connectivity is Beneficial

As Local Area Networks (LANs) have become more common in the office and in industry, some clear market development trends have emerged. Possibly the most significant of these is the concern for cost reduction, connectivity, and footprint reduction. These needs are driven by intense competition between network vendors for market share. Connectivity to Local Area Networks will become a both a necessity and a requirement by portable computer owners.

Ethernet Has the Largest LAN Installed Base

Of all the Local Area Networks on the market today, Ethernet has approximately 60% of the installed base. Designing the 82593 Ethernet LAN Controller onto the motherboard provides the portable computer user with access to the largest LAN market.

ExCA™ Implementation

Some portable manufacturers offer LAN connection through an ExCA LAN card. The ExCA socket allows the user the flexibility in choosing different types of network connections.

LOM provides a plug-and-play feature for ease of use at the lowest cost implementation.

This Application Note provides an overview of the 82593 LAN Controller. It also describes the 82593 power down mode, various power management techniques, and design examples for portable computers. Details of the 82593 timing requirements, choice of components, power control design and related issues are provided to aid the designer in the implementation of the 82593.

2.0 THE 82593 LAN CONTROLLER

The 82593 Ethernet controller is designed for space constrained applications. Together with the 82503 dual serial transceiver, a 10BASE-T LAN connection can occupy as little as 5 square inches (32 square mm).

The 82593 employs a non-buffered slave architecture that requires no external buffer memory. This reduces board space, material cost and power consumption. The 82503 integrates both 10BASE-T and AUI media interfaces into a single device. Its interface to the 82593 is tightly coupled, no external glue logic is required. The clock for the 82593 parallel interface can be taken from the 82503, thereby eliminating an external oscillator. This implementation can be as low as 5 ICs and is easy to design. A simplified example is shown in Figure 1.

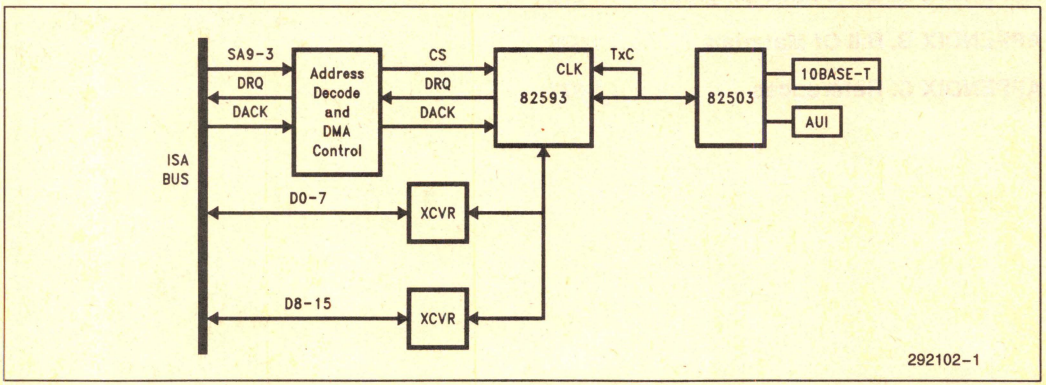


Figure 1. Non-Buffered Slave Design for Motherboard

3.0 82593 AND 82503 POWER MANAGEMENT FEATURES

3.1 Power Down Mode

Both the 82593 and the 82503 offer a power down feature. The 82503 can be powered down through an external pin. While in power down mode, it draws a maximum of 6 mW. The 82593 can be programmed to power down through a software command. In the power down mode, the maximum power dissipation is 38.5 mW.

3.2 Power Management Techniques

There are two ways of powering down the 82593 and the 82503. First by following a power down procedure to put the device in a power down mode. The advantage of this technique is that the 82593 maintains the configuration, while all other internal logic, including the internal clock circuitry, remains in static state. The parallel interface remains active and is ready to accept commands. On resume, the software is not required to re-configure and re-initialize the 82593. The following is a sample power down and power up sequence.

3.2.1 POWER DOWN SEQUENCE

1. Apply a minimum 300 ns pulse to the 82503 RESET pin. At the trailing edge of the pulse, assert the 82503 TEST and JABD pins as shown in Figure 2. Additional details are contained in the 82503 Data Sheet.
2. Switch the 82593 to port 1 access by issuing a SWITCH-TO-PORT-1 command.
3. Issue a POWER-DOWN command to place the 82593 into the Power Down mode. All internal circuits are in a static state, all input buffers are disabled, and all output buffers are tri-stated.

3.2.2 POWER RESUME SEQUENCE

1. Issue a NOP command to port 1 to restart the internal clock circuitry.
2. Issue a SEL-RST command to port 1. This causes the 82593 to exit the internal reset state.
3. De-assert the 82503 TEST and JABD pins. Wait a minimum of 1 ms (Timing parameter t183 in the 82503 Data Sheet) before the start of the transmission.

3.2.3 SEPARATE POWER SUPPLY

The second way to shut down the 82593 and 82503 is to turn off the power supply to the devices. This technique requires an external power FET or relay circuitry. The major advantage is that there is no power consumption for the entire LAN section. Where the portable PC is not connected to the network, the savings on standby power yields a substantial extension in battery life. The design example shown in the Section 4 illustrates design issues related to this implementation.

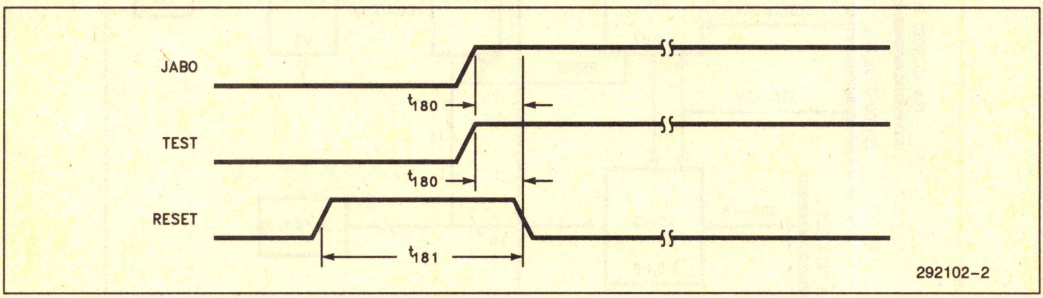


Figure 2. Power Down Mode Timing Diagram

4.0 DESIGN EXAMPLE FOR THE PORTABLES

The 82593 add-in board for the Intel SL Microprocessor Evaluation Board is designed to demonstrate 82593 features such as low component PCB space and low power dissipation. It is ideal for the portable motherboard application.

4.1 Architectural Overview

Figure 3 shows the block diagram of the 82593H3C board. Schematics of the 82593H3C board are contained in Appendix A. The PLD equations for the 82593H3C board are contained in Section 4.3 of this Application Note.

The 593H3C board is switchless. The configuration is preset to:

I/O Address: 300h to 30Fh
Interrupts: IRQ10
DMA: DMA6 and DMA7

The control logic provides all the handshaking between the host and the 82593. As shown in Figure 3, it is implemented by using PLDs U6 and U7 for low PCB space and additional power saving. This is discussed in detail in Section 4.2.1. The logic function can also be accomplished using a single PLD, a buffer, and an AND gate.

The IA PROM contains the 48-bit Ethernet address of the board. In some portables, this information can be stored in the NET_ID block within the boot flash memory, therefore eliminating the need of an external IA PROM. For additional details on the Net ID Block, contact your local Intel Field Applications Engineer.

The power switching logic enables and disables power to the Ethernet section in different power operating modes.

It is important to note that the 82593 together with the 82503 provide a complete 10BASE-T solution.

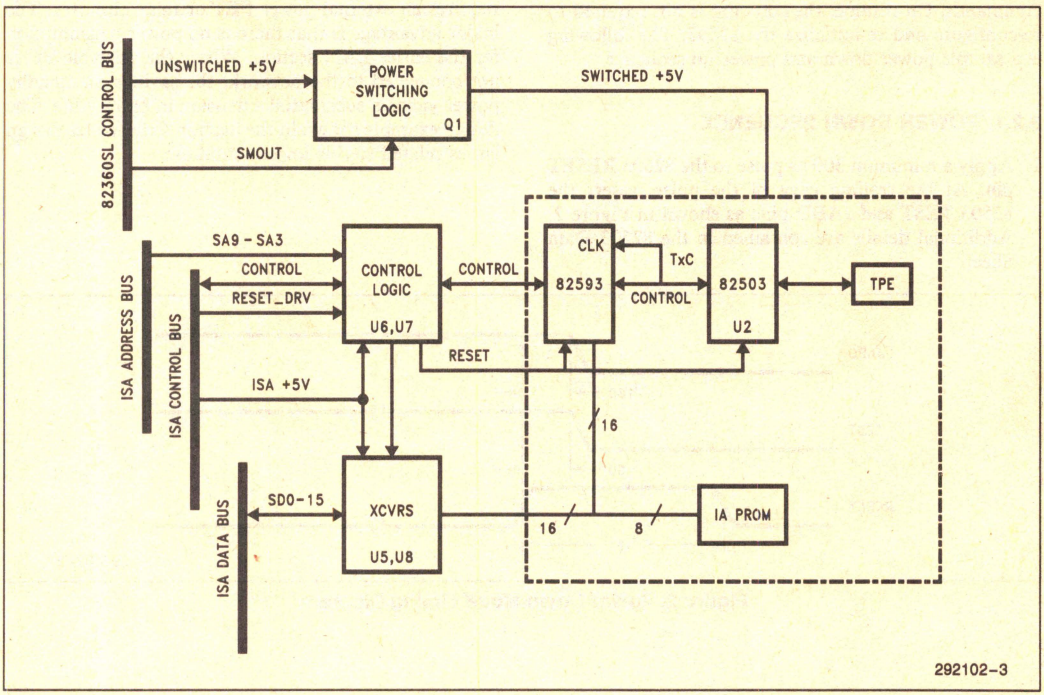


Figure 3. 82593 Portable Block Diagram

4.2 ISA Bus Interface

This section describes the address decoding logic and the timing requirements on an I/O access.

On power up, an active high RESET_DRV resets both the 82593 and the 82503. The minimum required pulse width for RESET_DRV signal is 300 ns. After resetting, the 82593 is configured by programming the port 0 command register at I/O address 300h. The address decoding is done internally within PLD U7. The equation is:

$$\overline{CS593} = !(!AEN * A9 * A8 * !A7 * !A6 * !A5 * !A4 * !A3)$$

Once the 82593 is configured, the application can assemble the transmit data in the host memory. Since each node on an Ethernet network is required to have a unique address, the program needs to read the Ethernet Individual Address from the IA PROM.

Reading the Ethernet Individual Address is done by an IOR command to the IA PROM at I/O address 308h through 30Fh. The maximum access time for the IA PROM is 100 ns. The equation is:

$$\overline{CS_IA} = !(!AEN * A9 * A8 * !A7 * !A6 * !A5 * !A4 * A3)$$

After the network software assembles the transmit data, it programs the DMA controller with the starting address of the block, the length of the block, other control information, and then issues a TRANSMIT command to the 82593. Upon receiving the TRANSMIT command, the 82593 fetches the first two bytes of the block to determine its length. If the link is free and at least one data byte is loaded into the 82593's Transmit FIFO, the 82593 begins transmitting the preamble and concurrently requests more bytes from the memory. The software driver for this board uses DRQ7 for receiving DMA transfers and DRQ6 for transmitting DMA transfers. The PLD equation is:

$$DRQ7 = DRQ5931 * !DRQ2 + DRQ5931 * DRQ7 * !(DRQ2 * (!\overline{IOR} + !\overline{IOW}))$$

The first term is for holding the DMA request if there is already an active DRQ2 request. DRQ2 is usually assigned to the floppy disk controller. The second term is for terminating the current DMA access whenever DRQ2 is active. This is to prevent the floppy disk drive from being overrun or underrun. Termination is synchronized with the leading edge of the $\overline{IOR}$ or $\overline{IOW}$ command. This is necessary to meet the DMA controllers timing requirements.

For reception, the 82593 compares the incoming frames' destination address with its programmed address. If it matches, the data is sent to the data area in the host memory via the DMA controller. The PLD equation is similar to the transmit equation and is:

$$DRQ6 = DRQ5930 * !DRQ2 + DRQ5930 * DRQ6 * !(DRQ2 * (!\overline{IOR} + !\overline{IOW}))$$

4.2.1 82593 I/O READ ACCESS

Figure 4 shows the worst case propagation delays within the ISA interface control logic along with a typical timing diagram. On an ISA I/O read cycle, the 82593 requires that the $\overline{CS593}$ activates before the $\overline{RD593}$. The delay calculation is as follows:

Maximum delay from SA bus valid to $\overline{CS593}$ is (The 20 ns is the additional delay when the PLD resumes from standby mode.)	20 ns + 10 ns
Minimum delay from SA bus valid to $\overline{IOR}$ is	28 ns
Minimum delay from $\overline{IOR}$ to $\overline{RD593}$ is	10 ns

Therefore, 30 ns on the $\overline{CS593}$ delay is always less than the $\overline{RD593}$ 38 ns delay.

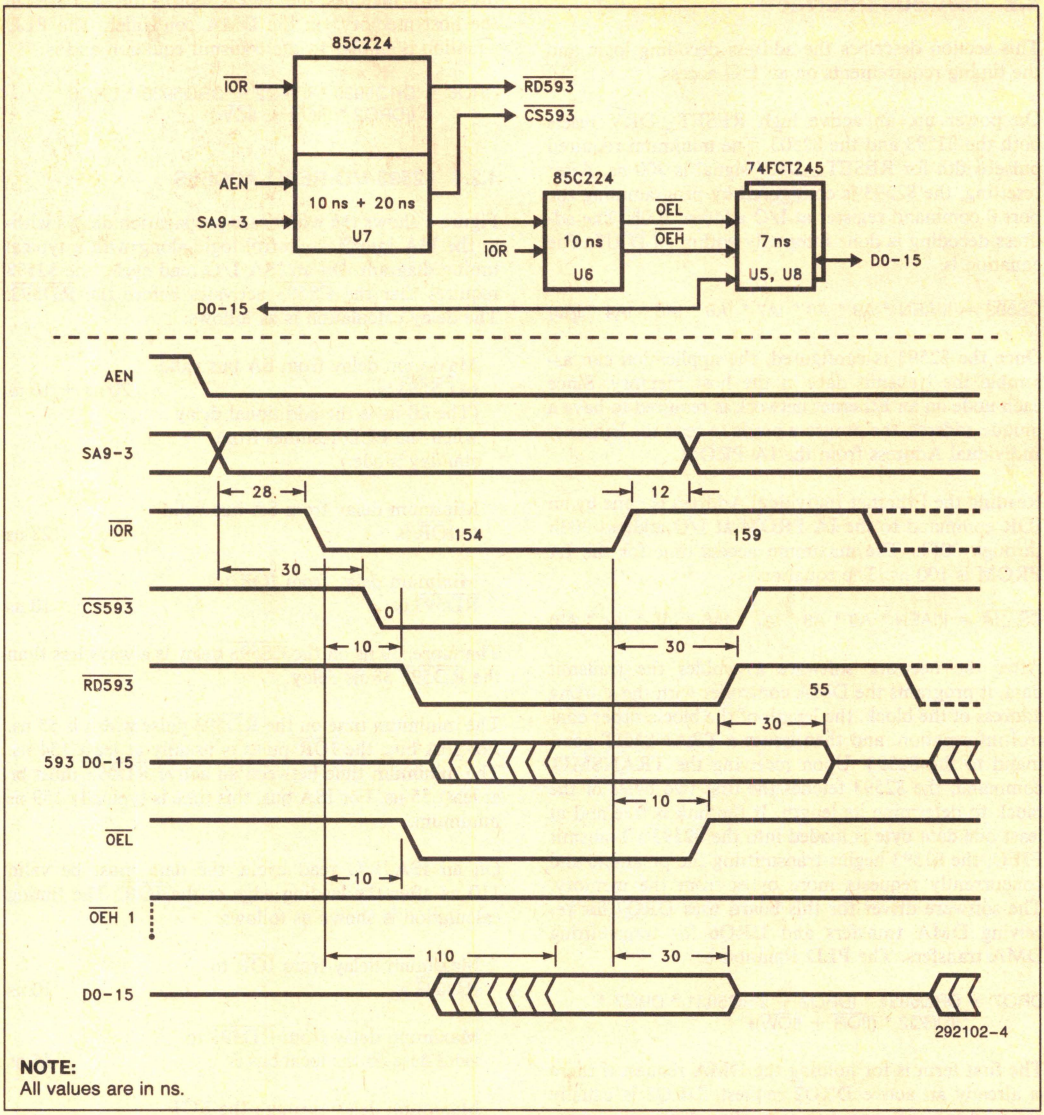
The minimum time on the $\overline{RD593}$ pulse width is 55 ns. For ISA bus, the $\overline{IOR}$ pulse is usually at least 154 ns. The minimum time between an active $\overline{RD593}$ must be at least 55 ns. For ISA bus, this time is typically 159 ns minimum.

On an ISA I/O read cycle, the data must be valid 110 ns after the leading edge of the $\overline{IOR}$. The timing calculation is shown as follows:

Maximum delay from $\overline{IOR}$ to $\overline{RD593}$ is	10 ns
Maximum delay from $\overline{RD593}$ to valid data on the local bus is	45 ns
Maximum delay through the FCT transceiver is	7 ns

Therefore, the total delay from $\overline{IOR}$ to valid data on the ISA bus is 62 ns.

The ISA bus timing requires the slave to tri-state the data bus within 30 ns after the trailing edge of the IOR command. As shown in Figure 4, the delay through U6 and the bus transceiver is 10 ns and 7 ns respectively, for a total of 17 ns.



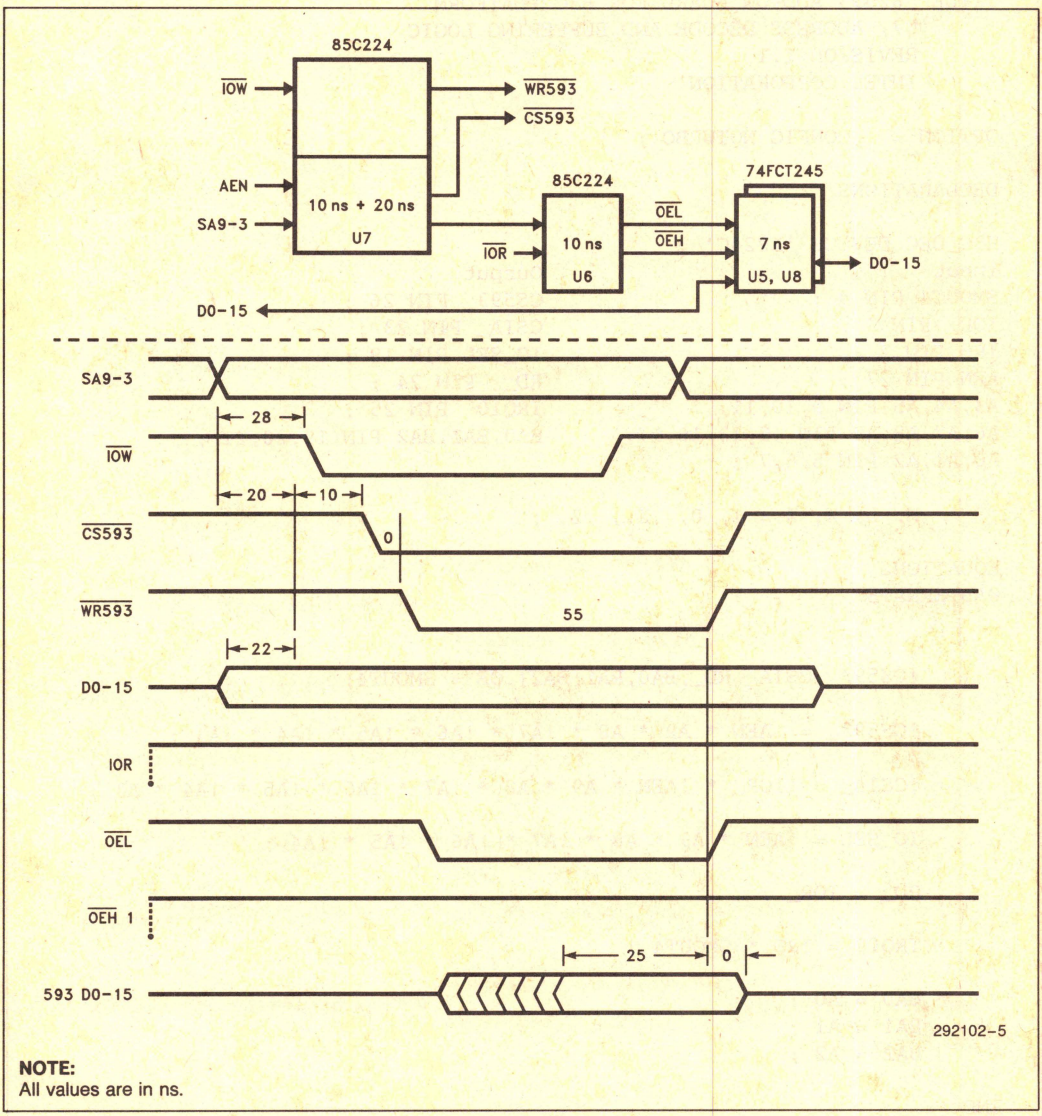
NOTE:
All values are in ns.

Figure 4. Worst Case Propagation Delays

4.2.2 82593 I/O WRITE ACCESS

Figure 5 shows that the 82593 requires a minimum of 25 ns data setup time for an I/O write cycle. Since the minimum $\overline{IOW}$ signal pulse width is at least 154 ns and the bus transceiver propagation delay is only 20 ns, the setup time is adequate.

The data hold time on 82593 I/O write is 0 ns. The ISA data hold time is 25 ns after the trailing edge of the $\overline{IOW}$. The delay on the $\overline{IOW}$ through U6 is only 10 ns, guaranteeing 15 ns hold time on valid data at the end of the $\overline{WR593}$ pulse.



NOTE:
All values are in ns.

Figure 5. 82593 I/O Write Access

4.3 PLD Equations

The following tables show the PLD equations for the H3C Modules.

4.3.1 MODULE H3C_DEC

```
TITLE '82593 ADD-ON BOARD FOR H3C PLATFORM
      U7, ADDRESS DECODE AND BUFFERING LOGIC
      REVISION 1.1
      INTEL CORPORATION'

OPTION = '-CONFIG NOTURBO';

DECLARATIONS

H3C_DEC DEVICE 'E224C' ;
Input                                 Output
SMOUT4 PIN 4 ;                        CS593_ PIN 26 ;
IOR_ PIN 3 ;                          CSIA_ PIN 23 ;
IRQ PIN 2 ;                           IO_SEL PIN 18 ;
AEN PIN 27 ;                          RD_  PIN 24 ;
A3,A4,A5 PIN 9,10,11;                 IRQ10  PIN 25 ;
A6,A7,A8,A9 PIN 12,13,16,17;          BA0,BA1,BA2 PIN 19,20,21 ;
A0,A1,A2 PIN 5,6,7 ;

      H, L, X, Z = 1, 0, .X., .Z. ;

EQUATIONS
@ALTERNATE


      [CS593_,CSIA_,RD_,BA0,BA1,BA2].OE = SMOUT4;

      !CS593_ = !AEN * A9 * A8 * !A7 * !A6 * !A5 * !A4 * !A3 ;

      !CSIA_ = !IOR_ * !AEN * A9 * A8 * !A7 * !A6 * !A5 * !A4 * A3 ;

      IO_SEL = !AEN * A9 * A8 * !A7 * !A6 * !A5 * !A4 ;

      RD_ = IOR_ ;

      IRQ10 = IRQ * SMOUT4 ;

      BA0 = A0 ;
      BA1 = A1 ;
      BA2 = A2 ;

END
```

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4.3.2 MODULE H3C—CNTL

```
TITLE '82593 ADDON BOARD FOR H3C PLATFORM
      U6, DATA BUS TRANSCEIVER AND DMA CONTROLS
      REVISION 1.1
      INTEL CORPORATION'

DECLARATIONS

H3C_CNTL DEVICE 'E224C' ;
Input                                  Output
   SMOUT4 PIN 10 ;                        DRQ6 PIN 19 ;
   IOR_ PIN 6 ;                           DRQ7 PIN 18 ;
   IOW_ PIN 5 ;                           OEH_ PIN 21 ;
   DRQ2 PIN 3 ;                           OEL_ PIN 23 ;
   DRQ5930 PIN 11 ;                       SMOUT4D1_ PIN 24 ;
   DRQ5931 PIN 27 ;                       DACK_ PIN 26 ;
   IO_SEL PIN 7 ;                         WR593_ PIN 20 ;
   RESET_DRV PIN 4 ;                      RESET PIN 25 ;
   PWRGOOD PIN 9 ;
   REFRESH_ PIN 2 ;
   DACK6_ PIN 16 ;
   DACK7_ PIN 17 ;
```

292102-7

4.3.2 MODULE H3C_CNTL (Continued)

```
EQUATIONS
@ALTERNATE

EQUATIONS
@ALTERNATE

Name                Product item                          Comment

[DACK_,WR593_].OE   = SMOUT4 ;                            Tri-state signal to 82583
                                                          during standby mode

[RESET].OE          = SMOUT4 * !RESET_DRV ;               Tri-state signal to 82583
                                                          during standby mode

[RESET].CLK         = REFRESH_ ;
[SMOUT4D1_].CLK     = REFRESH_ ;

SMOUT4D1_           = !SMOUT4 ;

RESET:              = SMOUT4D1_ ;

WR593_              = IOW_ ;

!OEL_               = (!IOR_ * IO_SEL                 +
                       !IOW_ * IO_SEL                 +
                       !IOR_ * !DACK6_                +  Transmit DMA read
                       !IOW_ * !DACK6_                +  Transmit DMA write
                       !IOR_ * !DACK7_                +  Recieve DMA read
                       !IOW_ * !DACK7_)               *  Recieve DMA write
                      SMOUT4 ;

!OEH_               = (!IOR_ * !DACK6_                +  Transmit DMA read
                       !IOW_ * !DACK6_                +  Transmit DMA write
                       !IOR_ * !DACK7_                +  Recieve DMA read
                       !IOW_ * !DACK7_)               *  Recieve DMA write
                      SMOUT4 ;

DRQ7                = (SMOUT4 * DRQ5931 * !DRQ2       +  See Section 4.2
                       SMOUT4 * DRQ7 * DRQ5931 *
                       !(!IOR_ * DRQ2 +
                         !IOW_ * DRQ2)) ;

DRQ6                = (SMOUT4 * DRQ5930 * !DRQ2       +  See Section 4.2
                       SMOUT4 * DRQ6 * DRQ5930 *
                       !(!IOR_ * DRQ2 +
                         !IOW_ * DRQ2)) ;

!DACK_              = !DACK6_                         +
                      !DACK7_;
```

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4.4 Logic Trade-Off

The host interface uses two PLDs. The PLD normally draws 40 mA when all inputs toggle at 25 MHz. When there is no activity at the inputs for 75 ns, the PLD automatically enters into a standby mode. In this mode, the PLD draws about 25 μA, thereby reducing power consumption.

The U7 PLD is used for address decoding. The input toggle rate is typically once in every 200 ns. Programming the PLD to Standby mode (See Reference 1) will reduce the power by 62.5 percent.

The U6 PLD cannot be programmed to the Standby mode due to the IOR Data Tri-state timing restrictions on the ISA bus. It takes 20 ns to resume from the Standby mode in addition to the normal PLD delay. The total delay from $\overline{IOR}$ inactive to data tri-stated is 37 ns, 7 ns over the specification. However, where the 82593 is in a closed environment such as portable computer and the host interface timing may be relaxed, then U6 should also be programmed to Standby mode to save power.

Selection of the bus transceiver is dependent on the application requirements. If the host interface timings can be relaxed, using the HCT or ACT series will generally give the lowest power dissipation. On the HCT Series, the quiescent current (I_{CC}) is at a maximum of 80 μA (see References 2 and 3) verses 52 mA for the LS series. In this design, FCT is used for meeting the ISA bus timings. The FCT series draws 1.6 mA additional quiescent current per input pin (delta I_{CC}) compared to 1 mA for the ACT series. The trade-off is the speed verses the power dissipation.

4.5 82503 Interface

The 82503 (U2) is strapped to select the 10BASE-T port with automatic polarity correction and link integrity enabled. CS0 and CS1 pins are tied low for interfacing with the Intel controller.

The 593H3C board supports the Ethernet 10BASE-T standard. It also supports A-Stepping and B- Stepping of the 82503. A-Stepping support is accomplished by connecting both TEST and JABD pins to the RESET signal. B-Stepping, or subsequent stepping, support is accomplished by strapping both pins to ground.

There are several LED indicators located at the top edge of the board. The LED's can be switched off by removing jumper J1. When lit, the LED's indicate the following status:

LED2 Indicates reverse polarity on the receive 10BASE-T pair.

LED3 Ethernet traffic collisions occur on the network.

LED4 Indicates active reception. Flash rate is proportional to the receive activity.

LED5 Indicates active transmission. Flash rate is proportional to the transmit activity.

LED6 Indicates good link integrity on the 10BASE-T port.

4.6 Power Supply Controls

The 82593H3C board uses three different power sources: an unswitchable +5V power, a switchable ISA +5V power and a switched on board +5V power. As shown in Figure 6, the board is divided into three different power planes representing the three power sources. The switchable ISA +5V is software controlled by the i386SL architecture. The switchable on board +5V power is controlled by the SMOUT4 signal on the 82360SL control bus connector.

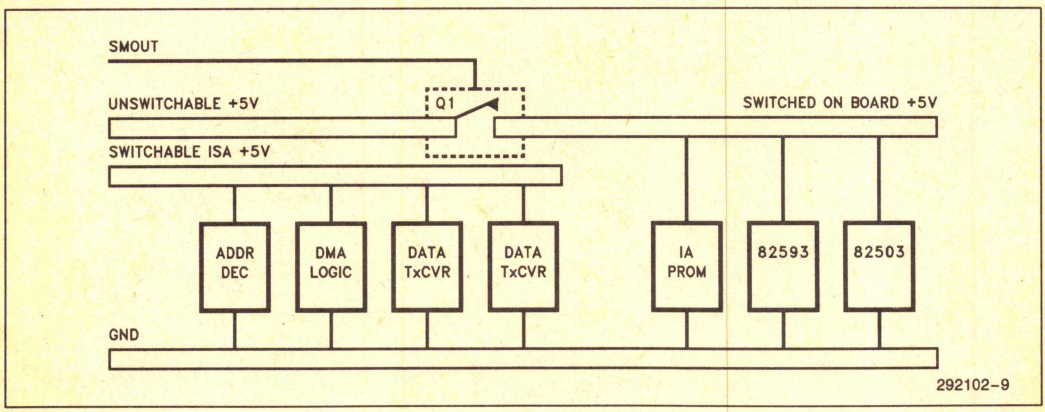


Figure 6. 82593H3C Power Planes Diagram

In active mode, the SMOUT4 signal is active high and the board is in the normal operating mode. When the system goes into local or global standby mode (see Reference 4), the SMOUT4 goes inactive (low). This turns the on-board switchable +5V to off, thereby cutting power to the 82593 and the 82503 logic. The host interface logic U6, U7 and the bus transceiver remains powered up. All signals interfacing with the 82593 are tristated, minimizing the current source to the 82593 input pins.

The switched +5V power supplies to the Ethernet section are taken from an unswitched +5V power source on the 82360SL control bus connector. This is because the ISA +5V power is the output of a MOSFET which is controlled by the i386SL. The potential drop across the MOSFET exists and the magnitude is dependent on the load. The On-state resistance of the MOSFET is about 0.25Ω at 1A, which translates to a 0.25V drop. Normally this is not a problem, but if the +5V power supply on the motherboard has a tolerance of 10% then the addition of the 0.25V drop might exceed the supply voltage specification for on board components.

In this design, the on board +5V switching is done by using a PhotoMOS Relay. The advantage of this over the MOSFET method is the simplicity and the small area required on the PCB. The input can be driven directly by a TTL output pin. The minimum current to turn on the relay is 5 mA. The rated on-state resistance is 0.25Ω maximum at 1A. Since this design draws a maximum of 0.6A, the maximum potential drop on the +5V power supply is less than 0.25V. This limits the power supply to a 5% tolerance. The relay has a maximum turn on time of 3 ms.

When the system goes into the suspend mode, the ISA +5V power to the board is switched off, shutting down the host interface logic. The 82593H3C board remains unoperational in this mode. On resume, the BIOS is required to reinitialize the device driver. Table 4-1 shows the AC characteristics of each pin in the different modes of operation.

Table 4-1. 82593H3C AC Characteristics

Inputs				Outputs			
To On-Board Logic	**Active Mode**	**Standby Mode**	**Suspend Mode**	**To 82593 and 82503**	**Active Mode**	**Standby Mode**	**Suspend Mode**
ISA__±5V	V_{CC}	V_{CC}	Float				
SMOUT4	High	Low	Tri-Stated	+5V	V_{CC}	Float	Float
AEN	Active	Active	Tri-Stated				
SA0–9	Active	Active	Tri-Stated	SA0–2	Active	Tri-Stated	Float
$\overline{IOW}$	Active	Active	Tri-Stated	$\overline{WR593}$	Active	Tri-Stated	Float
$\overline{IOR}$	Active	Active	Tri-Stated	$\overline{RD593}$	Active	Tri-Stated	Float
RESET_DRV	Active	Active	Tri-Stated	RESET	Active	Tri-Stated	Float
D0–15	Active	Active	Tri-Stated	D0–15	Active	Tri-Stated	Float
				$\overline{CS_593}$	Active	Tri-Stated	Float
				$\overline{CS_IA}$	Active	Tri-Stated	Float
				$\overline{DIR}$	Active	Active	Float
				$\overline{OEL}$	Active	High	Float
				$\overline{OEH}$	Active	High	Float
$\overline{DACK6}$	Active	High	Tri-Stated				
$\overline{DACK7}$	Active	High	Tri-Stated	$\overline{DACK}$	Active	Tri-Stated	Float

Inputs				Outputs			
To On-Board Logic	**Active Mode**	**Standby Mode**	**Suspend Mode**	**To ISA Bus**	**Active Mode**	**Standby Mode**	**Suspend Mode**
DRQ2	Active	Active	Tri-Stated				
DRQ5930	Active	PD (10K)	Float	DRQ6	Active	Low	Float
DRQ5931	Active	PD (10K)	Float	DRQ7	Active	Low	Float
IRQ	Active	PD (10K)	Float	IRQ10	Active	Low	Float

LEGEND: PD = Pull Down

DRQ6, DRQ7 and IRQ10 signals are ignored during the suspend mode.

On resume, after the power is restored to the board, a reset pulse (minimum 300 ns) is required to activate the 82503 and the 82593. Depending on from which mode the board is resumed, the RESET_DRV signal might not be active. Table 4-2 provides a brief description on different reset signals that occur upon resume:

Table 4-2. i386SL Reset Signal Characteristics

Connector Signal	Resume from Standby Mode	Resume from 5V Suspend Mode	Resume from 0V Suspend Mode
PWRGOOD	High	High	100 ms Pulse
CPU_RESET	Low	92 μs Pulse	92 μs Pulse
RESET_DRV	Low	120 ms Pulse	120 ms Pulse

On a cold boot, the voltage levels on the motherboard must be maintained for a minimum of 100 ms before the power good signal goes active as shown in Figure 7.

Figure 8 shows an implementation of the reset pulse generator. It requires a pull up resistor on the RESET signal that is connecting to the 82593 and the 82503. On a normal reset, the RESET_DRV is active, tri-stating the output buffer. The pull up resistor is used to provide an active high reset level to the devices. When RESET_DRV is inactive, it enables the internal state of the SMOUT4 signal, which is low to terminate the RESET pulse.

The logging of the SMOUT4 status is accomplished by the $\overline{\text{REFRESH}}$ signal. This is the only signal on the ISA connector that can provide a real-time time stamp. The time between two $\overline{\text{REFRESH}}$ pulses is always about 15 μs which is sufficient to reset both the 82503 and the 82593. At a Maximum of 30 μs after the board enters into the standby mode, the internal standby mode status is logged. Upon resume, the buffer output enable immediately turns on and the internal standby status is maintained for a minimum of 15 μs, which is enough time to reset both devices.

4.7 Layout Guidelines

All traces should be as short as possible for the following:

Between the 82593 and the 82503

Between the 82503 and CRA1

Between CRA1 and U3

Between U3 and RJ1.

The TD+ and TD− traces connecting to RJ1 should be routed as close as possible. Similarly for the RD+ and RD− signal pair. Separation between the TD pair and the RD pair should be at least 0.2 inches.

Y1 crystal connections to U2 should be as short as possible.

All V_{CC} traces from the surface mounted devices should be routed to the decoupling capacitors before connecting to the power plane. Refer to the 82503 Application Note for additional information.

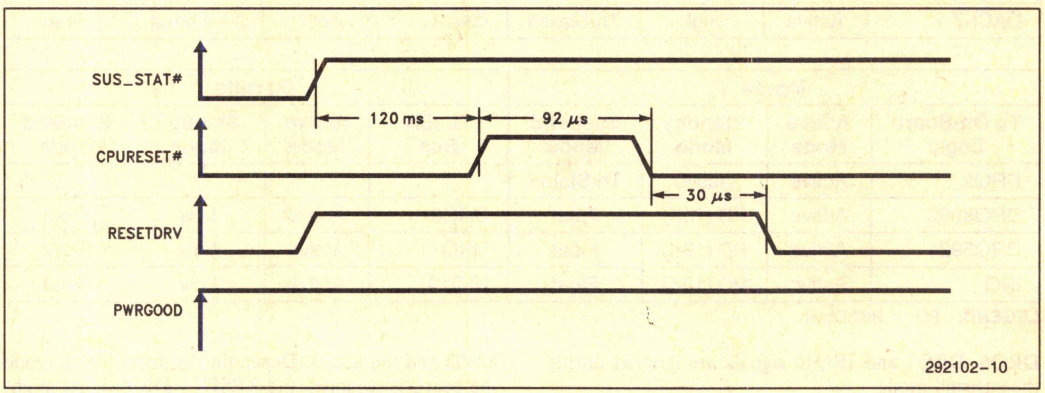


Figure 7. Standby Resume Reset Waveform

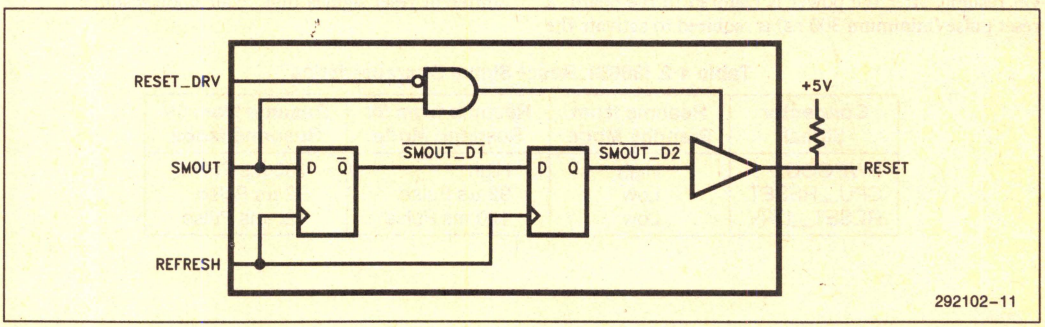


Figure 8. Standby Resume Reset Pulse Generation Logic

4.8 Design Alternatives

4.8.1 INDIVIDUAL ADDRESS PROM

In portables, the Individual Address can be stored in a non-volatile area such as in the BIOS space. This technique works especially well in systems that use Flash EPROM for the BIOS. The driver reads the appropriate location in the BIOS space called NETID block to determine the hardware configuration. Full details on the NETID format and an implementation example are outlined in Intel's LAN 593 Hardware/Software Interface Definition.

4.8.2 REMOTE BOOT EPROM

The remote boot feature allows the system administrator ease of distribution and upgrade of the device driver. The boot code contains the minimum operations to access the server. Once connected to the server, the client can download the entire operating system and specific program interface.

The boot code can reside within the ROM space in the BIOS. The mapping location can be specified in the NETID block. If a separate ROM device is preferred, then additional decode logic may be required.

APPENDIX A
SCHEMATICS

The 82593H3C schematics are included in this appendix in their entirety.

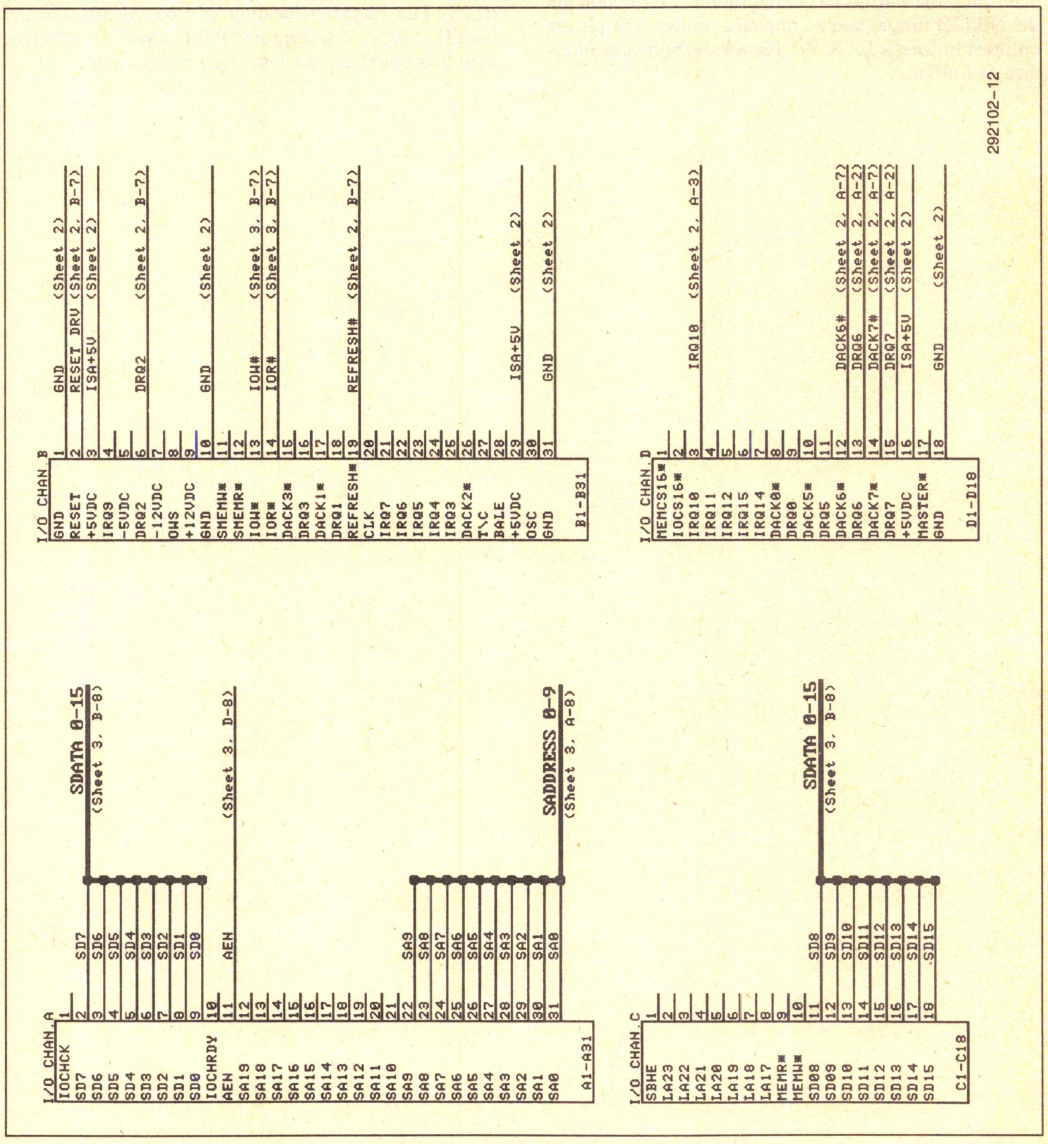


Figure A-1. 82593-HC3 LAN Module (Sheet 1 of 4)

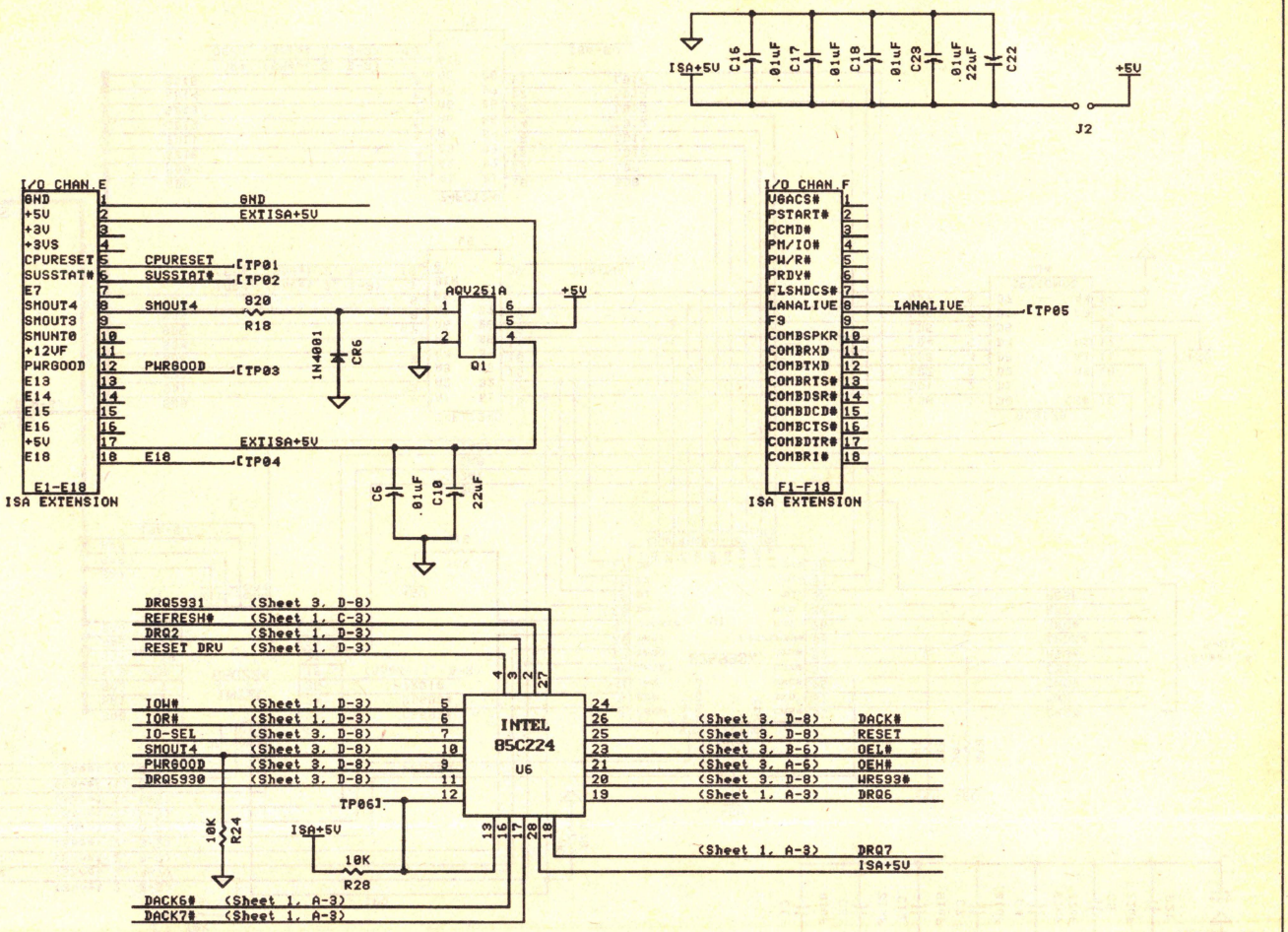


Figure A-2. 82593-HC3 LAN Module (Sheet 2 of 4)

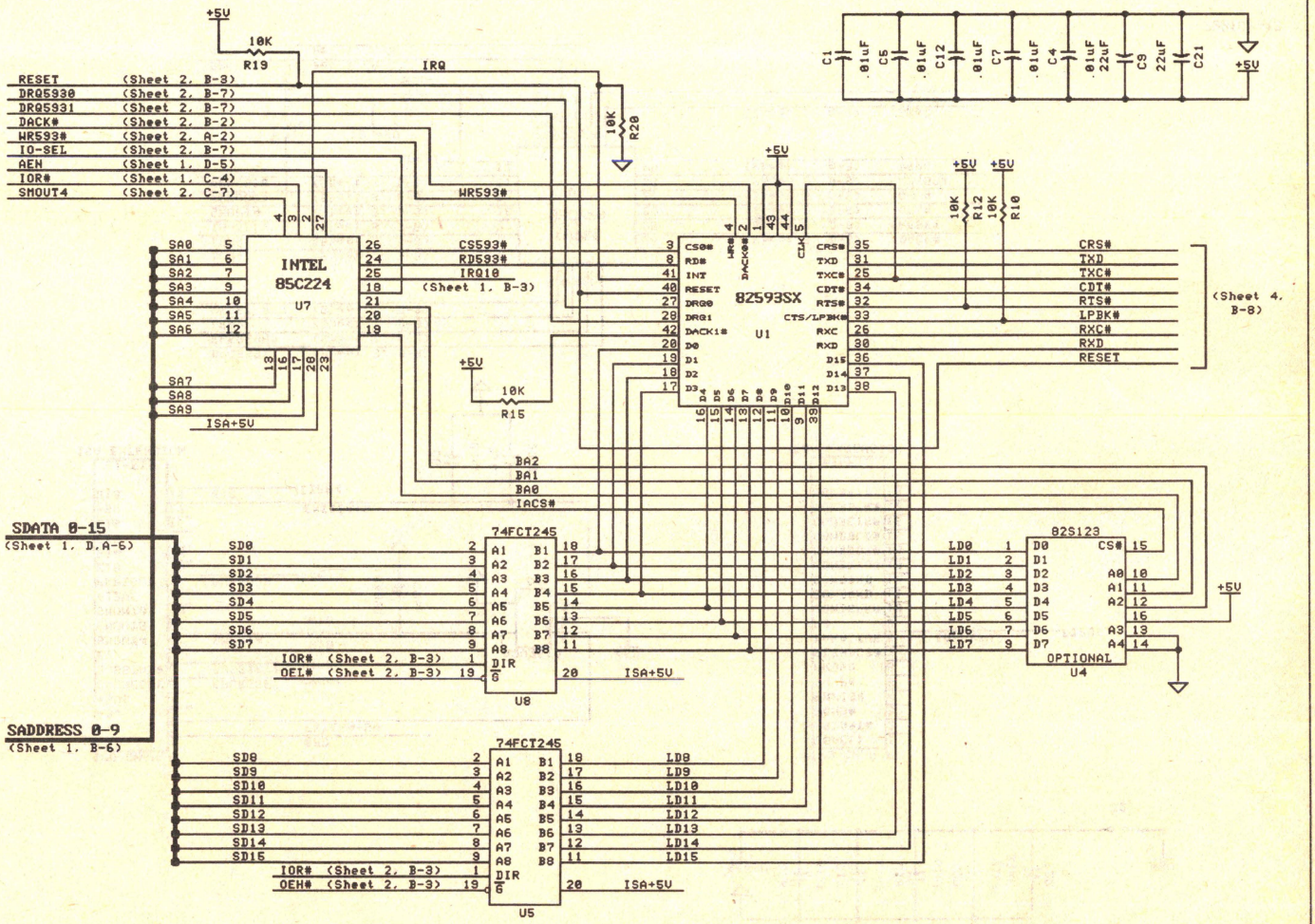


Figure A-3. 82593-HC3 LAN Module (Sheet 3 of 4)

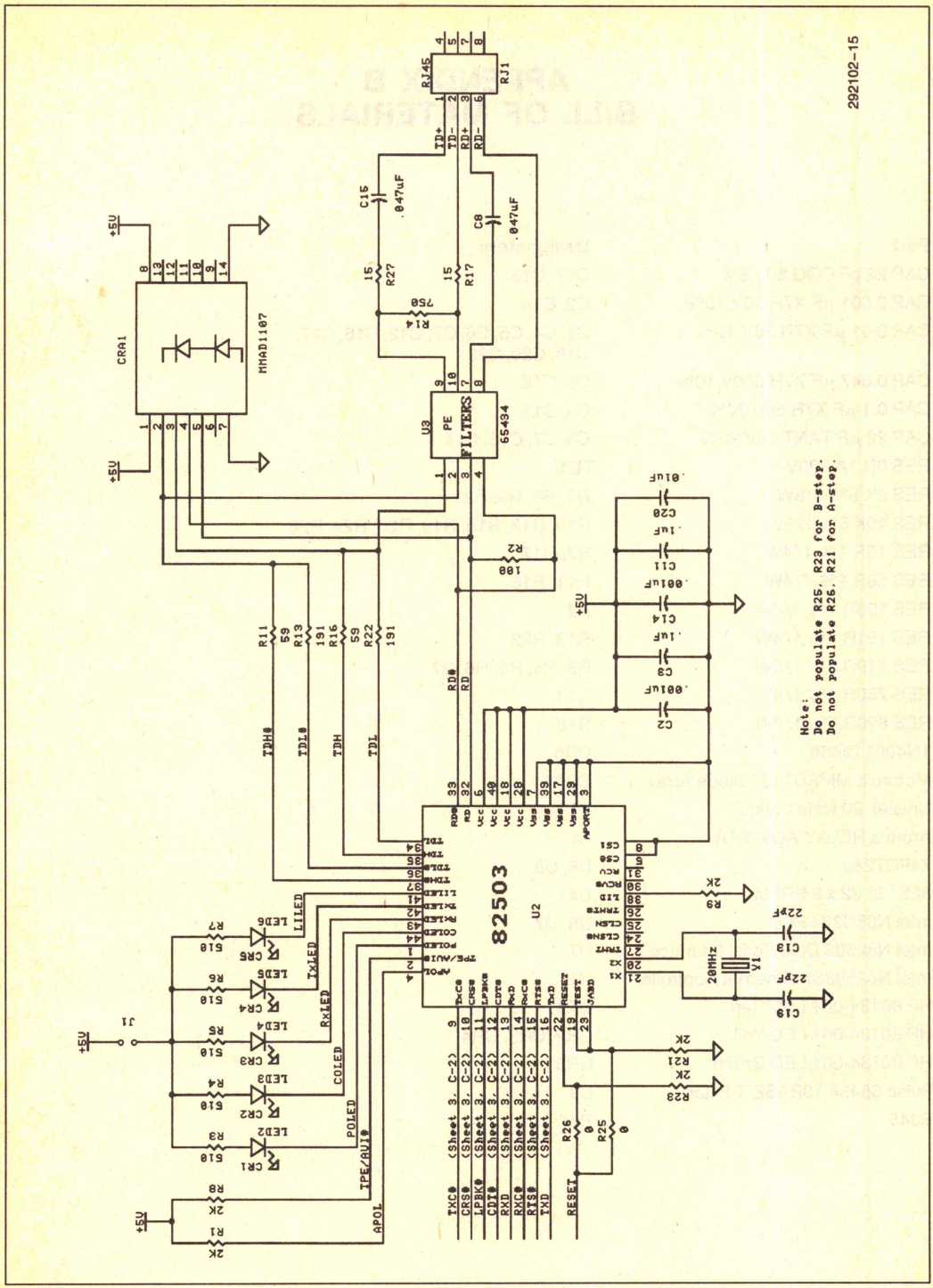


Figure A-4. 82593-HC3 LAN Module (Sheet 4 of 4)

APPENDIX B
BILL OF MATERIALS

Part	Designators
CAP 22 pF COG 50V 5%	C17, C18
CAP 0.001 μF X7R 50V 10%	C2, C14
CAP 0.01 μF X7R 50V 10%	C1, C4, C5, C6, C7, C12, C16, C17, C18, C20, C23
CAP 0.047 μF X7R 600V 10%	C8, C15
CAP 0.1 μF X7R 50V 20%	C3, C11
CAP 22 μF TANT 16V 20%	C5, C7, C13, C14
RES 0R 1A 200V	R25
RES 2K 5% 1/8W	R1, R8, R9, R21
RES 10K 5% 1/8W	R10, R12, R15, R19, R20, R24, R28
RES 15R 1% 1/4W	R7, R17
RES 59R 1% 1/4W	R11, R16
RES 100R 1% 1/4W	R2
RES 191R 1% 1/4W	R13, R22
RES 510R 5% 1/8W	R3, R4, R5, R6, R7
RES 750R 1% 1/4W	R14
RES 820R 5% 1/8W	R18
1N4001 Diode	CR6
Motorola MMAD1107 Diode Array	CRA1
Crystek 20 MHz Crystal	Y1
Aromat RELAY AQV251A	QI
74FCT245	U5, U8
82S123 32 x 8 PR0M	U4
Intel N85C224 PLD	U6, U7
Intel N82503 Dual Serial Interface	U7
Intel N82593SX Ethernet Controller	U1
HP 60134-001 LED Red	CR1
HP 60134-001 LED Yellow	CR2, CR3, CR4
HP 60134-001 LED Green	CR5
Pulse 65434 10BASE-T Filter	U3
RJ45	RJ1

APPENDIX C
REFERENCES

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EtherExpress™ FlashC LAN Adapters

The Product

Intel's most technically advanced 16-bit EtherExpress adapters.

Product Features

Ease of Installation

- One-step automatic configuration and installation of drivers to hard disk
- Auto-configures for the right connector, I/O addresses and IRQs

Update New Drivers with Ease

- The FlashUpdate utility automatically updates drivers for every EtherExpress card on the network from the administrator's disk
- Quick and easy flash memory lets you download future applications firmware into your EtherExpress FlashC

Easy Management of Your PC Assets

- The FlashView utility automatically scans hardware and software information and stores it in flash memory
- Integration with Intel's LANDesk™ Manager

Technical Summary

- 256K on-board Intel FLASH non-volatile memory
  - — Includes all new FLASHworks utilities
  - — Flash contents can be updated from one central console
  - — Supports unshielded twisted pair (10Base-T), thin and thick-wire coax Ethernet
  - — Complete board-level and on-network diagnostics
- LAN Sight Express remote node management software for Novell networks (to monitor nodes, diagnose performance bottlenecks, verify server usage and compile network traffic statistics) available free via Intel BBS
  - — SNMP (Simple Network Management Protocol) services option available for SNMP managed networks
  - — UL, FCC, VDE-approved

*Other brands and names are the property of their respective owners.

EtherExpress™ 16 LAN Adapters

The Product

A family of adapters consisting of EtherExpress 16, and EtherExpress 16TP and, the newest development, EtherExpress 16C which combines the functionality of the 16 and 16TP. The EtherExpress 16C provides 8-bit and 16-bit support for twisted-pair (10Base-T) thin and thick-wire Ethernet* cabling at a very competitive price.

Product Features

EtherExpress 16C LAN Adapters

- Price performance leader for Ethernet LAN adapter
- Thick-wire, Thin-wire and 10Base-T ports for three-way media support
- 16-bit custom silicon design and increased chip integration for higher reliability
- Automatic software configuration with intelligent Softset utility
- Compatible with EtherExpress 16 driver suite
- Full support for standard network operating system
- Auto-sensing IPX capability

Technical Summary

EtherExpress 16 LAN Family

- Best price/performance Ethernet adapter cards
- Completely software configurable, no jumpers or switches
- Free LANSight Express remote node management software
- Includes extensive driver suite compatible with major NOS (Network Operating System)
- SNMP compatible

EtherExpress™ 32 LAN Adapters

The Product

An intelligent EISA bus master Ethernet adapter which supports connections to both thick and thin Ethernet cabling with standard DIX/AUI 15-pin and BNC connectors.

Product Features

High Performance

- Specifically designed for EISA workstations and servers

High Speed Data Transfer

- Intelligent 32-bit bus master interface provides high-speed direct read/write between adapter and system memory

Ease of Configuration

- Simple and switchless software configuration according to EISA standard

Complete Board Level Diagnostics

- Comprehensive software verifies operations and identifies problems quickly before they get out of control

Technical Summary

- EISA (Extended Industry Standard Architecture) data bus for maximum throughput
- Intelligent 32-bit bus master interface for high-performance in EISA computers
- Editors Choice Award—1992 PC Magazine
- Optimum for multi-segment networks
- Comprehensive server and client drivers included
- Coax version available
- Total compliance with IEEE 802.3 Ethernet standard
- Full Support for Novell and Microsoft* NOS
- Supports the EISA 33 Mb/second burst mode for data transfers at maximum speed
- On board Intel 20 MHz 80186 co-processor to off-load host CPU
- Switchless software configuration with EISA configuration utility
- Direct connections to both thick- and thin-Ethernet cabling
- Comprehensive board-level diagnostics software
- Three year warranty and free technical support

EtherExpress™ MCA LAN Adapters

The Product

A 16-bit, half-size Ethernet adapter available in two options. The EtherExpress 16 MCA supports direct connections to thin or thick Ethernet wiring, while the 16 MCA TP supports direct connectors to thick Ethernet or 10Base-T unshielded twisted pair wiring.

Product Features

Easy Installation

- No need to set jumpers or switches
- Self-configuring, auto-sensing

Maximum Performance

- Highly integrated custom silicon
- 64K of on-board DRAM

Technical Summary

- Completely software configurable with new auto-sensing connector capability
- Switchless software configuration with IBM's standard PS/2* setup program
- 16-bit interface using custom silicon design and 64K of buffer memory
- Flash memory on-board for diskless workstations and remote boot
- Compatible with EtherExpress 16 driver suite
- Coax and 10Base-T versions available
- Free LANSight Express remote node management software
- Full support for all standard NOS
- Supports SNMP
- Comprehensive board-level diagnostics tests both adapter integrity and network connection
- Four LED status indicators for easy diagnostics (10Base-T only)
- Complete with 256K of Intel flash memory that provides remote boot code of Novell NetWare* and Microsoft* LAN Manager* networks
- Total compliance with IEEE 802.3 Ethernet standard
- Three year warranty and free technical support

TokenExpress™ LAN Adapters

The Product

A complete range of TokenExpress LAN adapters, all fully verified for complete SNA compatibility and interoperability.

Product Features

TokenExpress ISA 16s LAN Adapter

- 16-bit design operates in AT compatible and 8-bit PCs

Token Express ISA/8 LAN Adapter

- Economical 8-bit design

TokenExpress EISA 16/4 LAN Adapter

- Bus mastering DMA Token Ring adapter for EISA compatible computers

TokenExpress MCA 16/4 LAN Adapter

- Micro Channel bus master burst mode data transfer

TokenExpress EISA/32 LAN Adapter

- The performance leader in Token Ring adapters for EISA PCs and Servers

Technical Summary

- Interoperable with all IBM* computing environments
- Excellent price/performance leadership position
- 16-bit and 32-bit cards completely software configurable, no jumpers or switches
- Extensive high performance driver suite for servers and clients on major NOS
- Comprehensive diagnostics program
- Full 128K of on-board memory
- LANDesk™ and DMI ready
- Supports shielded twisted-pair (STP) and unshielded twisted-pair (UTP) media at 4 Mbps and 16 Mbps
- Meets IEEE 802.2 and IEEE 802.5 standards
- Intel LANSight Express remote node management software available at no charge via BBS
- SNMP Management available via Intel's SNMP Service software
- Three year warranty and free technical support

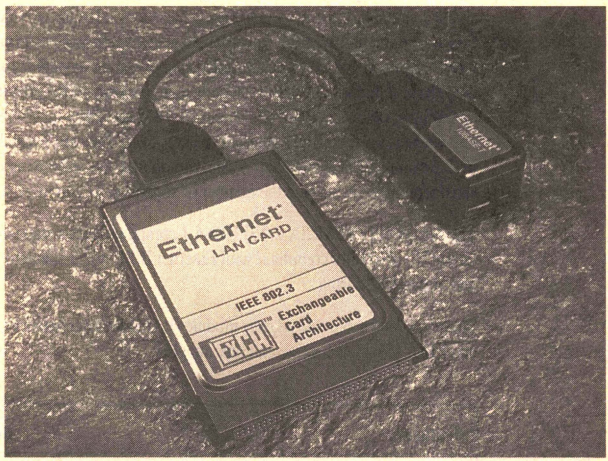
PCMCIA Cards

3

Ethernet* LAN Card Product Brief

Product Highlights

- Complete plug and play PCMCIA LAN solution. Comes with all drivers, installation, card and socket services and card management software necessary for reliable operation in a PCMCIA slot.
- Drivers for all major network operating systems.
- Industry-recognized Intel SoftSet installation software. Easy to operate and manage.
- Based on highly integrated Intel 82595 Ethernet Controller
- Complies with PCMCIA 2.0/ JEIDA 4.1 68-pin standard.
- 5 mm-thick PCMCIA Type II card.
- Detachable line adapter module (LAM) for multiple media attachment.
- Ethernet IEEE 802.3 compatibility (10BASE-T/TPE, 10BASE- 2/BNC).
- Activity and link integrity LEDs.



The Intel PCMCIA Ethernet LAN Card brings high performance and ease of use to PCMCIA networking. It lets you put networking capabilities into laptop computers without a lot of hassle, headache or expense.

It's a plug and play solution, providing PCMCIA network- readiness right out of the box. All the software you need comes with the card: drivers for the most popular network operating systems (Novell NetWare 2.2, 3.11, 4.0 and Lite 1.0; Microsoft* LAN Manager* 2.X; IBM* LAN Server* 2.X; Banyan Vines* 4.x; and Microsoft Windows for Workgroup* 3.1), PCMCIA- compliant card and socket services from SystemSoft*, and Intel's own card manager and Softset auto-configuration, auto-installation software that gets users on the network fast.*

The Intel PCMCIA Ethernet LAN Card is based on the highly integrated Intel 82595 ISA/PCMCIA Ethernet Controller, giving you 16-bit desktop performance in a PCMCIA form factor. As we develop additional software functionality for our 82595 line, you'll be able to leverage it across your entire 82595-based product line, from chips to NICs to PCMCIA form factor products. You decrease your time to market by taking advantage of Intel's product development efforts, while increasing the value of your products.

The card is standard PCMCIA 2.0 68-pin form factor and only 5 mm thick. It's passed Intel's extensive quality and reliability testing to ensure that it stands up to the rigors of mobile users on the go. These include PCMCIA mechanical qualification testing such as torque, bend, shock, vibration and environmental testing across extreme temperatures and voltages. Our CMOS technology and highly integrated 82595 are very power efficient, letting mobile users stay connected to the network for a long time. Maximum power draw is 85 mA; in idle mode, power consumption drops to 20 mA.

Finally, we've made it easy to customize our card and its accessories to your own OEM marketing needs. Manuals, software diskettes and the cards themselves can all be tailored to reflect your company's look.

Product Description

The Intel PCMCIA Ethernet LAN Card is the fastest, easiest way to deliver network-ready laptops to your customers. It snaps in and installs in minutes, not hours, thanks to a disk-full of software to make your job easier. Our industry-standard SoftSet installation utility automatically configures the card and sets up the software with a single command. Built-in card and socket services software provides card recognition and compatibility. Built-in card management software performs IRQ management and allows the card to be installed even when the system is running, so you don't have to reboot. There's even built-in driver support for popular network operating systems from Novell, Microsoft, IBM and Banyan. There are no jumpers or switches to set, no IRQ addresses to labor over. The card's installed and working in five minutes. Once installed, it's easy to operate too, improving customer satisfaction and decreasing the number of support calls you receive.

The card is fully PCMCIA 2.0/JEIDA 4.1 compliant with a standard 68-pin form factor. It's also fully compliant with Ethernet IEEE 802.3 standard for 10BASE-T and 10BASE-2 wiring.

There's a detachable line adapter module (LAM) for attachment to multiple media and LEDs to indicate active and link integrity.

Features	Benefits
— Installation, card manager, and card and socket services software	— A complete solution; no need for any other pieces Easy to install, easy to configure, easy to use
— Broad client driver support	— Meets broad target market. Usable on industry-standard networks like Novell, LAN Manager and Banyan
— Complies with PCMCIA 2.0/JEIDA 4.1 standards	— No jumpers Easy to transport Small form factor
— Intel-based 82595	— Great performance; 8 & 16-bit data path Glueless interface to PCMCIA Bus
— Activity and link integrity LEDs	— Indicates card status, improves diagnostics
— Supports both twisted pair Ethernet (10BASE-T) and ThinCoax (BNC 10BASE-2)	— Flexibility to connect to multiple network media

Product Codes

MBLA8110	TPE all geographies
MBLA8120US	BNC US
MBLA8120EU	BNC Europe

Additional Literature

Local Area Networking Family Product Brief	297085-002
EtherExpress Family Brochure	D413.01
TokenExpress Family Brochure	D414.02
Intel 82595 Data Sheet	290458-003
Intel 82595 User's Manual	TBD

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NORTH AMERICAN SALES OFFICES

ALABAMA

Intel Corp.
600 Boulevard South
Suite 104-I
Huntsville 35802
Tel: (800) 628-8686
FAX: (205) 883-3511

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Tel: (800) 628-8686
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Sacramento 95821
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San Diego 92123
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FAX: (619) 467-2460

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FAX: (408) 441-9540

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Intel Corp.
2250 Lucien Way
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Maitland 32751
Tel: (800) 628-8686
FAX: (407) 660-1283

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†Intel Corp.
20 Technology Parkway
Suite 150
Norcross 30092
Tel: (800) 628-8686
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FAX: (208) 377-1052

ILLINOIS

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Westford 01886
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MICHIGAN

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West Bloomfield 48322
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Bloomington 55431
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Intel Corp.
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Parsippany 07054-1315
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FAX: (201) 402-4893

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Lincroft Office Center
125 Half Mile Road
Red Bank 07701
Tel: (800) 628-8686
FAX: (908) 747-0983

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Suite 130
Islandia 11722
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Intel Corp.
6801 N. Broadway
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FAX: (405) 840-9819

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Building B
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20515 SH 249
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†Intel Corp.
428 East 6400 South
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Suite 401
Brookfield 53005
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Intel Semiconductor of
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999 Canada Place
Suite 404, #11
Vancouver V6C 3E2
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FAX: (604) 844-2813

ONTARIO

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Canada, Ltd.
2650 Queensview Drive
Suite 250
Ottawa K2B 8H6
Tel: (800) 628-8686
FAX: (613) 820-5936

†Intel Semiconductor of
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190 Attwell Drive
Suite 500
Rexdale M9W 6H8
Tel: (800) 628-8686
FAX: (416) 675-2438

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†Intel Semiconductor of
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Pt. Claire H9R 5N3
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FAX: 514-694-0064

†Sales and Service Office
*Field Application Location

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Hamilton Hallmark
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Irvine 92718-2809
Tel: (714) 768-4444
FAX: (714) 768-6456

Anthem Electronics
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Tel: (916) 624-9744
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Anthem Electronics
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FAX: (619) 546-7893

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San Jose 95131
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FAX: (408) 441-4504

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San Diego 92123
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21150 Califa St.
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Hamilton Hallmark
580 Menlo Drive, #2
Rocklin 95762
Tel: (916) 624-9781
FAX: (916) 961-0922

Pioneer Standard
5850 Canoga Blvd., #400
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Tel: (818) 883-4640

Pioneer Standard
217 Technology Dr., #110
Irvine 92718
Tel: (714) 753-5090

Pioneer Technologies Group
134 Rio Robles
San Jose 95134
Tel: (408) 954-9100
FAX: (408) 954-9113

Wyle Laboratories
15370 Barranca Pkwy.
Irvine 92713
Tel: (714) 753-9953
FAX: (714) 753-9877

Wyle Laboratories
15360 Barranca Pkwy., #200
Irvine 92713
Tel: (714) 753-9953
FAX: (714) 753-9877

Wyle Laboratories
2951 Sunrise Blvd., #175
Rancho Cordova 95742
Tel: (916) 638-5282
FAX: (916) 638-1491

Wyle Laboratories
9525 Chesapeake Drive
San Diego 92123
Tel: (619) 565-9171
FAX: (619) 365-0512

Wyle Laboratories
3000 Bowers Avenue
Santa Clara 95051
Tel: (408) 727-2500
FAX: (408) 727-5896

Wyle Laboratories
17872 Cowan Avenue
Irvine 92714
Tel: (714) 863-9953
FAX: (714) 263-0473

Wyle Laboratories
26010 Mureau Road, #150
Calabasas 91302
Tel: (818) 880-9000
FAX: (818) 880-5510

Zeus Arrow Electronics
6276 San Ignacio Ave., #E
San Jose 95119
Tel: (408) 629-4789
FAX: (408) 629-4792

Zeus Arrow Electronics
22700 Savi Ranch Pkwy.
Yorba Linda 92687-4613
Tel: (714) 921-9000
FAX: (714) 921-2715

COLORADO

Anthem Electronics
373 Inverness Drive South
Englewood 80112
Tel: (303) 790-4500
FAX: (303) 790-4532

Arrow/Schweber Electronics
61 Inverness Dr. East, #105
Englewood 80112
Tel: (303) 799-0258
FAX: (303) 373-5760

Hamilton Hallmark
12503 E. Euclid Drive, #20
Englewood 80111
Tel: (303) 790-1662
FAX: (303) 790-4991

Hamilton Hallmark
710 Wooten Road, #102
Colorado Springs 80915
Tel: (719) 637-0055
FAX: (719) 637-0088

Wyle Laboratories
451 E. 124th Avenue
Thornton 80241
Tel: (303) 457-9953
FAX: (303) 457-4831

CONNECTICUT

Anthem Electronics
61 Mattatuck Heights Road
Waterburg 06705
Tel: (203) 575-1575
FAX: (203) 596-3232

Arrow/Schweber Electronics
12 Beaumont Road
Wallingford 06492
Tel: (203) 265-7741
FAX: (203) 265-7988

Avnet Computer
55 Federal Road, #103
Danbury 06810
Tel: (203) 797-2880
FAX: (203) 791-9050

Hamilton Hallmark
125 Commerce Court, Unit 6
Cheshire 06410
Tel: (203) 271-2844
FAX: (203) 272-1704

Pioneer Standard
2 Trap Falls Road
Shelton 06484
Tel: (203) 929-5600

FLORIDA

Anthem Electronics
598 South Northlake Blvd., #1024
Altamonte Springs 32701
Tel: (813) 797-2900
FAX: (813) 796-4880

Arrow/Schweber Electronics
400 Fairway Drive, #102
Deerfield Beach 33441
Tel: (305) 429-8200
FAX: (305) 428-3991

Arrow/Schweber Electronics
37 Skyline Drive, #3101
Lake Mary 32746
Tel: (407) 333-9300
FAX: (407) 333-9320

Avnet Computer
3343 W. Commercial Boulevard
Bldg. C/D, Suite 107
Ft. Lauderdale 33309
Tel: (305) 730-9110
FAX: (305) 730-0368

Avnet Computer
3247 Tech Drive North
St. Petersburg 33716
Tel: (813) 573-5524
FAX: (813) 572-4324

Hamilton Hallmark
3350 N.W. 53rd St., #105-107
Ft. Lauderdale 33309
Tel: (305) 484-5482
FAX: (305) 484-2995

Hamilton Hallmark
10491 72nd St. North
Largo 34647
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FAX: (813) 544-4394

Hamilton Hallmark
7079 University Boulevard
Winter Park 32792
Tel: (407) 657-3300
FAX: (407) 678-4414

Pioneer Technologies Group
337 Northlake Blvd., #1000
Alta Monte Springs 32701
Tel: (407) 834-9090
FAX: (407) 834-0865

Pioneer Technologies Group
674 S. Military Trail
Deerfield Beach 33442
Tel: (305) 428-8877
FAX: (305) 481-2950

Pioneer Technologies Group
8031-2 Phillips Highway
Jacksonville 32256
Tel: (904) 730-0065

Wyle Laboratories
1000 112 Circle North
St. Petersburg 33716
Tel: (813) 530-3400
FAX: (813) 579-1518

GEORGIA

Arrow Commercial Systems Group
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